Assistant Commissioner for Patents Washington, D.C. 20231

In re: Patent Appln. USSN: 09/841,505 Filed: April 24, 2001 Action Day:

Oct 29, 2004

Title: CMOS tapered gate and synthesis method

Inventor(s): Brian W. Curran et al.

Examiner: Magid Y Dimyan Group Art: 5674

Attorney Docket No.: PO9-2000-0107US1

Attorney/Agent: Lynn L. Augspurger, Reg. No.: 24,227 Deposit Acct: 09-0463

Dear Sir:

State of New York County of Dutchess

Affidavit under 37 CFR 1.131

The undersigned Lisa Bryant Lacey before the designated Notary Public declare that the following facts applicable to the above application are true:

That appended code illustrates script that is taken from a file kept in the ordinary course of business at International Business Machines Corporation and printed to correctly illustrate the script which we inventors created and which the undersigned Lisa Bryant Lacey wrote in 1995 to implement the inventions described and claimed in U.S. Serial No. 09/841,505 filed April 24, 2001 entitled "CMOS tapered gate and synthesis method" which was used by Yiu Hing Chan and others at International Business Machines Corporation for synthesis of a working device for testing and proving that the process claimed worked for the intended purpose in 1999 and prior to April, 2001.

Furthermore, the undersigned has also appended hereto an abstract sheet taken from the log showing the use by Yiu Hing Chan documenting 1999 calls to the appended code script which were used for the synthesis method claimed in our patent application which we signed as the the completed patent application filed with the US Patent and Trademark Office in March, 2001 describing and claiming the process implemented by the appended code script. In addition Lisa Bryant Lacey made the an added comment in the log appended to the affidavit of Yiu Hing Chan pointing out the invocation of the TAPERED code of the invention in the file made in order to allow focus on that invocation by a reader of the log.

I make this declaration of facts before the undersigned Notary Public for presentation as proof under 37 CFR 1.131 because the reference to "Hwang" mentioned in the first official action regarding this application of which reference the undersigned Brian W. Curran was an author was made and published after our invention was conceived and reduced to practice.

Sworn to and subscribed before me a Notary Public, in the town of poughkeepsie, county of Dutchess, State of New York on this day of February 2005

Lisa Bryant Lacey

Lyn/ Sandra/Kilmer

Notary Public

Dutchess County New York

SANDRA LYN KILMER Notary Public, State of New York No. 5562885

Qualified in Dutchess County Commission Expires 40, 200 6

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10. 11

Brian W. Curran

Patricia L. Cramer

Notary Public

Dutches County, New York

PATRICIA L CRAIVIER

Notary Public, State of New York

No. 4527213

Qualified in Dutchess County

Qualified in Dutchess County Commission Expires 8 31 3000

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# the U.S. Copyright Office.
#
#
#
   NAME:
#
#
     tcl/late time.tcl, BooleDozer, bdz-4.1 1.8 9/18/98 15:38:46
#
#
   AUTHOR / REVIEWER:
#
#
     Michael Kazda
#
   DESCRIPTION:
#
#
#
     Late timing correction Scenario
#
   MODIFICATIONS:
#
#
#
     Date
             UserID Remark (newest to oldest)
     _____
#
#
     05/24/99 fvg
                    added cycle_steal 11 places. Saved dated backup
                    per dkung, num_clusters from (4) to (16) in lowvt
#
     04/15/99 lbl
     09/18/98 kazda rename interlude due to collision
#
     06/18/98 kazda removed WORST from bufmatch, fanmatch
#
                removed NO_VIOLATIONS from faninv
#
     06/15/98 kazda added gain-based/window repowering
#
# 03/26/98 raze str_parm not ued correctly.
  02/23/98 kazda added progress metering
# 02/16/98 kazda reset to parm offset to zero on exit
  11/19/97 raze syntax error, invalid command substitution
   06/27/97 - MAK - Correct randsim query before invoking
   06/16/97 - MAK - Added final fanout correction after dinv to correct
             any violations introduced by dinv or onebuff
             Correct delay_synlimit for medium in various places.
   05/30/97 DJG Added checksrc to beginning of scenario
   03/27/97 DJG Added INFO_ONLY flag to first checkfan call so as
            not to set the error level.
   02/20/97 HC Added reset_timing.
  11/01/96 CKH Replacing noncritcal repower option LOWEST with
             LOWEST NOT EQUAL, which seems to give a big speedup
   03/05/96 DJG Try to get some statistics
   11/08/95 - NDH - Based upon debugging by Andy, always use fastrpwr()
             instead of quick(repower) initialy.
  10/17/95 - NDH - Added tpushb() and tsteal() to main restructuring loop.
```

```
08/30/95 - NDH - Added randsim query before doing actual check
   08/16/95 - DJG - Added sweep after delBufClks
   07/28/95 - DSK - Added calls to Tony's tempBufClks and delBufClks when
             delay_lim >=4 and ! dont_bufclks
   07/26/95 - NDH - Added tc_parm( CHK_SINKSLEW( X ) ) where X="N" when
#
             we set slew prop to false and X="Y" when we set
#
             slew prop to true. This will ensure that we
#
             accurately measure slew times for fanout correction.
   6/14/95 - DJG - Removed args to late_area.scn it doesn't seem to
#
#
             take any anymore.
#
   1/10/95 - DJG - Added checkfan call right before SLEW calculation
#
             turned on.
   11/07/94 - LNR - Quit if technology is XC4000 or XC3000 or QSV
#
#
   10/04/94 - Chao- Added final slew correction with LTOR order.
   08/31/94 - DJG - Change ATTEMPS to 0 in two places for final legal
#
             fanout correction. 0 is infinite number of tries.
#
   02/17/94 - DJG - Changed to ! new_assert so users will not see change
#
             unless they want it.
  02/07/94 - RLK - Changed call to assert(SLEW/NOSLEW) to set_slew_prop
#
#
             unless is_parm("old_assert") is true.
  10/20/93 - DJG - remove traceset before trulegen
  09/15/93 - JRK - Added chkbuff before the last checkfan
proc late_time {use_sink_limit use_cap_limit args} {
  set delayEffort [get_default_delay_synlimit]
  set areaEffort [get_default_synlimit]
  # initialize some variables here
  set gain_based 0
  set args_num [llength $args]
  # run through the extra argumentes for late timing correction
  for { set i 0 } { $i < $args_num } { incr i } {
    set arg [findex $args [expr $i]]
    switch -regexp -- $arg {
       -gain.*
                     { set gain_based 1 }
       default
                      { error "Parameter not recognized" ?$arg?; }
    }
 }
  echo "In David's Exp. Timing Opt Scenario"
  checkfan
  if ($gain_based) {
    echo "Gain-based Late Time"
    lx_progress_update 0 "Gain-based Late Timing Correction..."
 } else {
    echo "Standard Late Time"
    lx_progress_update 0 "Late Timing Correction..."
 echo "Delay Effort = $delayEffort"
 echo "Area Effort = $areaEffort"
  #cputime
  #set the trace level to HOWMANY
```

```
#traceset "syntrace HOWMANY"
 echo "initialize window repower"
 if {$CTE::use tapered} {
    hide_tapered -clear
 if {$CTE::use_lowvt} {
    hide_lowvt -clear
 init_gain_based_repower "REPOWER_INTERVAL(8)"
 # Check if there are any rules to unhide
 set unhidden [str_parm "unhide_rules"]
 if { [string compare $unhidden ""] != 0 } {
    unhide rules $unhidden
 }
  #hide xpansion defs
 hide_def_with_view "XPANDVIEW,SRULE"
  #clear all hidden flags created by the synthesis process
  syn_hide_boxes_clear
  copy_hide
  #traceset "syntrace NOTRACE"
  trulegen
  traceset "syntrace HOWMANY"
  # set the max fanout value if one is in the parm file
  setmaxfanout
  # set the max number of icells this design can grow to
  set maxarea
  #clear all hidden mapping flags
  nextbox "syn_hide_set(!HIDE_DOMINANT)"
  #do interlude timing measurements
  It interlude
  checksrc
  #set timing mode to NOSLEW
  if {! [is_parm "new_assert"]} {
    assert "NOSLEW"
  } else {
    set slew_prop "OFF"
    tc_parm "CHK_SINKSLEW(N)"
  #initial timing parameter set up
  tc_parm "PINTYPE(OUTPUT_PIN),OFFSET(0)
MARGIN(0), ATTEMPTS(1), ITERATIONS(1), FUZZY(.01), MAX_CRIT(32)"
  if {[info exists env(LOW_POWER)]} {
    tc_parm "USE_POWER,BENEFIT_UNITS(0)"
  } else {
```

```
tc_parm "USE_AREA,BENEFIT_UNITS(0)"
   }
   #if delay limit 0 then simply return
   if {$delayEffort <= 0} {
     return
   # Buffer clock nets to improve run time!
                                                 ADD 19Dec94
   if {! [is_parm "dont_bufclks"] } {
      nextbox "tempBufClks"
 # }
   measure
   tc_parm "SLEW_LIM(100)"
   if {$use_sink_limit > 0} {
     tc_parm "SINK_LIM(100)"
   if \{ suse\_cap\_limit > 0 \} 
     tc_parm "CAP_LIM(100)"
   if [info exists CTE::cycle_steal] {
   cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
   techredund "EQNVIEW"
   simple_map
   critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
   #checkfan
  write_end_point_report -points 3 -paths 1
# write_comprehensive_report -file "bpaths.rpt" -detail -audit
  traceset "repower_paths HOWMANY"
  #traceset "syntrace DEBUG"
  #traceset "init_gain_based_repower WHEREWHAT"
  tc_parm "MARGIN(10000000)"
  repower_paths "FUZZY(0.02)"
  write_end_point_report -points 3 -paths 1
  #quit;
  #tapered_critical
  measure
  lx_progress_update 3 "Initial Logic Cleanup..."
  #initialize cleanup of logic
# tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),OFFSET(-1000)"
# quick "onebuff(SCORE(ALL),NO_VIOLATIONS),dinv(SCORE(ALL),NO_VIOLATIONS)"
  measure
  quick "tcte(SCORE(ALL),NO_VIOLATIONS)"
  measure
```

```
if {$use_sink_limit > 0} {
    tc_parm "SINK_LIM(200)"
 if \{ suse\_cap\_limit > 0 \} 
    tc_parm "CAP_LIM(200)"
 #set capacitance and sink limits
 if {$use_sink_limit > 0} {
    tc_parm "SINK_LIM(100)"
 if {$use_cap_limit > 0} {
    tc_parm "CAP_LIM(100)"
 Ix_progress_update 5 "Initial Pin Swapping..."
 if [info exists CTE::cycle_steal] {
  cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  }
  #initial pin swapping
  fanmatch "ESTIMATED, SORT, ONE_LEVEL"
  treematch "ESTIMATED,TWO_LEVEL,NO_VIOLATIONS"
  measure
  pad_pos
  load_xrule -file "/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule"
  nextbox "synexpand(XPANDVIEW)"
  measure
  write_end_point_report -points 3 -paths 1
  if {$delayEffort >= 4 && $areaEffort <= 6} {
    Ix progress update 41 "Expand AO and merge..."
    #perform an initial expand AO and merge
    add_r_off
    tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
"texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST,SIMILAR,VIEW(TRULE_BASE_A
UTOGEN),NO_VIOLATIONS)"
    add_r_off
    tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
    quick "texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WORST
,VIEW(TRULE_BASE_AUTOGEN)
                                   NO_VIOLATIONS)"
    add_r_off
    tc_parm
```

```
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    quick
"texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST,SIMILAR,VIEW(TRULE_AND_OR
_AUTOGEN)
               ,NO_VIOLATIONS)"
    add_r_off
    tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
    quick "texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,WORST
,VIEW(TRULE_AND_OR_AUTOGEN)
                                    ,NO_VIOLATIONS)"
    add_r_off
    tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    quick "tmerge(SCORE(ALL),ORD2,SORT_PINS,NO_VIOLATIONS)"
  }
  if [info exists CTE::cycle_steal] {
  cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  write_end_point_report -points 3 -paths 1
  lx_progress_update 131 "Powerup..."
  measure
  critical
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS), fantom (LIMITED, REPOWER (EXTERNAL)), faninv (LIMITED, REPOWER (EXTERNAL))"
  nextbox "synexpand(XPANDVIEW)"
  measure
  if [info exists CTE::cycle_steal] {
  cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
 write_end_point_report -points 3 -paths 1
 echo "Finished initial power up"
 # write_end_point_report -points 3 -paths 1
    checkfan
 lx_progress_update 279 "Pin swapping..."
 #swap pins after repowering
 fanmatch "ACTUAL,ONE_LEVEL,NO_VIOLATIONS"
 lx_progress_update 301 "Powering up critical path..."
 #initial powerup
 add_r off
 if {$delayEffort >= 7} {
```

```
tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RANK(5)"
 } else {
    tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1)
  while {1} {
    reset_critical_slack_limit
    repower_paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0} {
      break
    }
  }
  if [info exists CTE::cycle_steal] {
  cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  write_end_point_report -points 3 -paths 1
  if {$delayEffort >= 5} {
    tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    if {! ([has_dual_rail_children "NAND"] ||
    [has dual rail children "NOR"])} {
      #nextbox "tt2lev(TIMING,TECH,CRITICAL,PATTERN_LIMIT(4),FANOUT_LIMIT(1))"
      lx progress update 301 "Recovering and Kernel Factoring..."
      # find recovering from two level boxes
      nextbox "findtt(TWO_LEVEL,BOX(2),LIMITED)"
      nextbox "findtt(TWO_LEVEL,BOX(3),LIMITED)"
      if {$areaEffort >= 7} {
        nextbox "findtt(TWO LEVEL,BOX(4),LIMITED)"
        nextbox "findtt(TWO_LEVEL,BOX(5),LIMITED)"
      nextbox "tkern"
      add_r_off
      tc_parm
"WEIGHTED BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
      nextbox "powerize"
      quick "trecover(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO1FAN,NO_VIOLATIONS)"
    }
    if {$delayEffort >= 7 && $areaEffort <= 6} {
      add r off
      tc parm
"WEIGHTED BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
       quick "texpand(SCORE(ALL), RE POWER, INC, PUSH, SORT PINS,
WORST, SIMILAR, VIEW (TRULE_BASE_AUTOGEN), NO_VIOLATIONS)"
      add_r_off
      tc_parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
```

```
quick "texpand(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,
                                                                       WORST,
VIEW(TRULE_BASE_AUTOGEN),NO_VIOLATIONS)"
       add_r_off
       tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
       quick "texpand(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,
WORST, SIMILAR, VIEW (TRULE_AND_OR_AUTOGEN), NO_VIOLATIONS)"
      add_r_off
      tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
      quick "texpand(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,
                                                                       WORST.
VIEW(TRULE_AND_OR_AUTOGEN),NO_VIOLATIONS)"
      add r off
      tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
      quick "tmerge(SCORE(ALL),RE_POWER,INC,ORD2,SORT_PINS,WORST,NO_VIOLATIONS)"
    }
  }
  measure
  critical
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS), fantom(LIMITED, REPOWER(EXTERNAL)), faninv(LIMITED, REPOWER(EXTERNAL))"
  nextbox "synexpand(XPANDVIEW)"
  measure
  if [info exists CTE::cycle_steal] {
  cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  write_end_point_report -points 3 -paths 1
  lx_progress_update 667 "Pin Swapping..."
  #swap pins in trees
  treematch "ACTUAL ,TWO_LEVEL,NO_VIOLATIONS"
  #swap pins on box
  fanmatch "ACTUAL ,ONE_LEVEL,NO_VIOLATIONS"
  lx_progress_update 690 "Powerup..."
  #more powerup
 add_r_off
 if {$delayEffort >= 7} {
   tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,RANK(5)"
 } else {
   tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED
 while {1} {
   reset_critical slack limit
   repower_paths "FUZZY(0.02)"
   critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
```

```
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare critical slack limit] == 0} {
      break
    }
  }
  for \{ set i 0 \} \{ si < 8 \} \{ incr i \} \{ si < 8 \} \}
    if {[syntrace] >= 10} {
      It_interlude
    }
    echo "inside loop"
    measure
    write_end_point_report -points 3 -paths 1
    reset_critical_slack_limit
    #run all timing correction transforms under critical
    add_r_off
    if {$delayEffort >= 8} {
      tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RANK(5
),DEFAULT_POWER_SCORE(ALL)"
    } else {
      tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),
DEFAULT POWER SCORE(ALL)"
    }
    hide all -no clear
    hide nominal optbeta -clear
    scritflow "trestructure_tree( MAX_INPUTS( 16 ) MAX_DECOMPOSE( 4 ) SORT_PINS
CHECK_INPUTS MIN_INPUTS(2))"
    hide nominal -clear
    if {$CTE::use_tapered} {
      hide tapered -clear
    if {$CTE::use_lowvt} {
      hide lowvt -clear
    #do critical path analysis of all structural transforms
    critical "tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)"
    critical "tsteal(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, UP, NO_VIOLATIONS)"
    critical "tpushl(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
    critical "tpushr(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, NO_VIOLATIONS)"
    critical "tpushb(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
    critical "texpand(SCORE(ALL).PUSH.RE POWER.FASTEST.SORT PINS.SIMILAR.\
         VIEW(TRULE_BASE_AUTOGEN),NO_VIOLATIONS)"
    critical
"texpand(SCORE(ALL),PUSH,COMPLEMENT,RE_POWER,FASTEST,SORT_PINS,SIMILAR,\
         VIEW(TRULE_BASE_AUTOGEN),NO_VIOLATIONS)"
    critical "texpao(SCORE(ALL), PUSH, RE POWER, FASTEST, SORT_PINS, NO_VIOLATIONS)"
    critical "tbmove(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, MULTIPLE_CRITICAL, \
         INVERTC, CLONE, NO_VIOLATIONS)"
    critical "tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,DOWN,NO_VIOLATIONS)"
```

```
critical
 "tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tncube(SCORE(ALL),NO_VIOLATIONS)"
     repower_paths "FUZZY(0.02)"
     repower_paths "FUZZY(0.02), SIMULTANEOUS_REPOWER"
     critical "repower(SCORE(ALL),FASTEST,NO_VIOLATIONS),
 repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
     critical "clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS)"
     critical "onebuff(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS),\
         dinv(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS)"
     critical "tcte(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS)"
     critical "speedreg(RE_POWER),absrbreg()"
     noncritical "speedreg(RE_POWER),absrbreg()"
     hide_all -no_clear
     hide_nominal_optbeta -clear
     scritflow "trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS
CHECK_INPUTS MIN_INPUTS(2))"
    hide_nominal -clear
    if {$CTE::use_tapered} {
      hide_tapered -clear
    if {$CTE::use_lowvt} {
      hide lowvt -clear
    if {[compare_critical_slack_limit] == 0} {
      #lower repower books
      if {$delayEffort <= 3 || $areaEffort >= 4} {
        tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFFSET(0)"
        noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
      } else {
        tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
        noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
      tc_parm "MARGIN(10000000)"
      fanmatch "ACTUAL ,ONE_LEVEL,NO_VIOLATIONS"
      tc_parm "OFFSET(0)"
      tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED"
      tc_parm "REGALL"
      repower_paths "FUZZY(0.02)"
      critical "repower(SCORE(ALL), FASTEST , NO_VIOLATIONS),
repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
      if {[compare_critical_slack_limit] == 0) {
        break
      }
    }
 }
 measure
 critical
```

```
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS).fantom(LIMITED.REPOWER(EXTERNAL)),faninv(LIMITED,REPOWER(EXTERNAL))"
  nextbox "synexpand(XPANDVIEW)"
  measure
  repower_paths "FUZZY(0.02)"
  critical "repower(SCORE(ALL), FASTEST , NO VIOLATIONS),
repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
  if [info exists CTE::cycle_steal] {
  cycle steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  write _end_point_report -points 3 -paths 1
  #do interlude timing measurements
  lt_interlude
  lx_progress_update 1916 "Powering down noncritical paths..."
  #lower repower books
  if {$delayEffort <= 3 || $areaEffort >= 4} {
    tc parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE OFFSET(0)"
    noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
  } else {
    tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
    noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
  tc_parm "MARGIN(1000000)"
  lx_progress_update 1919 "Pin Swapping..."
  #pin swapping
  bufmatch "ESTIMATED,TWO LEVEL,NO VIOLATIONS"
  fanmatch "ACTUAL ,ONE_LEVEL,NO_VIOLATIONS"
  #fix dual rail boxes, swap pins and repower
  if {$delayEffort >= 4} {
    add r off
    tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    if {!$gain_based} {
      quick "tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)"
    #swap pins and repowering
    if ($gain_based) {
      tc_parm "BENEFIT_UNITS(10)"
    tc parm "OFFSET(0)"
    tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED"
    while {1} {
      reset_critical_slack_limit
      critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
      tc parm "REGALL"
      repower_paths "FUZZY(0.02)"
```

- **j** 

```
critical "repower(SCORE(ALL),INC ,NO_VIOLATIONS),
   repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
                      if {[compare_critical_slack_limit] == 0) {
                            break
               if ($gain_based) {
                      tc_parm "BENEFIT_UNITS(0)"
         }
         #checkfan
         write_end_point_report -points 3 -paths 1
         #check that the network has legal connections
         nextbox "chklegal"
         nextnet "chklegal"
         #reduce area if possible
        late_area
        #checkfan
        if [info exists CTE::cycle_steal] {
        cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
        write_end_point_report -points 3 -paths 1
        lx_progress_update 1977 "Checking violations..."
        # check before turning on SLEW propigation
        #checkfan "INFO_ONLY"
        #set timing mode to SLEW
       if {! [is_parm "new_assert"]} {
              assert "SLEW"
       } else {
              set_slew_prop "ON"
             tc_parm "CHK_SINKSLEW(Y)"
       tc_parm "SLEW_LIM(100)"
       lx_progress_update 1977 "Correcting violations..."
       #final legal fanout correction
       if {$use_sink_limit > 0} {
             tc_parm "SINK_LIM(100)"
       if {$use_cap_limit > 0} {
             tc_parm "CAP_LIM(100)"
      }
      critical
"repower(SCORE(ALL),INC,NO\_VIOLATIONS), clone(SCORE(ALL),ACTUAL,RE\_POWER,INC,NO\_VIOLATIONS), clone(ALL), clone(ALL),
ATIONS), fantom (LIMITED, REPOWER (EXTERNAL)), faninv (LIMITED, REPOWER (EXTERNAL))"
      nextbox "synexpand(XPANDVIEW)"
      while {1} {
```

```
reset_critical_slack_limit
    critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
    tc_parm "REGALL"
    repower paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0} {
      break
    }
  }
  if {$CTE::use tapered} {
    #runs tapering on a critical path
    tapered_critical
  #final swapping and repowering for speed
  if {$delayEffort >= 4} {
    lx_progress_update 1980 "Final Swapping and Repowering..."
    tc_parm "OFFSET(0)"
    tc parm
"WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WEIGHTED,DEFAULT_POWER_SCORE(AL
L)"
    nextbox "tkern"
    nextbox "powerize"
    quick "trecover(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,NO1FAN,NO_VIOLATIONS)"
    while {1} {
       reset critical slack limit
       critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
       tc_parm "REGALL"
       repower_paths "FUZZY(0.02)"
       critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
       if {[compare_critical_slack_limit] == 0} {
         break
       }
    }
  if [info exists CTE::cycle_steal] {
  cycle_steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
     write_end_point_report -points 3 -paths 1
     hide all -no clear
     hide nominal_optbeta -clear
     scritflow "trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS
CHECK INPUTS MIN INPUTS(2))"
     hide_nominal -clear
     if {$CTE::use_tapered} {
      hide_tapered -clear
     if {$CTE::use_lowvt} {
```

```
hide_lowvt -clear
     }
     #run transforms under slew
     tc_parm "OFFSET(0)"
     tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1)"
     critical "texpao(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS)"
     if {$delayEffort >= 5} {
       if {$delayEffort >= 8} {
         #run all transforms one last time
         critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
         critical "tshatter(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO_VIOLATIONS)"
         critical
 "tmerge(SCORE(ALL),RE_POWER,INC,ORD2,SORT_PINS,NO_VIOLATIONS),texpand(SCORE(ALL),P
USH,RE_POWER,INC,SORT_PINS,SIMILAR,NO_VIOLATIONS)"
         critical
 "tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tncube(SCORE(ALL),NO_VIOLATIONS)"
         critical
"onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),dinv(SCORE(ALL),RE_POWER,INC,NO_VI
OLATIONS)"
         critical "tcte(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)"
         if {0} {
           # fanout correction without apportionment
           qb fancorr 0
         } else {
           critical "repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)),clone(SCORE(ALL),ACTUAL
,RE_POWER,INC,NO_VIOLATIONS)"
         }
         critical "speedreg(RE_POWER),absrbreg()"
         noncritical "speedreg(RE_POWER),absrbreg()"
      } else {
         #get rid of odd books on critical paths
         critical
"texpand(SCORE(ALL),PUSH,RE_POWER,INC,SORT_PINS,SIMILAR,VIEW(TRULE_BASE_AUTOGEN
),NO_VIOLATIONS)"
         tc_parm "REGALL"
         critical "repower(SCORE(ALL),INC,NO_VIOLATIONS)"
      }
    }
    lx_progress_update 2060 "Correcting violations..."
  }
  echo "doing last techredund"
  traceset "syntrace HOWMANY"
  techredund "EQNVIEW"
  simple_map
  critical
"repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS), fantom(LIMITED, REPOWER(EXTERNAL)), faninv(LIMITED, REPOWER(EXTERNAL))"
  nextbox "synexpand(XPANDVIEW)"
```

```
#traceset "repower_paths DEBUG"
  while {1} {
    reset_critical_slack_limit
    critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
    tc parm "REGALL"
    repower_paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0} {
      break
    }
  }
  #traceset "dinv DEBUG"
  tc parm "SLEW_LIM(120), CAP_LIM(120), SINK_LIM(120)"
"onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),dinv(SCORE(ALL),RE_POWER,INC,NO_VI
OLATIONS)"
  tc_parm "SLEW_LIM(100), CAP_LIM(100), SINK_LIM(100)"
  critical "clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS)"
  #traceset "pushxor DEBUG"
  pushxor "NUM_CLUSTERS(8)"
  #checkfan
  if [info exists CTE::cycle_steal] {
  cycle steal -iterations 30 -epsilon 1 -min_slack 0 -no_verbose
  write_end_point_report -points 3 -paths 1
  Ix progress update 2061 "Removing unnecessary buffers..."
  #removal of buffers with one fanout
  if {$delayEffort <= 3 || $areaEffort >= 4} {
    tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFFSET(0)"
    noncritical "onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
    noncritical "dinv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
  } else {
    tc parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
    noncritical "onebuff(SCORE(ALL), RE_POWER, LOWEST, WORST, NO_VIOLATIONS)"
    noncritical "dinv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIOLATIONS)"
  }
  Ix_progress_update 2061 "Correcting violations..."
  #checkfan
  write_end_point_report -points 3 -paths 1
  if {$CTE::use tapered} {
    #runs lowvt on a critical path
    lowvt_critical
  if {$CTE::use_tapered} {
```

```
#runs tapering on a critical path
    tapered_critical
  }
  if {$CTE::use_tapered} {
    #runs lowvt on a critical path
    lowvt_critical
  write_end_point_report -points 3 -paths 1
  #traceset "repower_paths DEBUG"
  critical "clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS)"
  while {1} {
     reset_critical_slack_limit
    critical "tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS)"
    tc_parm "REGALL"
    repower_paths "FUZZY(0.02), SIMULTANEOUS_REPOWER"
    repower_paths "FUZZY(0.02)"
    critical "repower(SCORE(ALL),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA))"
    if {[compare_critical_slack_limit] == 0) {
      break
    }
  if {$CTE::use_tapered} {
    #runs lowvt on a critical path
   lowvt_critical
 }
 if [info exists CTE::cycle_steal] {
 cycle_steal -iterations 30 -epsilon 1 -no_verbose
 write_end_point_report -points 3 -paths 1
 #make sure you get rid of double buffers
 chkbuff
 #compute the number of inverters following IOPADs and REGs
 dualcnt "REG"
 dualcnt "IOPAD"
 #check that the network has legal connections
 dual_rail_to_single_rail
 nextbox "chklegal"
 nextnet "chklegal"
 #check that network has no anomolies
 checksrc
 #find double buffers
 nextbox "dbuff()"
 reset_timing
```

```
#check fanout
  checkfan
                                                                i
  # Remove clock buffers added at the top of this scenario.
                                                               ADD 19Dec94
  if {! [is_parm "dont_bufclks"]} {
     nextbox "delBufClks"
#
#
     sweep "1"
# }
  lx_progress_update 2068 "Measuring..."
  #do measure
  measure
  #do final interlude timing measurements
  slackhist
  prtdelay
  lt_interlude
  #run randsim
  if {[randsim "q"] != 0} {
    randsim "c"
  }
  ##cputime
  # Try to get some statistics
  good_names
}
# Add Relative Offset
proc add_r_off {} {
  # switch to relative offset depending on synlimit
  switch -regexp [get_default_delay_synlimit] {
     [0-3] { tc_parm "RELATIVE_OFFSET(100)" }
     [4-6] { tc_parm "OFFSET(0)" }
     [7-9] { tc_parm "OFFSET(-0.01)" }
     default { tc_parm "OFFSET(0)" }
}
# Timing Interlude Scenario
proc It_interlude {} {
 #cputime
 #print the worst slack report
 write_end_point_report -points 10
 #check fanout correction
 #checkfan();
 #do measure
 measure
 #check the random simulator
```

```
if {[randsim "q"] != 0} {
  randsim "c"
                                   į.
 }
proc gb_fancorr {apportion} {
 echo "Gain-based fanout correction apportion=$apportion"
 assign_wire_cap
 checksrc
 randsim "c"
 if ($apportion) {
#ALLISPECIAL
  gb_apportion_fanouts "SCALE_INCR(0.6), MIN_BOX_SCALE(0.010), SLACK_TARGET(0.02),
ACC_FACTOR(3.0), USE_INV"
 } else {
#ALLISPECIAL
  gb_apportion_fanouts "SCALE_INCR(0.6), NO_APPORTION, MIN_BOX_SCALE(0.010),
SLACK_TARGET(0.02), ACC_FACTOR(3.0), USE INV"
 }
 checksrc
 assign_wire_cap
 randsim "c"
# write_end_point_report -points 1
 gb_buffer_tree "GAIN_INCR(0.2), CHECK, LOAD_FRAC(0.6), UPPER_GAIN(6.0),
NUM_SLACK_INCR(4), USE_INV"
 checksrc
 nextbox "printbox"
 write_comprehensive_report
 assign_wire_cap
 randsim "c"
# measure ""
# Tapering the cells
proc tapered_critical {} {
 for {set i 0 } {$i < 20} {incr i} {
  reset_critical_slack_limit
  quick
        "tswap(SCORE(ALL),ACTUAL,ONE LEVEL)"
  tc_parm "WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RANK(5)"
  critical "repower(SCORE(ALL), REPOWER_GROUP(TAPERED, TAPERED_PIN_SWAP)"
  critical "repower(SCORE(ALL),NO_VIOLATIONS)"
  critical "repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(BETA))"
  tc_parm "MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFFSET(0)"
  noncritical "repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLATIONS)"
 tc_parm "MARGIN(10000000)"
  if {[compare_critical_slack_limit] == 0} {
```

```
break
  }
                                                                    ij
 }
}
# Lowvt conversion of cells
proc lowvt_critical {} {
   #traceset "repower_paths DEBUG"
  for {set i 0 } {$i < 10} {incr i} {
reset_critical_slack_limit
  write_end_point_report -points 5;
  repower_paths "FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)"
   write_end_point_report -points 5;
  if {[compare_critical_slack_limit] == 0} {
    break
  }
 }
 traceset "repower_paths HOWMANY"
}
```

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Be it known that in connection with my accompanying affidavit and log file appended to an affidavit of Yu-Hing Chan, I, Lisa Bryant Lacey, retrieved the following lines of information, to help clarify. I added a comment in the log "\*\*\*\*\*POU92000-0107US1\*\*\*\*\* code invocation" that should the reader of these pages.

\*\*\*\*\*POU92000-0107US1\*\*\*\*\* code invocation

[tc\_parm]: [set\_benefit\_per\_unit\_cost]: calculated margin is 6.090000

> critical

repower (SCORE (ALL), REPOWER\_GROUP (TAPERED), TAPER...

critical( repower (SCORE (ALL), REPOWER\_GROUP (TAPERED), TAPERED\_PIN\_SWAP)
);
-1865.06 Avg: -167.73

maximum area for proto box IDCDSUC is 4606

repower: setting SCORE option to ALL.

repower: setting TAPERED\_PIN\_SWAP option.

Also, to document the date, note that the log maintains the date when run

\*\*\*\*\*POU92000-0107US1\*\*\*\*\* code invocation date

Sun Apr 18 21:58:17 1999

Part : IDCDSUC

Lisa Bryant Lacey

Sworn to an subscribed before me, this 23 day of February, 2005

At Poughkeepsie, New York.

Sandra Kilmer, Notary Public, Dutchess County, New York

LYN

SANDRA LYN KILMER
Notary Public, State of New York
No. 5562885
Qualified in Dutchess County

Qualified in Dutchess County Commission Expires 20, 2006

1

Assistant Commissioner for Patents Washington, D.C. 20231

Filed: April 24, 2001 Action Day: In re: Patent Appln. USSN: 09/841,505

Oct 29, 2004

Title: CMOS tapered gate and synthesis method

Inventor(s): Brian W. Curran et al.

Group Art: 5674 Examiner: Magid Y Dimyan

Attorney Docket No.: PO9-2000-0107US1

Attorney/Agent: Lynn L. Augspurger, Reg. No.: 24,227 Deposit Acct: 09-0463

Dear Sir:

State of New York County of Dutchess

Corroborating Affidavit under 37 CFR 1.131

The undersigned Yiu Hing Chan before the designated Notary Public declare that the following facts applicable to the above application are true:

That I am a design engineer for International Business Machines Corporation and that the appended log printed from a log of work showing me using a tool which I used in 1999 when I was employed by International Business Machines Corporation, Poughkeepsie, New York, for testing the synthesis of working devices in accordance with a new method described in the aforementioned application and claims which I have read and understood. The appended log is a print from the log file kept by International Buiness Machines Corporation of my work and shows that in 1999 I personally used the code written by Lisa Bryant Lacey to implement the inventions described and claimed in U.S. Serial No. 09/841,505 filed April 24, 2001 entitled "CMOS tapered gate and synthesis method" and which I and others at International Business Machines Corporation used for synthesis of a working device for testing and proving that the process claimed worked for the intended purpose in 1999 and prior to April, 2001, and I say that the method of synthesis worked for me for the intended purpose in 1999 in accordance with the steps recited in the claims of US Patent Application Serial No. 09/841,505 which I have read and understand. Note that this log has an added comment pointing out the invocation of the TAPERED code of the invention in the file made in order to allow focus on that invocation by a reader of the log where the first line is Login: \*BATCH\* ibm5081 bsp5n11

I make this declaration of facts before the undersigned Notary Public for presentation as proof under 37 CFR 1.131 in the aforesaid application because the reference to "Hwang" mentioned in the first official action regarding this application of which inventor Brian W. Curran was an author was made and publiched after the invention was conceived and reduced to practice of my own knowledge.

Sworn to and subscribed before me a Notary Public, in the town of Poughkeepsie, county of Dutchess, State of New York on this \_ February 2005.

Yiu Hing Chan

Sandral Kilmer Notary/Public

SANDRA LYN KILMER Notary Public, State of New York

No. 5562885 Dutchess County New York Qualified in Dutchess County Commission Expires 2006

Login: \*BATCH\* ibm5081 bsp5n11

Initializing environment for the Alliance 00 project (apd) ...

Initialized for apd...

Initializing for CHIPID=alliance00\_cp ...

CTE: Initializing CTE environment @ apd.pok.ibm.com ...
CTE: Customizing CTE environment for project: alliance00 ...

CTE: Customizing CTE environment via user ./.cterc ...

\_\_\_\_\_

running: /afs/watson/projects/vlsi/cte/tools/bd2/0401v2/booledozer/4.1/bin/bdz -source ctesynz\_cp.tcl

**BooleDozer Logic Synthesis** 

Version 4.1 for AIX 4.1 Nutshell version 1.672 (03-25-1999)

Licensed Materials - Property of IBM 5765-802 (C) Copyright IBM Corporation 1998 All Rights Reserved

## IBM and BooleDozer are Trademarks of IBM Corporation

Install Directory: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0

Machine: bsp5n11, AIX 4.1 32bit, 595 POWER2 (L1 i32k d128k, L2 0k), 1 cpu

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/.bdz Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte\_site\_init.tcl

[CTE::site\_init]: Starting cte Bdz under Nutshell site customization...

[CTE::site\_init]: SEARCH auto\_path set to . ./tcl ./dll /afs/apd.pok.ibm.com/u/laceyl/tcl

/afs/apd.pok.ibm.com/u/laceyl/dll /afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/tcl

/afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/dll /afs/watson/projects/vlsi/cte/tools/synzilla/1.0/tcl

/afs/watson/projects/vlsi/cte/tools/synzilla/1.0/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/tcl

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/dll

/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/dft

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte\_defaults.tcl

[CTE::site\_init]: reading cte\_defaults.tcl [CTE::site\_init]: done reading defaults.tcl

Loading: /afs/apd.pok.ibm.com/func/vlsi/alliance00/timing/parms/cp.tcl

Loading: /afs/apd.pok.ibm.com/func/vlsi/alliance00/timing/bsiu/batchz/batch/idcdsuc.tcl

[CTE::site init]: ::CTE::site is gp390

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte\_setup\_tech.tcl

[CTE::site init]: Done

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/dll-rs6000/parmdb.dll

parmdb.dll version 0.0 (Mar 09 1999 20:01:28)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/idm/16/dll-rs6000/idm.dll

idm.dll version 16.0 (Mar 17 1999 03:19:04)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/srule.dll

srule.dll version 4.1 (Apr 14 1999 13:00:07)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/booledozer.dll

booledozer.dll version 4.1 (Apr 14 1999 17:19:37)

BooleDozer Build Version: 4.1.136

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/auto\_setup.tcl

[auto\_setup.tcl]: Loading std auto\_setup...

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/auto\_setup.tcl

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/wizard/3.1/tcl/wiz\_setup.tcl

[auto\_setup.tcl]: Initializing cte specific auto\_source and auto\_load commands...

[auto\_setup.tcl]: CTE::run\_dft not set to true - 'insscan' overridden with no op procedure [auto\_setup.tcl]: Done

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/create\_keywords.tcl [create\_keywords.tcl]: Loading std create\_keywords...

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/create\_keywords.tcl [create\_keywords.tcl]: Initializing cte specific create\_keywords...

[create\_keywords.tcl]: Done

Reading srule

"/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/rules/all/tib/srule/tib.srule". Parsed 35 ruledefs, 0 powerdefs, 95 groups, 69 rulepins.

bdz> bdz\_post\_srule

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/import\_export.tcl [BLDEQN-12]: CMVC version 1.34 compiled on Apr 13 1999 at 18:02:41.

[BD-450047]: CMVC version 1.17 compiled on Apr 13 1999 at 18:03:05.

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/icmcom.dll icmcom.dll version 3.1 (Mar 10 1999 09:48:07)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/icmvim.dll icmvim.dll version 3.1 (Mar 10 1999 09:48:09)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/dll/license.dll

license.dll version 3.1 (Apr 07 1999 14:28:56)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/icmsrc.dll icmsrc.dll version 3.1 (Mar 24 1999 00:37:00)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/einsengine.dll einsengine.dll version 3.1 (Mar 24 1999 22:38:48)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/rice/4.0/.dll-rs\_aix41/rice.dll rice.dll version 4.0 (Apr 07 1999 22:51:55)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/itvui.dll itvui.dll version 3.1 (Mar 24 1999 00:38:36)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/itvrc.dll itvrc.dll version 3.1 (Mar 10 1999 09:48:30)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/itvpd.dll itvpd.dll version 3.1 (Mar 25 1999 11:18:07)

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/einstimer.dll einstimer.dll version 3.1 (Mar 24 1999 22:39:01)

[ET-101]: Initializing EinsTimer...

CMVC Release Level: 03.01

Compiled: Wed Mar 24 22:00:23 1999

[ET-102]: EinsTimer Version 3 Release 1 Licensed Materials-Property of IBM

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"IBM" and "EinsTimer" are trademarks of

"International Business Machines"

[ET-110]: License obtained for ..... EinsTimer 1.1

Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs\_aix41/itvrep.dll itvrep.dll version 3.1 (Mar 24 1999 00:39:43)

```
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvpower.dll
itypower.dll version 3.1 (Mar 24 1999 00:40:25)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvelec.dll
itvelec.dll version 3.1 (Mar 22 1999 23:52:50)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvete.dll
itvete.dll version 3.1 (Mar 22 1999 23:52:56)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/assertTimer.dll
assertTimer.dll version 1.0 (Apr 14 1999 13:00:13)
Timing Assertion Code
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/bdztime.dll
bdztime.dll version 4.1 (Apr 15 1999 13:15:19)
[BD-101]: License Obtained for ..... BooleDozer 4.x
[make_feedthru_boxes]: IOPADs, BRKPTs, etc. set to FEEDTHRU boxes.
Loading: /afs/apd.pok.ibm.com/u/laceyl/.bdz_variables
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/ctesynz_cp.tcl
  > set trace -debug level -key tbmove
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/itvcdc.dll
itvcdc.dll version 3.1 (Mar 22 1999 23:53:02)
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/dll/cte.dll
cte.dll version 1.0 (Apr 13 1999 13:39:58)
CTE BooleDozer under Nutshell compiled code
cte_ci_init
     > CTE::tfuzz
Delays are given in units of 1.000000e-09 seconds
                                 > load_logic_rule -tech blackbox -srule /afs/apd/func/vlsi...
Fuzziness is 1.000000e-03
Reading srule "/afs/apd/func/vlsi/alliance00/bscc8/prod/srule/latches.srule".
[SRULE-17015]: line 24: Keyword "RACEFREE" not defined, adding as VARTYPE_STRING.
[SRULE-17015]: line 242: Keyword "SCAN_ONLY" not defined, adding as VARTYPE_STRING.
[SRULE-17015]; line 243; Keyword "NODEF" not defined, adding as VARTYPE_STRING.
Parsed 22 ruledefs, 0 powerdefs, 60 groups, 214 rulepins.
bdz> load xrule -file {/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/latches.xrule}
         > load xrule -file /afs/apd/func/vlsi/alliance00/bscc8/pro...
[BD-450042]: Reading XRULE file '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/latches.xrule'
[BD-450041]: File '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/latches.xrule' is being read under VIEW
'XPANDVIEW'
bdz> bdz_post_srule
           > bldegn
[BLDEQN-29]: (W) note - \" no longer needed in srules (only this one warning)
           > newgen
       > check_logic_rule -technology BLACKBOX -drop_inputs
CMVC version 1.39 compiled on Apr 8 1999 at 05:49:53.
[SRULE-2]: (W) "latches.srule", line 318, Rule L_AO22:AO does not have power level children
[SRULE-2]: (W) "latches.srule", line 332, Rule L_AO222:AO does not have power level children
[SRULE-2]: (W) "latches.srule", line 351, Rule L_AO2222:AO does not have power level children
[SRULE-2]: (W) "latches.srule", line 276, Rule L_AOI22:AOI does not have power level children
[SRULE-2]: (W) "latches.srule", line 299, Rule L_AOI222:AOI does not have power level children
[SRULE-2]: (W) "latches.srule", line 268, Rule L_NAND:NAND does not have power level children
[SRULE-2]: (W) "latches.srule", line 290, Rule L_NAND3:NAND does not have power level children
[SRULE-2]: (W) "latches.srule", line 374, Rule L_NAND4:NAND does not have power level children
[SRULE-2]: (W) "latches.srule", line 261, Rule L_NOT:NOT does not have power level children
[SRULE-2]: (W) "latches.srule", line 23, Rule XDLATR:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 241, Rule XLATSO:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 388, Rule XDLATCORE:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 412, Rule XSCANCORE:REG does not have power level children
[SRULE-2]: (W) "latches.srule", line 209, Rule XLAT8R:SEQUENTIAL does not have power level children
```

[SRULE-1]: (W) "latches.srule", line 23, Pin group M\_OUT on XDLATR:REG has no pins in it [SRULE-1]: (W) "latches.srule", line 388, Pin group M\_OUT on XDLATCORE:REG has no pins in it [SRULE-1025]: (E) "latches.srule", line 23, Pin group M\_OUT on box XDLATR has zero pins [SRULE-1025]: (E) "latches.srule", line 388, Pin group M\_OUT on box XDLATCORE has zero pins [CTE::setup\_bscc8]: setting ctesrule

> load\_logic\_rule -tech CC8S -srule /afs/apd/func/vlsi/all...

Reading srule "/afs/apd/func/vlsi/alliance00/bscc8/prod/srule/bscc8.srule.synz".

[SRULE-17015]: line 8: Keyword "BLOCK\_TOP" not defined, adding as VARTYPE\_STRING.

[SRULE-17015]: line 9: Keyword "GRP0" not defined, adding as VARTYPE\_STRING.

[SRULE-17015]: line 3210: Keyword "ISCB" not defined, adding as VARTYPE\_STRING.

Parsed 76 ruledefs, 1985 powerdefs, 206 groups, 361 rulepins.

bdz> bdz\_post\_srule

- > bldegn
- > newgen
- > load\_xrule -file /afs/apd/func/vlsi/alliance00/bscc8/pro...

[BD-450042]: Reading XRULE file '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule'

[BD-450041]: File '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule' is being read under VIEW 'XPANDVIEW'

> check\_logic\_rule -technology CC8S -drop\_inputs

CMVC version 1.39 compiled on Apr 8 1999 at 05:49:53.

[SRULE-2]: (W) "bscc8.srule.synz", line 8, Rule cs\_kvdd:CONSTANT does not have power level children

[SRULE-2]: (W) "bscc8.srule.synz", line 12, Rule cs\_kgnd:CONSTANT does not have power level children

[SRULE-9]: (W) "bscc8.srule.synz", line 3191, One of the power levels of cl\_scan:REG should be the default

(first power level cl\_scanonly will be used)

[SRULE-2]: (W) "bscc8.srule.synz", line 3232, Rule cb\_clk\_32\_1:SEQUENTIAL does not have power level children

> load\_cdc\_rule -rule /afs/apd/func/vlsi/alliance00/bscc8/...

[ET-1757]: Initializing CDC...

[ET-1758]: Rule = /afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface\_RS6K

[ET-607]: Starting the dynamic link to CDC for rule:

/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface\_RS6K

[DCL-512]: DCL Runtime Environment Version 3.1

Last compiled on Apr 12 1999 at 10:00:33.

[DCL-642]: I am running in process ID 92476

[DCL-17001]: RLEV: DCMinterface rule, version v1.0.2 IEEE 1481-1998, technology GENERIC, was compiled on 14:17:33 at Mar 12 1999

[DCL-19009]: CAP: Setting DEFAULT PINCAP value to: 0 as defined by environment variable <DCM\_DEFAULT\_PINCAP>

[DCL-17001]: RLEV: Methods subrule, version v1.0.2 IEEE 1481-1998, was compiled on 14:17:39 at Mar 12 1999

[DCL-19021]: INFO: Maximum number of DCM messages to be printed has been set to 100000000

[DCL-17001]: RLEV: LimitPrint subrule, version v1.0 IEEE 1481-1998, was compiled on 14:17:44 at Mar 12 1999

[DCL-17001]: RLEV: printSummary subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:37 at Mar 12 1999

[DCL-17001]: RLEV: Ceffective subrule, version v1.0 IEEE 1481-1998, was compiled on 14:17:50 at Mar 12 1999

[DCL-19000]: ENV: Environment variable < DCMCAPTHRESHOLD > NOT set by user.

[DCL-19017]: CAP: EffectiveC Cap Threshold not set.

[DCL-17001]: RLEV: techSpec subrule, version v1.0.3 IEEE 1481-1998, was compiled on 14:17:56 at Mar 12 1999

[DCL-17001]: RLEV: WireLoad subrule, version v1.0.1 IEEE 1481-1998, was compiled on 14:18:04 at Mar 12 1999

[DCL-17001]: RLEV: WireLoad table, Version 1.0.1 IEEE 1481-1998 Technology SA27, was compiled on 14:18:04 at Mar 12 1999

[DCL-17040]: The available wireload model levels are: 5lm, 6lm

[DCL-17002]: Environmental variable DCMWireLoadLevels not set using default.

[DCL-17001]: RLEV: NetDelay subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:12 at Mar 12 1999

[DCL-17001]: RLEV: cellName subrule, version v1.5 IEEE 1481-1998, was compiled on 14:18:17 at Mar 12 1999

[DCL-17001]: RLEV: CellName parser subrule, version v1.0.5 IEEE 1481-1998, was compiled on 14:18:30 at Mar 12 1999

[DCL-17001]: RLEV: Defaults subrule, version v1.0.4 IEEE 1481-1998, was compiled on 14:18:40 at Mar 12 1999

[DCL-17012]: Using the default supplied bomFile

[DCL-17001]: RLEV: \_cc8s\_rules\_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 09:32:54 at Apr 12 1999

[DCL-17001]: RLEV: \_cc8s\_latches\_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 12:12:01 at Apr 6 1999

[DCL-17001]: RLEV: railCache subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:52 at Mar 12 1999

[DCL-17020]: Environmental variable DCMDoRangeCheck set to do no reporting.

[ET-655]: IEEE standard interface version "IEEE 1481-1998" for technology "GENERIC". Library identification: "IBM\_GENERIC".

[ET-652]: (W) Could not find IEEE standard routine dpcmGetDelayGradient in rules. Substituting dummy routine.

[ET-652]: (W) Could not find IEEE standard routine dpcmGetSlewGradient in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGetAETCellPowerWithSensitivity in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGroupGetSettlingTime in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGroupGetSimultaneousSwitchTime in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmCalcPartialSwingEnergy in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmSetInitialState in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmFillPinCache in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmFreePinCache in rules. Substituting dummy routine.

[ET-653]: (W) Could not find IEEE standard power routine dpcmGetNetEnergy in rules. Substituting dummy routine.

[ET-611]: Dynamic link to CDC rule complete.

> source hide.tcl

```
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/hide.tcl > hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao... > hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao... > hide -no_clear -cells { cs_buffe } > hide -no_clear -cells { cs_invvn cs_invvv }
```

> hide -no\_clear -cells { cs\_nnd2f cs\_nnd2g cs\_nnd2n cs\_nn... > hide -no\_clear -cells { cs\_nnd3f cs\_nnd3g cs\_nnd3h cs\_nn...

> hide -no\_clear -cells { cs\_nnd4n cs\_nnd4v }

> hide -no\_clear -cells { cs\_nor2f cs\_nor2g cs\_nor2n cs\_no...

> hide -no\_clear -cells { cs\_nor3f cs\_nor3g cs\_nor3h cs\_no... > hide -no\_clear -cells { cs\_oa12f cs\_oa12g cs\_oa12n cs\_oa...

> hide -no\_clear -cells { cs\_oa21n cs\_oa21v }

> hide -no\_clear -cells { cs\_oa22n cs\_oa22v }

> hide -no\_clear -cells { cs\_xbn2n cs\_xbn2v }

> hide -no\_clear -cells { cs\_xbo2n cs\_xbo2v }

> find cell cs\_\*

> hide -no\_clear -cells {cs\_ao12f03b cs\_ao12f03c cs\_ao12f0...

> find cell cs buffe\*

> hide -no\_clear -cells {cs\_buffe01a cs\_buffe02a cs\_buffe0...

> hide -clear -cells { "cs\_invvn" }

> find cell cs invvn\*

> hide -clear -cells {cs\_invvn01b cs\_invvn01c cs\_invvn01d ...

> hide -clear -cells { "cs\_nnd2n" }

> find cell cs nnd2n\*

> hide -clear -cells {cs\_nnd2n02b cs\_nnd2n02c cs\_nnd2n02d ...

> hide -clear -cells { "cs\_nnd3n" }

```
> find cell cs_nnd3n*
  > hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
  > hide -clear -cells { "cs_nnd4n" }
   > find cell cs_nnd4n*
   > hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
   > hide -clear -cells { "cs nor2n" }
   > find cell cs nor2n*
   > hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
   > hide -clear -cells { "cs_nor3n" }
   > find cell cs_nor3n*
   > hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
   > hide -clear -cells { "cs_ao12n" }
   > find cell cs_ao12n*
   > hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
   > hide -clear -cells { "cs_ao21n" }
   > find cell cs_ao21n*
   > hide -clear -cells {cs ao21n03b cs ao21n03c cs_ao21n03d ...
   > hide -clear -cells { "cs_ao22n" }
   > find cell cs ao22n*
   > hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
   > hide -clear -cells { "cs_oa12n" }
   > find cell cs_oa12n*
   > hide -clear -cells {cs_oa12n03b cs_oa12n03c cs_oa12n03d ...
   > hide -clear -cells { "cs_oa21n" }
   > find cell cs_oa21n*
   > hide -clear -cells {cs_oa21n03b cs_oa21n03c cs_oa21n03d ...
   > hide -clear -cells { "cs_oa22n" }
   > find cell cs oa22n*
   > hide -clear -cells {cs oa22n03b cs oa22n03c cs_oa22n03d ...
   > hide -clear -cells { "cs_buffe" }
   > find cell cs buffe'
   > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
   > hide -clear -cells { "cs_xbo2n" }
   > find cell cs_xbo2n*
   > hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
   > hide -clear -cells { "cs_xbn2n" }
   > find cell cs_xbn2n*
   > hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
    > read_vim -def IDCDSUC -view HISVHDL -lib /afs/apd/func/v...
Reading proto IDCDSUC...
Reading proto DLAT_SCAN#1#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#1#B_0#1.LATCH...
bdz> vim_postimport __CiType_16_30aada78
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
```

```
> sweep 1
          > his attributes
          > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
          > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
          > nextnet ms2dot(BUS)
        > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30aad4e0
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim_idm_mem CURRENT
Reading proto IDCDSUC_MAC.LATCH.CONCSTMS...
bdz> vim_postimport __CiType_16_31471e98
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
       > trim_idm_mem CURRENT
Reading proto DLAT_SCAN#2#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#2#B 00#1.LATCH...
bdz> vim_postimport __CiType_16_3148a228
         > nextnet xpndbundles
```

```
> brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet with test test worth(FALSE),delname(SAVE)
        > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_30a55270
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is parm a penny saved is a penny earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim idm mem CURRENT
Reading proto DLAT_SCAN#12#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#12#B_00UUUUUUUUU#1.LATCH...
bdz> vim_postimport __CiType_16_30a6aea0
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is parm a penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
```

> padnet

```
> sweep 1
         > his attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim_idm_mem CURRENT
bdz> vim_postimport __CiType_16_3148b770
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim_idm_mem CURRENT
Reading proto DLAT_SCAN#3#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#3#B_00U#1.LATCH...
bdz> vim_postimport __CiType_16_30a6f328
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
       > trim_idm_mem_CURRENT
bdz> vim_postimport __CiType_16_30a6ada0
        > nextnet xpndbundles
         > padnet
```

```
> nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test_test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox with test test key(SYN_CONCAT), one in
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim_idm_mem CURRENT
Reading proto DLAT_SCAN#4#B_0#2#1#0#B_.LATCH...
Reading proto DLATTEST#4#B_00UU#1.LATCH...
bdz> vim_postimport __CiType_16_30a71048
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is parm a penny_saved_is_a_penny_earned
          > nextnet with test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim idm mem CURRENT
bdz> vim_postimport __CiType_16_30a6e6e0
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
```

> brkloops

```
> his_attributes
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim idm mem CURRENT
bdz> vim_postimport __CiType_16_30a445c8
         > nextnet xpndbundles
         > padnet
         > brkloops
         > nextbox xpndarr
         > is_parm a_penny_saved_is_a_penny_earned
          > nextnet_with_test test_worth(FALSE),delname(SAVE)
         > nextbox xpndconcat
         > nextbox_with_test test_key(SYN_CONCAT),onein
         > nextbox xpndiopad
         > nextbox_with_test {test_def(BRKPT), xpndprim}
         > nextbox_with_test {test_def(DOT), xpndintbidi}
[xpndintbidi]: 0 intbidi boxes expanded
         > sweep 1
         > his_attributes
[BD-350205]: (W) No config rule exists for attribute 'PIN_FUNCTION' on IDM_PROTO_PIN_TYPE
'clkl_mode7->clkl_mode7', defaulting to string.
         > nextbox bindcmpnt(BHC)
[insscan]: CTE::run_dft not set to true - 'insscan' overridden with no op!
         > sweep 1
         > nextbox_with_test test_key(ARITHMETIC_TYPE,TWOS_COMPLEME...
         > nextnet ms2dot(BUS)
        > trim idm mem CURRENT
[ctesynz_cp.tcl]: model loaded aokay...flattening...
  > expand -hierarchy
bdz> post_expand
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/post_expand.tcl
     > sweep
     > delbrkpt BREAKLOOPS
     > brkloops
     > nextnet {delkey( EDIFNAME )}
     > nextbox {delkey( EDIFNAME )}
          > set nochange
          > rtolbox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
          > ltorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
          > sweep
         > nochange
          > set_nochange
          > rtolbox_with_test test_key(IOPAD_LOCATION,2).rm_dangling...
          > Itorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
          > sweep
         > nochange
     > nextbox_with_test test_key(IOPAD_LOCATION,2),resolve net...
     > nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
     > sweep
     > nextbox merge_dots()
```

```
> nextbox dot2ms()
     > nextnet {ms2dot( BUS )}
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/hisprep.tcl
    > proto_get_int HIS_BD_VIM_SYNC,0
    > proto get int HISPREPSCN.0
    > createkwd HISPREPSCN, VARTYPE_INTEGER, CLAS_PROTO_BOX
    > proto_set_key HISPREPSCN,1
     > nextnet_with_test test_worth(FALSE,NO_QUALIFIER),delname...
    > synsasname PROTECT
    > syn_hide_from_keywords
[SRULE-17200]: 0 LOGIC_STYLE keywords set on usage boxes from proto box keyword
[SRULE-17205]: 0 LOGIC STYLE keywords were found on usage boxes
ISRULE-17210]: 0 SYN USAGE BOX HIDE keywords set on usage boxes
    > nextbox exprnway,exprnot,exprorsel
    > nextbox with test test syn_hide(!HIDE_MAP,!HIDE_DOMINANT...
    > nextbox expropt1(SSS,SSG,GSG,SGG),exprxpnd
    > expr_reset
    > nextbox_with_test test_key(LOGIC_STYLE,DATA_FLOW),syn_hi...
    > nextbox bindvhdltibs
    > nextbox_with_test test_clkcomp,eq2and,onein
    > nextbox_with_test test_key(ADDER_EXPANSION),comp2sub
    > nextbox xpndadd(USE_TIB)
    > nextbox xpndabs
    > nextbox xpndregs
    > nextbox makesrl
    > nextbox impregs
    > is_parm new_assert
    > nextbox xpndcmpnt,xpndprim
[ET-203]: Timing top level created for design: IDCDSUC, analysis mode: default.
    > cleanup 1
    > delbrkpt BREAKLOOP
    > brkloops ERROR
    > keyword_is_defined {BEC_HISPREP, CLAS_PROTO_BOX}
[BD-354300]: Keyword BEC_HISPREP for object_class CLAS_PROTO_BOX has <NOT> been defined
      > echo {<<< hisprep.scn called from synthesis, running cle...
<<< hisprep.scn called from synthesis, running cleanse >>>
      > cleanse
    > nextbox eq2and
    > constant selector
    > elimdc ZERO
    > cleanup 1
     > keyword is defined {BEC_HISPREP, CLAS_PROTO_BOX}
[BD-354300]: Keyword BEC_HISPREP for object_class CLAS_PROTO_BOX has <NOT> been defined
      > echo {<<< hisprep.scn called from synthesis, running cle...
<<< hisprep.scn called from synthesis, running cleanse >>>
      > cleanse
     > move_component_times
     > copyinfo
     > Itorbox deldang()
     > checksrc
[BD-40101]: (W) Disconnected input port clkl_mode7.
[BD-40101]: (W) Disconnected input port clkg2.
[BD-40129]: Network IDCDSUC had no old problems.
[BD-40130]: (W) Network IDCDSUC has 2 potential problem(s).
```

> source cte\_clock\_block\_processing.tcl

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte\_clock\_block\_processing.tcl > summary\_report

[measure]: Compiled on Mar 12 1999 at 05:03:29.

```
The model <IDCDSUC> has:
```

**Primary Inputs** 122 **Primary Outputs** 73 **Primary BIDIs** 0 Signals 1187 **Gate Count** 863 Connections 2051 Master REG Bits 83 Slave REG Bits 83 Internal Area 4790 External Area 0 Gates/Connects 0.420770 Fanout Count 2051 Average Fanout 1.727885 Avg Tech Box Size = 5.550406 Tech Box Size Stddev = 0.023559 Power 0.000000

\*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\*

 Real signals
 =
 814

 Real boxes
 =
 488

 Real connections
 =
 1676

 Real LSTs
 =
 2490

 Real ICells/box
 =
 9.815574

 Real LSTs/box
 =
 5.102459

 Real nets/box
 =
 1.668033

Cell Total Each Cell

Type Cnt Boxname		Power Level Function Int Ext Power Int Ext Power
164	AND	> AND 0 0 0.000 0 0 0.000
180	BRKPT	> BRKPT 0 0 0.000 0 0 0.000
195	IOPAD	> IOPAD 0 0 0.000 0 0 0.000
62	NAND	> NAND 0 0 0.000 0 0 0.000
23	NOR	> NOR 0 0 0.000 0 0 0.000
91	OR	> OR 0 0 0.000 0 0 0.000
83	XDLATCORE	> REG 0 0 0.000 0 0 0.000
1	cb_mode_block	A > SEQUENTIAL 70 0 0.000 70 0 0.000
59	XRFCBA	A > SEQUENTIAL 80 0 0.000 4720 0 0.000
5	XOR	> XOR 0 0 0.000 0 0 0.000

## [End of measure]

[measure]: Execution time was 0.0 seconds.

[cte\_clock\_block\_processing.tcl]: cb\_mode\_block

> CTE::mode\_block DEF(cb\_mode\_block)

[mode\_block]: Rel 1.0 Compiled on Jan 7 1999 at 18:31:02.

> source cte\_fixmodeblock.tcl

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte\_fixmodeblock.tcl > unpadnet

```
> idm::filter -on gates -expr {[regexp XRFCBA @def_name ]}
```

- > idm::object\_name \_\_CiType\_18\_305b89c8
- > led::connect\_net -net clkl\_mode7 -pin slow\_mode.clockblo...
- > idm::object\_name \_\_CiType\_18\_305b8c38
- > led::connect\_net -net clkl\_mode7 -pin ru\_rq\_blk.clockblo...
- > idm::object\_name \_\_CiType\_18\_305b8ea8
- > led::connect\_net -net clkl\_mode7 -pin iu\_rst\_fst.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d17d8
- > led::connect\_net -net clkl\_mode7 -pin iu\_restart.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d1a48
- > led::connect\_net -net clkl\_mode7 -pin ia\_to\_if.clockbloc...
- > idm::object\_name \_\_CiType\_18\_305d1cb8
- > led::connect\_net -net clkl\_mode7 -pin frc\_mmode.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d1f28
- > led::connect\_net -net clkl\_mode7 -pin local\_milli.clockb...
- > idm::object\_name \_\_CiType\_18\_305d2198
- > led::connect\_net -net clkl\_mode7 -pin ia\_to\_if\_t1.clockb...
- > idm::object\_name \_\_CiType\_18\_305d2408
- > led::connect\_net -net clkl\_mode7 -pin mia\_to\_if.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d2678
- > led::connect\_net -net clkl\_mode7 -pin slow\_mode\_t1.clock...
- > idm::object\_name \_\_CiType\_18\_305d28e8
- > led::connect\_net -net clkl\_mode7 -pin iq\_empty\_dly.clock...
- > idm::object\_name \_\_CiType\_18\_305d2b58
- > led::connect\_net -net clkl\_mode7 -pin slow\_mode\_t2.clock...
- > idm::object\_name \_\_CiType\_18\_305d2dc8
- > led::connect\_net -net clkl\_mode7 -pin s390\_updt\_blk.cloc...
- > idm::object\_name \_\_CiType\_18\_305d3038
- > led::connect\_net -net clkl\_mode7 -pin srlz\_nomatch.clock...
- > idm::object\_name \_\_CiType\_18\_305d32a8
- > led::connect\_net -net clkl\_mode7 -pin bce\_hold\_aa.clockb...
- > idm::object\_name \_\_CiType\_18\_305d3518
- > led::connect\_net -net clkl\_mode7 -pin srlz\_actn.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d3878
- > led::connect\_net -net clkl\_mode7 -pin op\_44\_dcd.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d3ae8
- > led::connect\_net -net clkl\_mode7 -pin op\_cmp\_tr.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d3d58
- > led::connect\_net -net clkl\_mode7 -pin num\_dcd.clockblock...
- > idm::object\_name \_\_CiType\_18\_305d40b8
- > led::connect\_net -net clkl\_mode7 -pin mia\_to\_if\_t1.clock...
- > led::connect\_net -net clkl\_mode7 -pin eu\_op\_encode.clock...
- > idm::object\_name \_\_CiType\_18\_305d4fe8
- > led::connect\_net -net clkl\_mode7 -pin frc\_blk\_1cyc.clock...
- > idm::object\_name \_\_CiType\_18\_305d5258
- > led::connect\_net -net clkl\_mode7 -pin local\_milli\_t1.clo...
- > idm::object\_name \_\_CiType\_18\_305d54c8
- > led::connect\_net -net clkl\_mode7 -pin local\_milli\_t2.clo...
- > idm::object\_name \_\_CiType\_18\_305d5738
- > led::connect\_net -net clkl\_mode7 -pin bht\_block.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d59a8
- > led::connect\_net -net clkl\_mode7 -pin srlz\_blk.clockbloc...
- > idm::object\_name \_\_CiType\_18\_305d5c18
- > led::connect\_net -net clkl\_mode7 -pin exc\_cond.clockbloc...

```
> idm::object_name __CiType_18_305d5e88
```

- > led::connect\_net -net clkl\_mode7 -pin slow\_mode\_dly.cloc...
- > idm::object\_name \_\_CiType\_18\_305d60f8
- > led::connect\_net -net clkl\_mode7 -pin dcd\_succ\_disable\_s...
- > idm::object\_name \_\_CiType\_18\_305d6548
- > led::connect\_net -net clkl\_mode7 -pin drain\_blk.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d67b8
- > led::connect\_net -net clkl\_mode7 -pin dcd\_ilc.clockblock...
- > idm::object\_name \_\_CiType\_18\_305d6b18
- > led::connect\_net -net clkl\_mode7 -pin slow\_mode\_blk.cloc...
- > idm::object\_name \_\_CiType 18 305d6d88
- > led::connect\_net -net clkl\_mode7 -pin op\_cmp\_44.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d6ff8
- > led::connect\_net -net clkl\_mode7 -pin op\_cmp\_dsbl.clockb...
- > idm::object\_name \_\_CiType\_18\_305d7268
- > led::connect\_net -net clkl\_mode7 -pin eu\_frc\_milli.clock...
- > idm::object\_name \_\_CiType\_18\_305d74d8
- > led::connect\_net -net clkl\_mode7 -pin bcr\_store\_stat.clo...
- > idm::object\_name \_\_CiType\_18\_305d7748
- > led::connect\_net -net clkl\_mode7 -pin exc\_info.clockbloc...
- > idm::object\_name \_\_CiType\_18\_305d7c88
- > led::connect\_net -net clkl\_mode7 -pin spare.clockblock/c...
- > idm::object\_name \_\_CiType\_18\_305d7ef8
- > led::connect\_net -net clkl\_mode7 -pin mcset\_e1.clockbloc...
- > idm::object\_name \_\_CiType\_18\_305d8168
- > led::connect\_net -net clkl\_mode7 -pin eu\_iu\_spare.clockb...
- > idm::object\_name \_\_CiType\_18\_305d83d8
- > led::connect\_net -net clkl\_mode7 -pin dsbl\_ovrlp\_blk.clo...
- > idm::object\_name \_\_CiType\_18\_305d8648
- > led::connect\_net -net clkl\_mode7 -pin inst\_fetch.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d88b8
- > led::connect\_net -net clkl\_mode7 -pin iu\_dsbl\_ovrlp.cloc...
- > idm::object\_name \_\_CiType 18 305d8b28
- > |ed::connect\_net -net clkl\_mode7 -pin ex\_in\_prog.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d8d98
- > led::connect\_net -net clkl\_mode7 -pin blk\_dcd.clockblock...
- > idm::object\_name \_\_CiType\_18\_305d92d8
- > led::connect\_net -net clkl\_mode7 -pin dcd\_succ\_dly.clock...
- > idm::object\_name \_\_CiType\_18\_305d9548
- > led::connect\_net -net clkl\_mode7 -pin exec\_recov.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d97b8
- > led::connect\_net -net clkl\_mode7 -pin ru\_updt\_dly.clockb...
- > idm::object\_name \_\_CiType\_18\_305d9a28
- > led::connect\_net -net clkl\_mode7 -pin iu\_rst\_fst\_t1.cloc...
- > idm::object\_name \_\_CiType\_18\_305d9c98
- > led::connect\_net -net clkl\_mode7 -pin inst\_store.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d9f08
- > led::connect\_net -net clkl\_mode7 -pin eu\_dsbl\_aftr.clock...
- > idm::object\_name \_\_CiType\_18\_305da178
- > led::connect\_net -net clkl\_mode7 -pin dcdsuc\_err.clockbl...
- > idm::object\_name \_\_CiType\_18\_305da3e8
- > led::connect\_net -net clkl\_mode7 -pin dcd\_cyl\_cnt.clockb...
- > idm::object\_name \_\_CiType\_18\_305da748
- > led::connect\_net -net clkl\_mode7 -pin blk\_mcend.clockblo...
- > idm::object\_name \_\_CiType\_18\_305da9b8

```
> led::connect_net -net clkl_mode7 -pin op_44_info.clockbl...
         > idm::object_name __CiType_18_305dad18
         > led::connect_net -net clkl_mode7 -pin rcvry_reset.clockb...
         > idm::object_name __CiType_18_305daf88
         > led::connect_net -net clkl_mode7 -pin br_wrongs.clockblo...
         > idm::object_name __CiType_18_305db1f8
         > led::connect_net -net clkl_mode7 -pin rstrt_reset.clockb...
         > idm::object_name __CiType_18_305db468
         > led::connect_net -net clkl_mode7 -pin br_dcd_pend.clockb...
       > idm::filter -on gates -expr {[regexp cb_mode_block @def...
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/new_led.tcl
          > idm::locate_or_create_keyword_def -clas group -name PGRO...
          > idm::locate or create keyword def -clas group -name PGRO...
          > idm::locate_or_create_keyword_def -clas group -name PGRO...
          > idm::locate_or_create_keyword_def -clas group -name COMM...
          > idm::get active network
           > idm::locate net -proto box CiType_16_30a445c8 -name cl...
        > led::create_net -name clkl_mode4_0
         > idm::object_name __CiType_18_305b1a98
         > led::connect_net -net clkl_mode4_0 -pin gptr_latch/clkl_...
         > idm::object_name __CiType_18_305b89c8
         > led::connect_net -net clkl_mode4_0 -pin slow_mode.clockb...
         > idm::object_name __CiType_18_305b8c38
         > led::connect_net -net clkl_mode4_0 -pin ru_rq_blk.clockb...
         > idm::object_name __CiType_18_305b8ea8
         > led::connect_net -net clkl_mode4_0 -pin iu_rst_fst.clock...
         > idm::object_name __CiType_18_305d17d8
         > led::connect_net -net clkl_mode4_0 -pin iu_restart.clock...
         > idm::object_name __CiType_18_305d1a48
         > led::connect_net -net clkl_mode4_0 -pin ia_to_if.clockbl...
         > idm::object_name __CiType_18_305d1cb8
         > led::connect_net -net clkl_mode4_0 -pin frc_mmode.clockb...
         > idm::object_name __CiType_18_305d1f28
         > led::connect_net -net clkl_mode4_0 -pin local_milli.cloc...
         > idm::object_name __CiType_18_305d2198
         > led::connect_net -net clkl_mode4_0 -pin ia_to_if_t1.cloc...
         > idm::object_name __CiType_18_305d2408
         > led::connect_net -net clkl_mode4_0 -pin mia_to_if.clockb...
         > idm::object_name __CiType_18_305d2678
         > led::connect_net -net clkl_mode4_0 -pin slow_mode_t1.clo...
         > idm::object_name __CiType_18_305d28e8
```

- > led::connect\_net -net clkl\_mode4\_0 -pin iq\_empty\_dly.clo...
- > idm::object\_name \_\_CiType\_18\_305d2b58
- > led::connect\_net -net clkl\_mode4\_0 -pin slow\_mode\_t2.clo...
- > idm::object\_name \_\_CiType\_18\_305d2dc8
- > led::connect\_net -net clkl\_mode4\_0 -pin s390\_updt\_blk.cl...
- > idm::object\_name \_\_CiType\_18\_305d3038
- > led::connect\_net -net clkl\_mode4\_0 -pin srlz\_nomatch.clo...
- > idm::object\_name \_\_CiType\_18\_305d32a8
- > led::connect\_net -net clkl\_mode4\_0 -pin bce\_hold\_aa.cloc...
- > idm::object\_name \_\_CiType\_18\_305d3518
- > led::connect\_net -net clkl\_mode4\_0 -pin srlz\_actn.clockb...
- > idm::object name CiType 18 305d3878
- > led::connect\_net -net clkl\_mode4\_0 -pin op\_44\_dcd.clockb...
- > idm::object\_name \_\_CiType\_18\_305d3ae8

```
> led::connect_net -net clkl_mode4_0 -pin op_cmp_tr.clockb...
```

- > idm::object\_name \_\_CiType\_18\_305d3d58
- > led::connect\_net -net clkl\_mode4\_0 -pin num\_dcd.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d40b8
- > led::connect\_net -net clkl\_mode4\_0 -pin mia\_to\_if\_t1.clo...
- > idm::object\_name \_\_CiType\_18\_305d4328
- > led::connect\_net -net clkl\_mode4\_0 -pin eu\_op\_encode.clo...
- > idm::object\_name \_\_CiType\_18\_305d4fe8
- > led::connect\_net -net clkl\_mode4\_0 -pin frc\_blk\_1cyc.clo...
- > idm::object\_name \_\_CiType\_18\_305d5258
- > led::connect\_net -net clkl\_mode4\_0 -pin local\_milli\_t1.c...
- > idm::object\_name \_\_CiType\_18\_305d54c8
- > led::connect\_net -net clkl\_mode4\_0 -pin local\_milli\_t2.c...
- > idm::object\_name \_\_CiType\_18\_305d5738
- > led::connect\_net -net clkl\_mode4\_0 -pin bht\_block.clockb...
- > idm::object\_name \_\_CiType\_18\_305d59a8
- > led::connect\_net -net clkl\_mode4\_0 -pin srlz\_blk.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d5c18
- > led::connect\_net -net clkl\_mode4\_0 -pin exc\_cond.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d5e88
- > led::connect\_net -net clkl\_mode4\_0 -pin slow\_mode\_dly.cl...
- > idm::object\_name \_\_CiType\_18\_305d60f8
- > led::connect\_net -net clkl\_mode4\_0 -pin dcd\_succ\_disable...
- > idm::object\_name \_\_CiType\_18\_305d6548
- > led::connect\_net -net clkl\_mode4\_0 -pin drain\_blk.clockb...
- > idm::object\_name \_\_CiType\_18\_305d67b8
- > led::connect\_net -net clkl\_mode4\_0 -pin dcd\_ilc.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d6b18
- > led::connect\_net -net clkl\_mode4\_0 -pin slow\_mode\_blk.cl...
- > idm::object\_name \_\_CiType\_18\_305d6d88
- > led::connect\_net -net clkl\_mode4\_0 -pin op\_cmp\_44.clockb...
- > idm::object\_name \_\_CiType\_18 305d6ff8
- > led::connect\_net -net clkl\_mode4\_0 -pin op\_cmp\_dsbl.cloc...
- > idm::object\_name \_\_CiType\_18\_305d7268
- > led::connect\_net -net clkl\_mode4\_0 -pin eu\_frc\_milli.clo...
- > idm::object\_name \_\_CiType\_18\_305d74d8
- > led::connect\_net -net clkl\_mode4\_0 -pin bcr\_store\_stat.c...
- > idm::object\_name \_\_CiType\_18\_305d7748
- > led::connect\_net -net clkl\_mode4\_0 -pin exc\_info.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d7c88
- > led::connect\_net -net clkl\_mode4\_0 -pin spare.clockblock...
- > idm::object\_name \_\_CiType\_18\_305d7ef8
- > led::connect\_net -net clkl\_mode4\_0 -pin mcset\_e1.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d8168
- > led::connect\_net -net clkl\_mode4\_0 -pin eu\_iu\_spare.cloc...
- > idm::object\_name \_\_CiType\_18 305d83d8
- > led::connect\_net -net clkl\_mode4\_0 -pin dsbl\_ovrlp\_blk.c...
- > idm::object\_name \_\_CiType\_18\_305d8648
- > led::connect\_net -net clkl\_mode4\_0 -pin inst\_fetch.clock...
- > idm::object\_name \_\_CiType\_18\_305d88b8
- > led::connect\_net -net clkl\_mode4\_0 -pin iu\_dsbl\_ovrlp.cl...
- > idm::object\_name \_\_CiType\_18\_305d8b28
- > led::connect\_net -net clkl\_mode4\_0 -pin ex\_in\_prog.clock...
- > idm::object\_name \_\_CiType\_18\_305d8d98
- > led::connect\_net -net clkl\_mode4\_0 -pin blk\_dcd.clockblo...

```
> idm::object_name __CiType_18_305d92d8
```

- > led::connect\_net -net clkl\_mode4\_0 -pin dcd\_succ\_dly.clo...
- > idm::object\_name \_\_CiType\_18\_305d9548
- > led::connect\_net -net clkl\_mode4\_0 -pin exec\_recov.clock...
- > idm::object\_name \_\_CiType\_18\_305d97b8
- > led::connect\_net -net clkl\_mode4\_0 -pin ru\_updt\_dly.cloc...
- > idm::object\_name \_\_CiType\_18\_305d9a28
- > led::connect\_net -net clkl\_mode4\_0 -pin iu\_rst\_fst\_t1.cl...
- > idm::object\_name \_\_CiType\_18\_305d9c98
- > led::connect\_net -net clkl\_mode4\_0 -pin inst\_store.clock...
- > idm::object\_name \_\_CiType\_18\_305d9f08
- > led::connect\_net -net clkl\_mode4\_0 -pin eu\_dsbl\_aftr.clo...
- > idm::object\_name \_\_CiType\_18\_305da178
- > led::connect\_net -net clkl\_mode4\_0 -pin dcdsuc\_err.clock...
- > idm::object\_name \_\_CiType\_18\_305da3e8
- > led::connect\_net -net clkl\_mode4\_0 -pin dcd\_cyl\_cnt.cloc...
- > idm::object\_name \_\_CiType\_18\_305da748
- > led::connect\_net -net clkl\_mode4\_0 -pin blk\_mcend.clockb...
- > idm::object\_name \_\_\_CiType\_18\_305da9b8
- > led::connect\_net -net clkl\_mode4\_0 -pin op\_44\_info.clock...
- > idm::object\_name \_\_CiType\_18\_305dad18
- > led::connect\_net -net clkl\_mode4\_0 -pin rcvry\_reset.cloc...
- > idm::object\_name \_\_CiType\_18\_305daf88
- > led::connect\_net -net clkl\_mode4\_0 -pin br\_wrongs.clockb...
- > idm::object\_name \_\_CiType\_18\_305db1f8
- > led::connect\_net -net clkl\_mode4\_0 -pin rstrt\_reset.cloc...
- > idm::object\_name \_\_CiType\_18\_305db468
- > led::connect\_net -net clkl\_mode4\_0 -pin br\_dcd\_pend.cloc...
- > idm::get\_active\_network
  - > idm::locate\_net -proto\_box \_\_CiType\_16\_30a445c8 -name cl...
- > led::create\_net -name clkl\_mode5\_0
- > idm::object\_name \_\_CiType\_18\_305b1a98
- > led::connect\_net -net clkl\_mode5\_0 -pin gptr\_latch/clkl\_...
- > idm::object\_name \_\_\_CiType\_18\_305b89c8
- > led::connect\_net -net clkl\_mode5\_0 -pin slow\_mode.clockb...
- > idm::object\_name \_\_CiType\_18\_305b8c38
- > led::connect\_net -net clkl\_mode5\_0 -pin ru\_rq\_blk.clockb...
- > idm::object\_name \_\_CiType\_18\_305b8ea8
- > led::connect\_net -net clkl\_mode5\_0 -pin iu\_rst\_fst.clock...
- > idm::object\_name \_\_CiType\_18\_305d17d8
- > led::connect\_net -net clkl\_mode5\_0 -pin iu\_restart.clock...
- > idm::object\_name \_\_CiType\_18\_305d1a48
- > led::connect\_net -net clkl\_mode5\_0 -pin ia\_to\_if.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d1cb8
- > led::connect\_net -net clkl\_mode5\_0 -pin frc\_mmode.clockb...
- > idm::object\_name \_\_CiType\_18\_305d1f28
- > led::connect\_net -net clkl\_mode5\_0 -pin local\_milli.cloc...
- > idm::object\_name \_\_CiType\_18\_305d2198
- > led::connect\_net -net clkl\_mode5\_0 -pin ia\_to\_if\_t1.cloc...
- > idm::object\_name \_\_CiType\_18\_305d2408
- > led::connect\_net -net clkl\_mode5\_0 -pin mia\_to\_if.clockb...
- > idm::object\_name \_\_CiType\_18\_305d2678
- > led::connect\_net -net clkl\_mode5\_0 -pin slow\_mode\_t1.clo...
- > idm::object\_name \_\_CiType\_18\_305d28e8
- > led::connect\_net -net clkl\_mode5\_0 -pin iq\_empty\_dly.clo...

```
> idm::object_name __CiType_18_305d2b58
```

- > led::connect\_net -net clkl\_mode5\_0 -pin slow\_mode t2.clo...
- > idm::object\_name \_\_CiType\_18\_305d2dc8
- > led::connect\_net -net clkl\_mode5\_0 -pin s390\_updt\_blk.cl...
- > idm::object\_name \_\_CiType\_18\_305d3038
- > led::connect\_net -net clkl\_mode5\_0 -pin srlz\_nomatch.clo...
- > idm::object\_name \_\_CiType\_18\_305d32a8
- > led::connect\_net -net clkl\_mode5\_0 -pin bce\_hold\_aa.cloc...
- > idm::object\_name \_\_CiType\_18\_305d3518
- > led::connect\_net -net clkl\_mode5\_0 -pin srlz\_actn.clockb...
- > idm::object\_name \_\_CiType\_18 305d3878
- > led::connect\_net -net clkl\_mode5\_0 -pin op\_44\_dcd.clockb...
- > idm::object\_name \_\_CiType\_18\_305d3ae8
- > led::connect\_net -net clkl\_mode5\_0 -pin op\_cmp\_tr.clockb...
- > idm::object\_name \_\_CiType\_18\_305d3d58
- > led::connect\_net -net clkl\_mode5\_0 -pin num\_dcd.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d40b8
- > led::connect\_net -net clkl\_mode5\_0 -pin mia\_to\_if\_t1.clo...
- > idm::object\_name \_\_CiType\_18\_305d4328
- > led::connect\_net -net clkl\_mode5\_0 -pin eu\_op\_encode.clo...
- > idm::object\_name \_\_CiType\_18\_305d4fe8
- > led::connect\_net -net clkl\_mode5\_0 -pin frc\_blk\_1cyc.clo...
- > idm::object\_name \_\_CiType\_18\_305d5258
- > led::connect\_net -net clkl\_mode5\_0 -pin local\_milli\_t1.c...
- > idm::object\_name \_\_CiType\_18\_305d54c8
- > led::connect\_net -net clkl\_mode5\_0 -pin local\_milli\_t2.c...
- > idm::object\_name \_\_CiType\_18\_305d5738
- > led::connect\_net -net clkl\_mode5\_0 -pin bht\_block.clockb...
- > idm::object\_name \_\_CiType\_18\_305d59a8
- > led::connect\_net -net clkl\_mode5\_0 -pin srlz\_blk.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d5c18
- > led::connect\_net -net clkl\_mode5\_0 -pin exc\_cond.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d5e88
- > led::connect\_net -net clkl\_mode5\_0 -pin slow\_mode\_dly.cl...
- > idm::object\_name \_\_CiType\_18\_305d60f8
- > led::connect\_net -net clkl\_mode5\_0 -pin dcd\_succ\_disable...
- > idm::object\_name \_\_CiType\_18\_305d6548
- > led::connect\_net -net clkl\_mode5\_0 -pin drain\_blk.clockb...
- > idm::object\_name \_\_CiType\_18\_305d67b8
- > led::connect\_net -net clkl\_mode5\_0 -pin dcd\_ilc.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d6b18
- > led::connect\_net -net clkl\_mode5\_0 -pin slow\_mode\_blk.cl...
- > idm::object\_name \_\_CiType\_18\_305d6d88
- > led::connect\_net -net clkl\_mode5\_0 -pin op\_cmp\_44.clockb....
- > idm::object\_name \_\_CiType\_18\_305d6ff8
- > led::connect\_net -net clkl\_mode5\_0 -pin op\_cmp\_dsbl.cloc...
- > idm::object\_name \_\_CiType\_18\_305d7268
- > led::connect\_net -net clkl\_mode5\_0 -pin eu\_frc\_milli.clo...
- > idm::object\_name \_\_CiType\_18\_305d74d8
- > led::connect\_net -net clkl\_mode5\_0 -pin bcr\_store\_stat.c...
- > idm::object\_name \_\_CiType\_18\_305d7748
- > led::connect\_net -net clkl\_mode5\_0 -pin exc\_info.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d7c88
- > led::connect\_net -net clkl\_mode5\_0 -pin spare.clockblock...
- > idm::object\_name \_\_CiType\_18\_305d7ef8

```
> led::connect_net -net clkl_mode5_0 -pin mcset_e1.clockbl...
```

- > idm::object\_name \_\_CiType\_18\_305d8168
- > led::connect\_net -net clkl\_mode5\_0 -pin eu\_iu\_spare.cloc...
- > idm::object\_name \_\_CiType\_18\_305d83d8
- > led::connect\_net -net clkl\_mode5\_0 -pin dsbl\_ovrlp\_blk.c...
- > idm::object\_name \_\_CiType\_18\_305d8648
- > led::connect\_net -net clkl\_mode5\_0 -pin inst\_fetch.clock...
- > idm::object\_name \_\_CiType\_18\_305d88b8
- > led::connect\_net -net clkl\_mode5\_0 -pin iu\_dsbl\_ovrlp.cl...
- > idm::object\_name \_\_CiType\_18\_305d8b28
- > led::connect\_net -net clkl\_mode5\_0 -pin ex\_in\_prog.clock...
- > idm::object\_name \_\_CiType\_18\_305d8d98
- > led::connect\_net -net clkl\_mode5\_0 -pin blk\_dcd.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d92d8
- > led::connect\_net -net clkl\_mode5\_0 -pin dcd\_succ\_dly.clo...
- > idm::object\_name \_\_CiType\_18\_305d9548
- > led::connect\_net -net clkl\_mode5\_0 -pin exec\_recov.clock...
- > idm::object\_name \_\_CiType\_18\_305d97b8
- > led::connect\_net -net clkl\_mode5\_0 -pin ru\_updt\_dly.cloc...
- > idm::object\_name \_\_CiType\_18\_305d9a28
- > led::connect\_net -net clkl\_mode5\_0 -pin iu\_rst\_fst\_t1.cl...
- > idm::object\_name \_\_CiType\_18\_305d9c98
- > led::connect\_net -net clkl\_mode5\_0 -pin inst\_store.clock...
- > idm::object\_name \_\_CiType\_18\_305d9f08
- > led::connect\_net -net clkl\_mode5\_0 -pin eu\_dsbl\_aftr.clo...
- > idm::object\_name \_\_CiType\_18\_305da178
- > led::connect\_net -net clkl\_mode5\_0 -pin dcdsuc\_err.clock...
- > idm::object\_name \_\_CiType\_18\_305da3e8
- > led::connect\_net -net clkl\_mode5\_0 -pin dcd\_cyl\_cnt.cloc...
- > idm::object\_name \_\_CiType\_18\_305da748
- > led::connect\_net -net clkl\_mode5\_0 -pin blk\_mcend.clockb...
- > idm::object\_name \_\_CiType\_18\_305da9b8
- > led::connect\_net -net clkl\_mode5\_0 -pin op\_44\_info.clock...
- > idm::object\_name \_\_CiType\_18\_305dad18
- > led::connect\_net -net clkl\_mode5\_0 -pin rcvry\_reset.cloc...
- > idm::object\_name \_\_CiType\_18\_305daf88
- > led::connect\_net -net clkl\_mode5\_0 -pin br\_wrongs.clockb...
- > idm::object\_name \_\_CiType\_18\_305db1f8
- > led::connect\_net -net clkl\_mode5\_0 -pin rstrt\_reset.cloc...
- > idm::object\_name \_\_CiType\_18\_305db468
- > led::connect\_net -net clkl\_mode5\_0 -pin br\_dcd\_pend.cloc...
- > idm::get\_active\_network
- > idm::locate\_net -proto\_box \_\_CiType\_16\_30a445c8 -name cl...
- > led::create\_net -name clkl\_mode6\_0
- > idm::object\_name \_\_CiType\_18\_305b1a98
- > led::connect\_net -net clkl\_mode6\_0 -pin gptr\_latch/clkl\_...
- > idm::object\_name \_\_CiType\_18\_305b89c8
- > led::connect\_net -net clkl\_mode6\_0 -pin slow\_mode.clockb...
- > idm::object\_name \_\_CiType\_18\_305b8c38
- > led::connect\_net -net clkl\_mode6\_0 -pin ru\_rq\_blk.clockb...
- > idm::object\_name \_\_CiType\_18\_305b8ea8
- > led::connect\_net -net clkl\_mode6\_0 -pin iu\_rst\_fst.clock...
- > idm::object\_name \_\_CiType\_18\_305d17d8
- > led::connect\_net -net clkl\_mode6\_0 -pin iu\_restart.clock...
- > idm::object\_name \_\_CiType\_18\_305d1a48

```
> led::connect_net -net clkl_mode6_0 -pin ia_to_if.clockbl...
```

- > idm::object\_name \_\_CiType\_18\_305d1cb8
- > led::connect\_net -net clkl\_mode6\_0 -pin frc\_mmode.clockb...
- > idm::object\_name \_\_CiType\_18\_305d1f28
- > led::connect\_net -net clkl\_mode6\_0 -pin local\_milli.cloc...
- > idm::object\_name \_\_CiType\_18\_305d2198
- > led::connect\_net -net clkl\_mode6\_0 -pin ia\_to\_if\_t1.cloc...
- > idm::object\_name \_\_CiType\_18\_305d2408
- > led::connect\_net -net clkl\_mode6\_0 -pin mia\_to\_if.clockb...
- > idm::object\_name \_\_CiType\_18\_305d2678
- > led::connect\_net -net clkl\_mode6\_0 -pin slow\_mode\_t1.clo...
- > idm::object\_name \_\_CiType\_18\_305d28e8
- > led::connect\_net -net clkl\_mode6\_0 -pin iq\_empty\_dly.clo...
- > idm::object\_name \_\_CiType\_18\_305d2b58
- > led::connect\_net -net clkl\_mode6\_0 -pin slow\_mode\_t2.clo...
- > idm::object\_name \_\_CiType\_18\_305d2dc8
- > led::connect\_net -net clkl\_mode6\_0 -pin s390\_updt\_blk.cl...
- > idm::object\_name \_\_CiType\_18\_305d3038
- > led::connect\_net -net clkl\_mode6\_0 -pin srlz\_nomatch.clo...
- > idm::object\_name \_\_CiType\_18\_305d32a8
- > led::connect\_net -net clkl\_mode6\_0 -pin bce\_hold\_aa.cloc...
- > idm::object\_name \_\_CiType\_18\_305d3518
- > led::connect\_net -net clkl\_mode6\_0 -pin srlz\_actn.clockb...
- > idm::object\_name \_\_CiType\_18\_305d3878
- > led::connect\_net -net clkl\_mode6\_0 -pin op\_44\_dcd.clockb...
- > idm::object\_name \_\_CiType 18 305d3ae8
- > led::connect\_net -net clkl\_mode6\_0 -pin op\_cmp\_tr.clockb...
- > idm::object\_name \_\_CiType\_18\_305d3d58
- > led::connect\_net -net clkl\_mode6\_0 -pin num\_dcd.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d40b8
- > led::connect\_net -net clkl\_mode6\_0 -pin mia\_to\_if\_t1.clo...
- > idm::object\_name \_\_CiType\_18\_305d4328
- > led::connect\_net -net clkl\_mode6\_0 -pin eu\_op encode.clo...
- > idm::object\_name \_\_CiType\_18\_305d4fe8
- > led::connect\_net -net clkl\_mode6\_0 -pin frc\_blk\_1cyc.clo...
- > idm::object\_name \_\_CiType\_18\_305d5258
- > led::connect\_net -net clkl\_mode6\_0 -pin local\_milli\_t1.c...
- > idm::object\_name \_\_CiType 18 305d54c8
- > led::connect\_net -net clkl\_mode6\_0 -pin local\_milli\_t2.c...
- > idm::object\_name \_\_CiType\_18\_305d5738
- > led::connect\_net -net clkl\_mode6\_0 -pin bht\_block.clockb...
- > idm::object\_name \_\_CiType\_18\_305d59a8
- > led::connect\_net -net clkl\_mode6\_0 -pin srlz\_blk.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d5c18
- > led::connect\_net -net clkl\_mode6\_0 -pin exc\_cond.clockbl...
- > idm::object\_name \_\_CiType 18 305d5e88
- > led::connect\_net -net clkl\_mode6\_0 -pin slow\_mode\_dly.cl...
- > idm::object\_name \_\_CiType\_18\_305d60f8
- > led::connect\_net -net clkl\_mode6\_0 -pin dcd\_succ\_disable...
- > idm::object\_name \_\_CiType\_18\_305d6548
- > led::connect\_net -net clkl\_mode6\_0 -pin drain\_blk.clockb...
- > idm::object\_name \_\_CiType\_18\_305d67b8
- > led::connect\_net -net clkl\_mode6\_0 -pin dcd\_ilc.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d6b18
- > led::connect\_net -net clkl\_mode6\_0 -pin slow\_mode\_blk.cl...

- > idm::object\_name \_\_CiType\_18\_305d6d88
- > led::connect\_net -net clkl\_mode6\_0 -pin op\_cmp\_44.clockb...
- > idm::object\_name \_\_CiType\_18\_305d6ff8
- > led::connect\_net -net clkl\_mode6\_0 -pin op\_cmp\_dsbl.cloc...
- > idm::object\_name \_\_CiType\_18\_305d7268
- > led::connect\_net -net clkl\_mode6\_0 -pin eu\_frc\_milli.clo...
- > idm::object\_name \_\_CiType\_18\_305d74d8
- > led::connect\_net -net clkl\_mode6\_0 -pin bcr\_store\_stat.c...
- > idm::object\_name \_\_CiType\_18\_305d7748
- > led::connect\_net -net clkl\_mode6\_0 -pin exc\_info.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d7c88
- > led::connect\_net -net clkl\_mode6\_0 -pin spare.clockblock...
- > idm::object\_name \_\_CiType\_18\_305d7ef8
- > led::connect\_net -net clkl\_mode6\_0 -pin mcset\_e1.clockbl...
- > idm::object\_name \_\_CiType\_18\_305d8168
- > led::connect\_net -net clkl\_mode6\_0 -pin eu\_iu\_spare.cloc...
- > idm::object\_name \_\_CiType\_18\_305d83d8
- > led::connect\_net -net clkl\_mode6\_0 -pin dsbl\_ovrlp\_blk.c...
- > idm::object\_name \_\_CiType\_18\_305d8648
- > led::connect\_net -net clkl\_mode6\_0 -pin inst\_fetch.clock...
- > idm::object\_name \_\_CiType\_18\_305d88b8
- > led::connect\_net -net clkl\_mode6\_0 -pin iu\_dsbl\_ovrlp.cl...
- > idm::object\_name \_\_CiType\_18\_305d8b28
- > led::connect\_net -net clkl\_mode6\_0 -pin ex\_in\_prog.clock...
- > idm::object\_name \_\_CiType\_18\_305d8d98
- > led::connect\_net -net clkl\_mode6\_0 -pin blk\_dcd.clockblo...
- > idm::object\_name \_\_CiType\_18\_305d92d8
- > led::connect\_net -net clkl\_mode6\_0 -pin dcd\_succ\_dly.clo...
- > idm::object\_name \_\_CiType\_18\_305d9548
- > led::connect\_net -net clkl\_mode6\_0 -pin exec\_recov.clock...
- > idm::object\_name \_\_CiType\_18\_305d97b8
- > led::connect\_net -net clkl\_mode6\_0 -pin ru\_updt\_dly.cloc...
- > idm::object\_name \_\_CiType\_18\_305d9a28
- > led::connect\_net -net clkl\_mode6\_0 -pin iu\_rst\_fst\_t1.cl...
- > idm::object\_name \_\_CiType\_18\_305d9c98
- > led::connect\_net -net clkl\_mode6\_0 -pin inst\_store.clock...
- > idm::object\_name \_\_CiType\_18\_305d9f08
- > led::connect\_net -net clkl\_mode6\_0 -pin eu\_dsbl\_aftr.clo...
- > idm::object\_name \_\_CiType\_18\_305da178
- > led::connect\_net -net clkl\_mode6\_0 -pin dcdsuc\_err.clock...
- > idm::object\_name \_\_CiType\_18\_305da3e8
- > led::connect\_net -net clkl\_mode6\_0 -pin dcd\_cyl\_cnt.cloc...
- > idm::object\_name \_\_CiType\_18\_305da748
- > led::connect\_net -net clkl\_mode6\_0 -pin blk\_mcend.clockb...
- > idm::object\_name \_\_CiType\_18\_305da9b8
- > led::connect\_net -net clkl\_mode6\_0 -pin op\_44\_info.clock...
- > idm::object\_name \_\_CiType\_18\_305dad18
- > led::connect\_net -net clkl\_mode6\_0 -pin rcvry\_reset.cloc...
- > idm::object\_name \_\_CiType\_18\_305daf88
- > led::connect\_net -net clkl\_mode6\_0 -pin br\_wrongs.clockb...
- > led::connect\_net -net clkl\_mode6\_0 -pin rstrt\_reset.cloc...
- > idm::object\_name \_\_CiType\_18\_305db468
- > led::connect\_net -net clkl\_mode6\_0 -pin br\_dcd\_pend.cloc...
- > CTE::cte\_lcb\_drv {MERGE\_BOOKS TRUE}

```
[cte_lcb_drv]: (W) Internal error: Row 1 for XRFCBA has errors
[cte_lcb_drv]: (W) Internal error : Row 2 for cb_clk_32_1 has errors
[cte_lcb_drv]: (W) Internal error : Row 4 for cb_mode_block has errors
[cte_lcb_drv]: Merging books by DRV input nets due to MERGE_BOOKS setting.
[cte_lcb_drv]: Merging of LCB/DRV books only based on input pins matching exactly.
Index
                Usage box name
                                             Def box name inputs
[cte_lcb_drv]: Merging books by LCB input nets due to MERGE_BOOKS setting.
[cte_lcb_drv]: Merging of LCB/DRV books only based on input pins matching exactly.
[cte_lcb_drv]: Transferred ru_rq_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ru_rq_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ru_rq_blk.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_rst_fst.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_rst_fst.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_rst_fst.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_restart.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_restart.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_restart.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred ia_to_if.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ia_to_if.reg_n.lat_0 pin c2 to slow mode.clockblock
[cte_lcb_drv]: Transferred ia_to_if.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred frc_mmode.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred frc_mmode.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred frc_mmode.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred ia_to_if_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ia_to_if_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ia_to_if_t1.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred mia_to_if.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred mia_to_if.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred mia_to_if.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_t1.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred iq_empty_dly.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iq_empty_dly.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iq_empty_dly.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_t2.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_t2.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_t2.reg_n.lat_0 pin clka to slow_mode.clockblock
rcte_lcb_drv]: Transferred s390_updt_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred s390_updt_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred s390_updt_blk.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_nomatch.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_nomatch.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_nomatch.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred bce_hold_aa.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred bce_hold_aa.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred bce_hold_aa.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_actn.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_actn.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_actn.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_actn.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_actn.reg_n.lat_0 pin clka to slow_mode.clockblock
```

```
[cte_lcb_drv]: Transferred srlz_actn.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_dcd.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_dry]: Transferred op 44 dcd.req_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_dcd.reg_n.lat_0 pin clka to slow_mode.clockblock
Icte lcb dryl: Transferred op cmp tr.reg n.lat 0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_tr.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_tr.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred num_dcd.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred num_dcd.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred num_dcd.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred num_dcd.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred num_dcd.reg_n.lat_0 pin clka to slow_mode.clockblock
Icte lcb dryl: Transferred num dcd.reg n.lat 1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred mia_to_if_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred mia_to_if_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_dryl: Transferred mia_to_if_t1.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte |cb |drv]: Transferred eu op encode.reg n.lat 2 pin c1 to slow mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_3 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_4 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_5 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_6 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_7 pin c1 to slow_mode.clockblock
[cte |cb drv]: Transferred eu op encode.reg_n.lat_8 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_9 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_10 pin c1 to slow_mode.clockblock
Icte Icb dryl: Transferred eu op encode.reg n.lat 11 pin c1 to slow_mode.clockblock
[cte | cb | drv]: Transferred eu_op_encode.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_2 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_3 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_4 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_5 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_6 pin c2 to slow_mode.clockblock
[cte lcb drv]: Transferred eu op encode.reg_n.lat_7 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_8 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_9 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_10 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_11 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_dry]: Transferred eu_op_encode.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_dry]: Transferred eu_op_encode.reg_n.lat_2 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_3 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred_eu_op_encode.reg_n.lat_4 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_5 pin clka to slow_mode.clockblock
Icte_lcb_drv1: Transferred eu_op_encode.reg_n.lat_6 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_7 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_8 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_9 pin clka to slow_mode.clockblock
[cte lcb drv]: Transferred eu op_encode.reg_n.lat_10 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_op_encode.reg_n.lat_11 pin clka to slow_mode.clockblock
[cte lcb drv]: Transferred frc blk 1cyc.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred frc_blk_1cyc.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred frc_blk_1cyc.reg_n.lat_0 pin clka to slow_mode.clockblock
```

```
[cte_lcb_drv]: Transferred local_milli_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli_t1.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli_t2.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli_t2.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred local_milli_t2.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred bht_block.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred bht_block.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred bht_block.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred srlz_blk.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_cond.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_cond.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_cond.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_dly.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_dly.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_dly.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_2 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_2 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_0 pin clka to slow mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_disable_scan.reg_n.lat_2 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred drain_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred drain_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred drain_blk.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_ilc.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_ilc.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_ilc.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_ilc.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_ilc.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_ilc.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred slow_mode_blk.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_44.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_44.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_44.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_dsbl.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_dsbl.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_cmp_dsbl.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_frc_milli.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_frc_milli.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_frc_milli.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred bcr_store_stat.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred bcr_store_stat.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred bcr_store_stat.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_2 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_3 pin c1 to slow_mode.clockblock
```

```
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_2 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_3 pin c2 to slow_mode.clockblock
Icte lcb dryl: Transferred exc info.reg n.lat 0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_2 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred exc_info.reg_n.lat_3 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred spare.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred spare.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred spare.reg_n.lat_0 pin clka to slow_mode.clockblock
Icte Icb dryl: Transferred mcset e1.reg n.lat 0 pin c1 to slow_mode.clockblock
cte lcb dryl: Transferred mcset e1.reg n.lat 0 pin c2 to slow mode.clockblock
[cte |cb drv]: Transferred mcset e1.reg n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_iu_spare.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_iu_spare.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_iu_spare.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dsbl_ovrlp_blk.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dsbl_ovrlp_blk.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dsbl_ovrlp_blk.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred inst_fetch.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred inst_fetch.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred inst_fetch.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_dsbl_ovrlp.reg_n.lat_0 pin c1 to slow_mode.clockblock
Icte Icb dryl: Transferred iu dsbl ovrlp.reg n.lat 0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_dsbl_ovrlp.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred ex_in_prog.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ex_in_prog.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ex_in_prog.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte lcb drv]: Transferred blk_dcd.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_2 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_3 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]; Transferred blk_dcd.reg_n.lat_2 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_3 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte |cb drv]: Transferred blk dcd.reg n.lat 1 pin clka to slow_mode.clockblock
[cte lcb drv]: Transferred blk dcd.reg n.lat 2 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_dcd.reg_n.lat_3 pin clka to slow_mode.clockblock
[cte_lcb_dry]: Transferred dcd_succ_dly.req_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_dly.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_succ_dly.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred exec_recov.req_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exec_recov.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred exec_recov.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred ru_updt_dly.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ru_updt_dly.req_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred ru_updt_dly.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_rst_fst_t1.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_rst_fst_t1.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred iu_rst_fst_t1.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred inst_store.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred inst_store.reg_n.lat_0 pin c2 to slow_mode.clockblock
```

```
[cte_lcb_drv]: Transferred inst_store.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_dsbl_aftr.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_dsbl_aftr.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred eu_dsbl_aftr.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcdsuc_err.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcdsuc_err.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcdsuc_err.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred dcd_cyl_cnt.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_mcend.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_mcend.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred blk_mcend.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_1 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_1 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred op_44_info.reg_n.lat_1 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred rcvry_reset.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rcvry_reset.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rcvry_reset.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_wrongs.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_wrongs.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_wrongs.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred rstrt_reset.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rstrt_reset.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred rstrt_reset.reg_n.lat_0 pin clka to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_dcd_pend.reg_n.lat_0 pin c1 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_dcd_pend.reg_n.lat_0 pin c2 to slow_mode.clockblock
[cte_lcb_drv]: Transferred br_dcd_pend.reg_n.lat_0 pin clka to slow_mode.clockblock
Index
                Usage box name
                                            Def box name inputs
          slow_mode.clockblock
                                               XRFCBA
[cte_lcb_drv]: Found 1 LCBs and created 5 new LCBs
[cte_lcb_drv]: Found 1 DRVs and created 0 new DRVs
       > idm::filter -on gates -expr {[regexp XRFCBA @def_name ]}
        > idm::object_name __CiType_18_305b89c8
[cte_fixmodeblock.tcl]: slow_mode.clockblock
        > idm::object_name __CiType_18_305b89c8
        > rebind -gates slow_mode.clockblock -new_cell cb_clk_32_1...
        > idm::object_name __CiType_18_305db468
[cte_fixmodeblock.tcl]: slow_mode.clockblock_1
        > idm::object_name __CiType_18_305db468
        > rebind -gates slow_mode.clockblock_1 -new_cell cb_clk_32...
        > idm::object_name __CiType_18_305db1f8
[cte_fixmodeblock.tcl]: slow_mode.clockblock_2
        > idm::object_name __CiType_18_305db1f8
        > rebind -gates slow_mode.clockblock_2 -new_cell cb_clk_32...
        > idm::object_name __CiType_18_305daf88
[cte_fixmodeblock.tcl]: slow_mode.clockblock_3
        > idm::object_name __CiType_18_305daf88
        > rebind -gates slow_mode.clockblock_3 -new_cell cb_clk_32...
```

```
> idm::object_name __CiType_18_305dad18
[cte_fixmodeblock.tcl]: slow_mode.clockblock_4
```

- > idm::object\_name \_\_CiType\_18\_305dad18
- > rebind -gates slow\_mode.clockblock\_4 -new\_cell cb\_clk\_32...
- > idm::object\_name \_\_CiType\_18\_305da9b8

[cte\_fixmodeblock.tcl]: slow\_mode.clockblock\_5

- > idm::object\_name \_\_CiType\_18\_305da9b8
- > rebind -gates slow\_mode.clockblock\_5 -new\_cell cb\_clk\_32...
- > cleanse
- > padnet

[[padnet]]: (W) Feed-thru or mult-PO net dcd\_succ\_last\_t1 has been renamed to dcd\_succ\_last\_t1&0 at proto pin dcd\_succ\_last\_t1 because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net dcd\_success\_tr has been renamed to dcd\_success\_tr&0 at proto pin dcd\_success\_tr because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net dcd\_succ\_first\_t1 has been renamed to dcd\_succ\_first\_t1&0 at proto pin dcd\_succ\_first\_t1 because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_milli\_mode\_t1 has been renamed to iu\_milli\_mode\_t1&0 at proto pin iu\_milli\_mode\_t1 because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_milli\_mode\_t2 has been renamed to iu\_milli\_mode\_t2&0 at proto pin iu\_milli\_mode\_t2 because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_exc\_cond has been renamed to iu\_exc\_cond&0 at proto pin iu\_exc\_cond because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_intrupt\_info(0) has been renamed to iu\_intrupt\_info&0(0) at proto pin iu\_intrupt\_info(0) because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_intrupt\_info(1) has been renamed to iu\_intrupt\_info&0(1) at proto pin iu\_intrupt\_info(1) because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_intrupt\_info(2) has been renamed to iu\_intrupt\_info&0(2) at proto pin iu\_intrupt\_info(2) because itconnects to multiple proto pins.

[[padnet]]: (W) Feed-thru or mult-PO net iu\_intrupt\_info(3) has been renamed to iu\_intrupt\_info&0(3) at proto pin iu\_intrupt\_info(3) because itconnects to multiple proto pins.

> summary\_report

## The model <IDCDSUC> has:

122 **Primary Inputs Primary Outputs** 73 Primary BIDIs 0 Signals 1033 Gate Count 810 = 1757 Connections Master REG Bits 83 Slave REG Bits 83 Internal Area 550 External Area 0 Gates/Connects 0.461013 **Fanout Count** 1757 Average Fanout 1.700871 Avg Tech Box Size = 0.679012 Tech Box Size Stddev = 0.008999 0.000000 Power

# \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\*

Real signals = 659
Real boxes = 435
Real connections = 1382
Real LSTs = 2041

```
Real ICells/box
                        1.264368
 Real LSTs/box
                         4.691954
 Real nets/box
                =
                        1.514943
 Cell
              Total
 Each
               Cell
Type Cnt Boxname
                             Power Level Function
                                                 Int Ext Power Int Ext Power
 164
       AND
                                     AND
                                            0
                                                0
                                                   0.000
                                                           0
                               >
                                                               0.000
 180
       BRKPT
                                     BRKPT
                                              0
                                                   0.000
                                 >
                                                                 0.000
 195
       IOPAD
                                     IOPAD
                                                  0
                                                                0.000
                                             0
                                                    0.000
                                                            0
 62
      NAND
                                     NAND
                                             0
                                                 0
                                                    0.000
                                                            0
                                                                0.000
 23
      NOR
                                    NOR
                                            0
                                                0.000
                                                           0
                                                               0.000
 91
      OR
                                    OR
                                          0
                                              0
                                                 0.000
                                                         0
                                                             0.000
 83
      XDLATCORE
                                         REG
                                                0
                                                    0.000
                                                             0
                                                                   0.000
  1
      cb_mode block
                                   > SEQUENTIAL
                                                   70
                                                        0.000
                                                                  70
  6
      cb_clk_32_1
                                 > SEQUENTIAL
                                                 80 0 0.000 480
                                                                      0.000
  5
      XOR
                                    XOR
                                           0
                                               0.000
                                                         0
                                                              0.000
[End of measure]
[measure]: Execution time was 0.0 seconds.
    > hidetech HIDE(BLACKBOX)
    > summary_report
The model <IDCDSUC> has:
Primary Inputs
                           122
 Primary Outputs
                            73
 Primary BIDIs
                           0
 Signals
                        1033
Gate Count
                          810
Connections
                          1757
Master REG Bits
                            83
Slave REG Bits
                            83
Internal Area
                          550
External Area
                           0
Gates/Connects
                         0.461013
Fanout Count
                          1757
Average Fanout
                         1.700871
Avg Tech Box Size =
                          0.679012
Tech Box Size Stddev =
                           0.008999
Power
              =
                      0.000000
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
Real signals
               =
                          659
Real boxes
                          435
Real connections
                           1382
Real LSTs
                         2041
Real ICells/box
                        1.264368
Real LSTs/box
                        4.691954
Real nets/box
                        1.514943
Cell
             Total
Each
              Cell
Type Cnt Boxname
                             Power Level Function
                                                  Int Ext Power Int Ext Power
-----
164
      AND
                                    AND
                                           0
                                               0
                                                 0.000
                                                          0
                                                              0.000
180
      BRKPT
                                    BRKPT
                                              0
                                                  0.000
                                                             0
                                                                0.000
```

```
195
        IOPAD
                                          IOPAD
                                                    0
                                                         0.000
                                                                     0
                                                                          0.000
                                          NAND
                                                   0
                                                        0.000
                                                                    0
                                                                             0.000
       NAND
                                                                         0
 62
                                                          0.000
                                                                   0
                                                                        0
                                                                           0.000
       NOR
                                          NOR
 23
                                                     0.000
                                                                      0.000
                                         OR
                                                0
                                                                 0
       OR
 91
                                                           0.000
                                                                            0.000
                                              REG
                                                                        0
 83
       XDLATCORE
                                                      0
                                        > SEQUENTIAL
                                                          70
                                                                0.000
                                                                            70
                                                                                  0.000
       cb_mode_block
  1
                                     > SEQUENTIAL
                                                        80
                                                              0
                                                                 0.000 480
                                                                                0.000
  6
       cb_clk_32_1
                                                                       0.000
       XOR
                                         XOR
                                                 0
                                                     0.000
                                                                  0
  5
[End of measure]
[measure]: Execution time was 0.0 seconds.
   > source ap unmap rea.tcl
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/gp_unmap_reg.tcl
    > observe -none
[gp_unmap_reg.tcl]: Unmapping all gates bound to: cmsff_sc_a
[gp_unmap_reg.tcl]: Unmapping all gates bound to: cns_msff_a
[gp_unmap_reg.tcl]: Unmapping all gates bound to: csl_scan_a
[gp_unmap_reg.tcl]: Unmapping all gates bound to: csl_ns_a
[gp_unmap_reg.tcl]: Unmapping all gates bound to: cls_msc_a
[gp_unmap_reg.tcl]: Unmapping all gates bound to: cs_cns_msffa
[gp_unmap_reg.tcl]: Unmapping all gates bound to: CMSFF_SC_A
[gp_unmap_reg.tcl]: Unmapping all gates bound to: CNS_MSFF_A
[gp_unmap_reg.tcl]: Unmapping all gates bound to: CSL_SCAN_A
[gp_unmap_reg.tcl]: Unmapping all gates bound to: CSL_NS_A
[gp_unmap_reg.tcl]: Unmapping all gates bound to: CSL_MSC_A
[gp_unmap_reg.tcl]: Unmapping all gates bound to: CS_CNS_MSFFA
[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLLAT6S
[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLDLATS
[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLLAT2S
[gp_unmap_reg.tcl]: Unmapping all gates bound to: VHDLLAT5S
[gp_unmap_reg.tcl]: Unmapping all gates bound to: XDLATR
[gp_unmap_reg.tcl]: Unmapping all gates bound to: XDLATCORE
[gp_unmap_reg.tcl]: Unmapping all gates bound to: XSCANCORE
    > nextbox xpndregs
[multiclk]: Release 1.0 Compiled on Feb 17 1999 at 16:37:02.
[multiclk]: There are 2 clock pins and 6 clock blocks
   > cleanse
  > check model report
[BD-40132]: Network IDCDSUC has no potential problems.
[ctesynz_cp.tcl]: SEARCH auto_path set to . ./tcl ./dll /afs/apd.pok.ibm.com/u/laceyl/tcl
/afs/apd.pok.ibm.com/u/laceyl/dll /afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/tcl
/afs/watson/projects/vlsi/cte/tools/bd2/0401v2/cte/2.0/dll /afs/watson/projects/vlsi/cte/tools/synzilla/1.0/tcl
/afs/watson/projects/vlsi/cte/tools/synzilla/1.0/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/tcl
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/dft
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/.
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/wizard/3.1/dll
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.
```

```
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/einstimer/3.1/.dll-rs_aix41/.
/afs/eda/project/EinsTimer/0301.stage/modules/einstimer/3.1/dll
/afs/eda.fishkill.ibm.com/prod/einstimer/3.1/dll
 ***** start Synzilla *****
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/write_synz.tcl
     > use cds
The Constant Delay Synthesis Engine is under development and should
be considered experimental.
      > use_cds
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/hnl.dll
hnl.dll version 1.0 (Apr 14 1999 18:12:01)
HNL Banner
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/synzext.dll
synzext.dll version 1.1 (Apr 14 1999 17:23:02)
Synzilla Extension
       > write_top -dir /data/laceyl/synztmp/IDCDSUC -root IDCDSUC
bdz> export_envs 1
       > write_vim_as_hnl -file /data/laceyl/synztmp/IDCDSUC/IDCD...
bdz> synzprep
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/synzprep.tcl
           > expand -view HISVHDL -hierarchy -hide
bdz> post_expand
             > sweep
             > delbrkpt BREAKLOOPS
             > brkloops
             > nextnet {delkey( EDIFNAME )}
             > nextbox {delkey( EDIFNAME )}
                  > set_nochange
                  > rtolbox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
                  > ltorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
                  > sweep
                > nochange
             > nextbox_with_test test_key(IOPAD_LOCATION,2),resolve_net...
             > nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
             > sweep
             > nextbox merge_dots()
             > nextbox dot2ms()
             > nextnet {ms2dot( BUS )}
          > good names
Good names for IDCDSUC
                                                     Count
                                                                User
                                                                         Like
                                                                                   New
For all nets
                               1033
                                        66.12%
                                                   13.84%
                                                              20.04%
For register output nets
                             166
                                   100.00%
                                                0.00%
                                                          0.00%
For break point input nets
                              180
                                    100.00%
                                                 0.00%
                                                           0.00%
For model input/output nets
                               195
                                      94.87%
                                                 5.13%
                                                            0.00%
                                                      Count
                                                                  User
                                                                            Like
                                                                                     New
For all boxes
                                810
                                       53.58%
                                                   0.00%
                                                            46.42%
For register boxes
                                83
                                      100.00%
                                                   0.00%
                                                             0.00%
          > view_name_is VHDL1076
          > view_name_is HIAVIEW
          > view_name_is HISVHDL
             > proto_get_int HIS_BD_VIM_SYNC,0
```

- > proto\_get\_int HISPREPSCN,0
- > view\_name\_is BSN
- > good\_names

#### Good names for IDCDSUC

			Cou	nt User	Like	New
For all nets	103	3 66.12%	13.84%	20.04%		
For register output nets	166	100.00%	0.00%	0.00%		
For break point input nets	180	100.00%	0.00%	0.00%		
For model input/output nets	195	94.87%	5.13%	0.00%		

Count User Like New For all boxes 810 53.58% 0.00% 46.42%

For register boxes 81 100.00% 0.00% 40.42%

- > copyinfo
  - > any\_dontcare
  - > nextbox\_with\_test test\_syn\_hide(!HIDE\_MAP,!HIDE\_DOMINANT...
  - > nextbox\_with\_test test\_syn\_hide(!HIDE\_MAP),decode\_or
  - > nextbox\_with\_test test\_syn\_hide(!HIDE\_MAP),decode\_and
  - > propcon 1
  - > cleanup 1
  - > nextbox prep\_minterm,minterm
  - > any\_dontcare
  - > cleanse
  - > nextbox mapterm
  - > has\_children CONSTANT
  - > nextbox mapcon
  - > nextbox\_with\_test test\_syn\_hide(HIDE\_MAP),mapcomp,mapadd...

[mapadd]: Execution time was 0.0 seconds.

- > nextbox xpndcomp
- > nextbox xpndmux
- > nextbox xpndsel,xpnddcd
- > nextbox xpndadd
- > nextbox xpndao
- > nextbox xpndcsa
- > cleanse
- > fixpads
- > unpadnet
- > good\_names

## Good names for IDCDSUC

			Cou	nt User	Like	New
For all nets	838	3 75.30%	0.00%	24.70%		
For register output nets	166	100.00%	0.00%	0.00%		
For break point input nets	180	100.00%	0.00%	0.00%		
For model input/output nets	185	100.00%	0.00%	0.00%		

Count User Like New For all boxes 615 70.57% 0.00% 29.43%

For all boxes 615 70.57% 0.00% 29.43% For register boxes 83 100.00% 0.00% 0.00%

- > synzexpnd -hierarchy
- > checksrc
- > msg::get\_level -msgid BD-41519
- > msg::set\_level -msgid BD-41519 -hidden
  - > expand -view SYNZ\_EXPANSIONS -hide -copy\_all\_keys

```
bdz> post_expand
                 > sweep
                 > delbrkpt BREAKLOOPS
                 > brkloops
                 > nextnet {delkey( EDIFNAME )}
                 > nextbox {delkey( EDIFNAME )}
                      > set_nochange
                      > rtolbox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
                      > ltorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
                      > sweep
                    > nochange
                 > nextbox_with_test test_key(IOPAD_LOCATION,2),resolve_net...
                 > nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
                 > nextbox merge_dots()
                 > nextbox dot2ms()
                 > nextnet {ms2dot( BUS )}
              > expand -view SYNZ_EXPANSIONS -hide -copy_all_keys
bdz> post_expand
                 > sweep
                 > delbrkpt BREAKLOOPS
                 > brkloops
                 > nextnet {delkey( EDIFNAME )}
                 > nextbox {delkey( EDIFNAME )}
                     > set nochange
                     > rtolbox_with_test test_key(IOPAD_LOCATION,2),rm_dangling...
                     > ltorbox_with_test test_key(IOPAD_LOCATION,1),rm_dangling...
                     > sweep
                    > nochange
                > nextbox_with_test test_key(IOPAD_LOCATION,2),resolve net...
                > nextbox_with_test test_key(IOPAD_LOCATION,1),resolve_net...
                > sweep
                > nextbox merge_dots()
                > nextbox dot2ms()
                > nextnet {ms2dot( BUS )}
          > msg::set_level -msgid BD-41519 -warning
[SynzExt-19]: Wrote design hierarchy IDCDSUC with 2 proto boxes to HNL file
'/data/laceyl/synztmp/IDCDSUC/IDCDSUC.hnl'
        > write_timer_parms -file /data/laceyl/synztmp/IDCDSUC/IDC...
[ICM-15]: >Begin...Parms Export
        for file /data/laceyl/synztmp/IDCDSUC/IDCDSUC.tparms.
[ICM-16]: <End.....Parms Export.
       > write_lib -file /data/laceyl/synztmp/IDCDSUC/IDCDSUC/CC8...
[SynzExt-22]: Writing to file /data/laceyl/synztmp/IDCDSUC/IDCDSUC/CC8S.lib
Please wait while the Constant Delay Synthesis engine is initialized...
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/tcl/8.0/dll-rs6000/expect.dll
expect.dll version 5.26 (Nov 19 1998 15:52:48)
Expect Tcl extension
    > observe
observe -none -ci_cmds read_bdz -remove -dir /data/laceyl/synztmp/IDCDSUC -file IDCDSUC -libanal
bscc8_anal.tcl -no_liblint -no_interact -no_assert Loading:
/data/laceyl/synztmp/IDCDSUC/IDCDSUC/top.tcl
```

```
Synz
                                                                      Nutshell version 1.672
                                                   Licensed Materials - Property of IBM
(03-25-1999)
5765-XXX
                        (C) Copyright IBM Corporation 1997
                                                                               All Rights Reserved
Install Directory: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/nutshell/1.0 Machine: bsp5n11, AIX
4.1 32bit, 595 POWER2 (L1 i32k d128k, L2 0k), 1 cpu Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/.synz Binding:
/afs/watson.jbm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/hnl.dll hnl.dll version 1.0 (Apr 14 1999
18:12:01) HNL Banner Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/dll/license.dll
license.dll version 3.1 (Apr 07 1999 14:28:56) Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/timer.dll timer.dll version 1.0 (Apr 14
                                                      CMVC Release Level: 03.01
                                                                                         Compiled: Fri
1999 18:12:09) [ET-0101]:Initializing EinsTimer...
Feb 5 09:05:11 1999 [ET-0102]:EinsTimer Version 3 Release 1
                                                                     Licensed Materials-Property of
                                                           All rights reserved.
          5765-801 (C) Copyright IBM Corp. 1994-97
                                                                                           US
Government Users Restricted Rights -
                                            Use, duplication or disclosure restricted
                                                                                         by GSA
Schedule Contract with IBM Corp.
                                               "IBM" and "EinsTimer" are trademarks of
"International Business Machines" [ET-0110]:License obtained for ..... EinsTimer 1.1 Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/synzilla.dll synzilla.dll version 1.0 (Apr
16 1999 10:14:14) Synzilla Build Version: 1.0.219 Load calculator version 2 - initialized Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/synz_init.tcl Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/create attributes.tcl Loading:
/afs/apd.pok.ibm.com/u/laceyl/.synz_variables Interactive nutshell, "help" for help, "exit" or ctrl-d to exit.
\square[7msynz\square[0m\square[1m@bsp5n11>\square[0m
□[14Cobserve -none -ci_cmds □[7msynz□[0m□[1m@bsp5n11>□[0m
[14Cread bdz -remove -dir /data/laceyl/synztmp/IDCDSUC -file IDCDSUC -libanal bscc8_anal.tcl
-no_liblint -no_interact -no_assert Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/read_bdz.tcl
                                                                              > echo {synz interact 0}
                     > read timer parms -file /data/laceyl/synztmp/IDCDSUC/IDCD... ICM-015 I:
synz interact 0
                               for file /data/laceyl/synztmp/IDCDSUC/IDCDSUC.tparms. ICM-016 I:
>Begin...Parm Reader
                                    > echo {Reading library file /data/lacevl/synztmp/IDCDSUC/...
<End.....Parm Reader.
Reading library file /data/laceyl/synztmp/IDCDSUC/IDCDSUC/CC8S.lib
                                                                            > msa::aet level -msaid
                 > msg::set_level -msgid MASK-108 -hidden
                                                                  > msg::set_level -msgid MASK-108
MASK-108
                > load cdc rule -rule /afs/apd/func/vlsi/alliance00/bscc8/... [ET-1757]:Initializing CDC...
-warning
[ET-1758]: Rule
                   = /afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface_RS6K [ET-1759]: Sub
Rules =
/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/%RULENAME
[ET-1760]: Tables
/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/tables:/afs/apd/fu
nc/vlsi/alliance00/bscc8/prod/ndr/../tables:/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/%RULENAME
[ET-0607]: Starting the dynamic link to CDC for rule:
/afs/apd/func/vlsi/alliance00/bscc8/prod/ndr/IEEEinterface_RS6K [DCL-0512]: DCL Runtime Environment
                  Last compiled on Apr 12 1999 at 10:00:33. [DCL-0642]: I am running in process ID
147522 [DCL-17001]: RLEV: DCMinterface rule, version v1.0.2 IEEE 1481-1998, technology GENERIC,
-19009]: CAP: Setting DEFAULT PINCAP value to: 0 as defined by environment variable
<DCM_DEFAULT_PINCAP> [DCL-17001]: RLEV: Methods subrule, version v1.0.2 IEEE 1481-1998,
was compiled on 14:17:39 at Mar 12 1999 [DCL-19021]: INFO: Maximum number of DCM messages to
be printed has been set to 100000000 [DCL-17001]: RLEV: LimitPrint subrule, version v1.0 IEEE
1481-1998, was compiled on 14:17:44 at Mar 12 1999 [DCL-17001]: RLEV: printSummary subrule,
version v1.0 IEEE 1481-1998, was compiled on 14:18:37 at Mar 12 1999 [DCL-17001]: RLEV: Ceffective
subrule, version v1.0 IEEE 1481-1998, was compiled on 14:17:50 at Mar 12 1999 [DCL-19000]: ENV:
Environment variable < DCMCAPTHRESHOLD> NOT set by user. [DCL-19017]: CAP: EffectiveC Cap
Threshold not set. [DCL-17001]: RLEV: techSpec subrule, version v1.0.3 IEEE 1481-1998, was compiled
on 14:17:56 at Mar 12 1999 [DCL-17001]: RLEV: WireLoad subrule, version v1.0.1 IEEE 1481-1998, was
compiled on 14:18:04 at Mar 12 1999 [DCL-17001]: RLEV: WireLoad table, Version 1.0.1 IEEE
1481-1998 Technology SA27, was compiled on 14:18:04 at Mar 12 1999 [DCL-17040]: The available
wireload model levels are: 5lm, 6lm [DCL-17002]: Environmental variable DCMWireLoadLevels not set
```

using default. [DCL-17001]: RLEV: NetDelay subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:12 at Mar 12 1999 [DCL-17001]: RLEV: cellName subrule, version v1.5 IEEE 1481-1998, was compiled on 14:18:17 at Mar 12 1999 [DCL-17001]: RLEV: CellName parser subrule, version v1.0.5 IEEE 1481-1998, was compiled on 14:18:30 at Mar 12 1999 [DCL-17001]: RLEV: Defaults subrule. version v1.0.4 IEEE 1481-1998, was compiled on 14:18:40 at Mar 12 1999 [DCL-17012]: Using the default supplied bomFile [DCL-17001]: RLEV: \_cc8s\_rules\_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 09:32:54 at Apr 12 1999 [DCL-17001]: RLEV: \_cc8s\_latches\_r subrule, version v1.0.9 IEEE 1481-1998, was compiled on 12:12:01 at Apr 6 1999 [DCL-17001]: RLEV: railCache subrule, version v1.0 IEEE 1481-1998, was compiled on 14:18:52 at Mar 12 1999 [DCL-17020]: Environmental variable DCMDoRangeCheck set to do no reporting. [ET-0655]:IEEE standard interface version "IEEE technology "GENERIC". Library identification: "IBM\_GENERIC". [ET-0652]:Could 1481-1998" for not find IEEE standard routine dpcmGetDelayGradient in rules. Substituting dummy routine. [ET-0652]:Could not find IEEE standard routine dpcmGetSlewGradient in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGetAETCellPowerWithSensitivity in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGroupGetSettlingTime in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGroupGetSimultaneousSwitchTime in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmCalcPartialSwingEnergy in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmSetInitialState in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmFillPinCache in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmFreePinCache in rules. Substituting dummy routine. [ET-0653]:Could not find IEEE standard power routine dpcmGetNetEnergy in rules. Substituting dummy routine. [ET-0611]:Dynamic link to CDC rule complete. [HNLIO-2007]: Loaded library 'HISVHDL'. > hnl::hnl\_nets\_preserve -initialize > echo SYNZ\_READ\_BDZ SYNZ\_READ\_BDZ > source bscc8\_anal.tcl Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/bscc8\_anal.tcl > echo {Setting picap to 0.2} Setting picap to 0.2 > hnl::get\_active\_idesign > load units -femto > time\_units -pico > hnl\_attr\_get\_by\_name -obj\_type port -name PIN\_FUNCTION top level created for design: IDCDSUC, analysis mode: SLOW\_CHIP. [ET-1709]:Could not find clock or phase "C3". set load limit for port a\_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port b\_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port test\_c1 to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port clkg to 10000.0 set load limit for port gptr\_scan\_in to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port scan\_in to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port gptr\_a\_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port gptr\_b\_clk to 10000.0 [ET-1709]:Could not find clock or phase "C3". set load limit for port clkg2 to 10000.0 set load limit for port scan\_enable to 10000.0 [ET-1709]:Could not find clock or phase "C3". slow\_mode.clockblock cb\_clk\_32\_1 set load limit on slow\_mode.clockblock/c1 to 10000.0 set slew limit on slow\_mode.clockblock/c1 to 650.0 set slew limit on iu\_rst\_fst\_t1.reg\_n.lat\_0/C1 to 650.0 set slew limit on inst\_store.reg\_n.lat\_0/C1 to 650.0 set slew limit on eu\_dsbl\_aftr.reg\_n.lat\_0/C1 to 650.0 set slew limit on dcdsuc\_err.reg\_n.lat\_0/C1 to 650.0 set slew limit on dcd\_cyl\_cnt.reg\_n.lat\_0/C1 to 650.0 set slew limit on dcd\_cyl\_cnt.reg\_n.lat\_1/C1 to 650.0 set slew limit on blk\_mcend.reg\_n.lat\_0/C1 to 650.0 set slew limit on op\_44\_info.reg\_n.lat\_0/C1 to 650.0 set slew limit on op\_44\_info.reg\_n.lat\_1/C1 to 650.0 set slew limit on rcvry\_reset.reg\_n.lat\_0/C1 to 650.0 set slew limit on br\_wrongs.reg\_n.lat\_0/C1 to 650.0 set slew limit on rstrt\_reset.reg\_n.lat\_0/C1 to 650.0 set slew limit on br\_dcd\_pend.reg\_n.lat\_0/C1 to 650.0 set load limit on slow\_mode.clockblock/c2 to 10000.0 set slew limit on slow\_mode.clockblock/c2 to 650.0 set slew limit on iu\_rst\_fst\_t1.reg\_n.lat\_0/B to 650.0 set slew limit on inst\_store.reg\_n.lat\_0/B to 650.0 set slew limit on eu\_dsbl\_aftr.reg\_n.lat\_0/B to 650.0 set slew limit on dcdsuc\_err.reg\_n.lat\_0/B to 650.0 set slew limit on dcd\_cyl\_cnt.reg\_n.lat\_0/B to 650.0 set slew limit on dcd\_cyl\_cnt.reg\_n.lat\_1/B to 650.0 set slew limit on blk\_mcend.reg\_n.lat\_0/B to 650.0 set slew limit on op\_44\_info.reg\_n.lat\_0/B to 650.0 set slew limit on op\_44\_info.reg\_n.lat\_1/B to 650.0 set slew limit on rcvry\_reset.reg\_n.lat\_0/B to 650.0 set slew limit on br\_wrongs.reg\_n.lat\_0/B to 650.0 set slew limit on rstrt\_reset.reg\_n.lat\_0/B to 650.0 set slew limit on br\_dcd\_pend.reg\_n.lat\_0/B to 650.0 set load limit on slow\_mode.clockblock/clka to 10000.0 set slew limit on slow\_mode.clockblock/clka to 650.0 set slew limit on iu\_rst\_fst\_t1.reg\_n.lat\_0/A to 650.0 set slew limit on inst\_store.reg\_n.lat\_0/A to 650.0 set slew limit on eu\_dsbl\_aftr.reg\_n.lat\_0/A to 650.0 set slew limit on

dcdsuc\_err.reg\_n.lat\_0/A to 650.0 set slew limit on dcd\_cyl\_cnt.reg\_n.lat\_0/A to 650.0 set slew limit on dcd\_cyl\_cnt.reg\_n.lat\_1/A to 650.0 set slew limit on blk\_mcend.reg\_n.lat\_0/A to 650.0 set slew limit on op\_44\_info.reg\_n.lat\_0/A to 650.0 set slew limit on op\_44\_info.reg\_n.lat\_1/A to 650.0 set slew limit on rcvry reset.reg\_n.lat\_0/A to 650.0 set slew limit on br\_wrongs.reg\_n.lat\_0/A to 650.0 set slew limit on rstrt\_reset.reg\_n.lat\_0/A to 650.0 set slew limit on br\_dcd\_pend.reg\_n.lat\_0/A to 650.0 set load limit on slow mode.clockblock/a\_clk to 10000.0 set slew limit on a\_clk to 650.0 set slew limit on slow mode.clockblock/a clk to 650.0 set slew limit on slow\_mode.clockblock\_1/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_2/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_3/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_4/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_5/a\_clk to 650.0 set load limit on slow\_mode.clockblock/b\_clk to 10000.0 set slew limit on b\_clk to 650.0 set slew limit on slow\_mode.clockblock/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_1/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_2/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_3/b\_clk to mode.clockblock\_4/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_5/b\_clk to 650.0 set load limit on slow mode.clockblock/clkg to 10000.0 set slew limit on clkg to 650.0 set slew limit on slow mode.clockblock/clkg to 650.0 set slew limit on slow\_mode.clockblock\_1/clkg to 650.0 set slew limit on slow mode.clockblock 2/clkg to 650.0 set load limit on slow\_mode.clockblock/scan\_enable to 10000.0 set slew limit on scan\_enable to 650.0 set slew limit on slow\_mode.clockblock/scan\_enable to 650.0 set slew limit on slow mode.clockblock\_1/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_2/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_3/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_4/scan\_enable to 650.0 set slew limit on slow mode.clockblock\_5/scan\_enable to 650.0 set load limit on slow\_mode.clockblock/clkl\_mode4 to 10000.0 set slew limit on gptr\_latch/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode4 to 650.0 set slew limit on slow mode.clockblock\_3/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode4 to 650.0 set load limit on slow mode.clockblock/clkl\_mode5 to 10000.0 set slew limit on gptr\_latch/clkl\_mode5 to 650.0 set slew limit on slow mode.clockblock/clkl mode5 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode5 to 650.0 set slew limit on slow mode.clockblock\_3/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode5 to 650.0 set slew limit on slow mode.clockblock\_5/clkl\_mode5 to 650.0 set load limit on slow\_mode.clockblock/clkl\_mode6 to 10000.0 set slew limit on gptr\_latch/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode6 to 650.0 set slew limit on slow mode.clockblock\_2/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode6 to 650.0 set load limit on slow\_mode.clockblock/clkl\_mode7 to 10000.0 set slew limit on clkl\_mode7 to 650.0 set slew limit on slow mode.clockblock/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode7 to 650.0 set slew limit on slow mode.clockblock 3/clkl mode7 to 650.0 set slew limit on slow mode.clockblock\_4/clkl\_mode7 to 650.0 set slew limit on slow mode.clockblock\_5/clkl\_mode7 to 650.0 set load limit on slow\_mode.clockblock/clkl\_mode8 to 10000.0 set slew limit on gptr\_latch/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode8 to 650.0 set load limit on slow\_mode.clockblock/test\_c1 to 10000.0 set slew limit on test\_c1 to 650.0 set slew limit on slow\_mode.clockblock/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_1/test\_c1 to 650.0 set slew limit on slow mode.clockblock\_2/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_3/test\_c1 to 650.0 set slew limit on slow mode.clockblock 4/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_5/test\_c1 to 650.0 slow\_mode.clockblock\_1 cb\_clk\_32\_1 set load limit on slow\_mode.clockblock\_1/c1 to 10000.0 set slew limit on slow\_mode.reg\_n.lat\_0/C1 to 650.0 set slew limit on ru\_rq\_blk.reg\_n.lat\_0/C1 to 650.0 set slew limit on iu\_rst\_fst.reg\_n.lat\_0/C1 to 650.0 set slew limit on iu\_restart.reg\_n.lat\_0/C1 to 650.0 set slew limit on ia\_to\_if.reg\_n.lat\_0/C1 to 650.0 set slew limit on frc\_mmode.reg\_n.lat\_0/C1 to 650.0 set slew limit on local\_milli.reg\_n.lat\_0/C1 to 650.0 set slew limit on

eg\_n.lat\_0/C1 to 650.0 set slew limit on mia\_to\_if.reg\_n.lat\_0/C1 to 650.0 set slew limit on slow\_mode\_t1.reg\_n.lat\_0/C1 to 650.0 set slew limit on iq\_empty\_dly.reg\_n.lat\_0/C1 to 650.0 set slew limit on slow\_mode\_t2.reg\_n.lat\_0/C1 to 650.0 set slew limit on s390\_updt\_blk.reg\_n.lat\_0/C1 to 650.0 set slew limit on srlz\_nomatch.reg\_n.lat\_0/C1 to 650.0 set slew limit on slow\_mode.clockblock\_1/c1 to 650.0 set load limit on slow\_mode.clockblock\_1/c2 to 10000.0 set slew limit on slow\_mode.reg\_n.lat\_0/B to 650.0 set slew limit on ru\_rq\_blk.reg\_n.lat\_0/B to 650.0 set slew limit on iu\_rst\_fst.reg\_n.lat\_0/B to 650.0 set slew limit on iu\_restart.reg\_n.lat\_0/B to 650.0 set slew limit on ia\_to\_if.reg\_n.lat\_0/B to 650.0 set slew limit on frc\_mmode.reg\_n.lat\_0/B to 650.0 set slew limit on local\_milli.reg\_n.lat\_0/B to 650.0 set slew limit on ia\_to\_if\_t1.reg\_n.lat\_0/B to 650.0 set slew limit on mia\_to\_if.reg\_n.lat\_0/B to 650.0 set slew limit on slow\_mode\_t1.reg\_n.lat\_0/B to 650.0 set slew limit on iq\_empty\_dly.reg\_n.lat\_0/B to 650.0 set slew limit on slow\_mode\_t2.reg\_n.lat\_0/B to 650.0 set slew limit on s390\_updt\_blk.reg\_n.lat\_0/B to 650.0 set slew limit on srlz\_nomatch.reg\_n.lat\_0/B to 650.0 set slew limit on slow\_mode.clockblock\_1/c2 to 650.0 set load limit on slow\_mode.clockblock\_1/clka to 10000.0 set slew limit on slow\_mode.reg\_n.lat\_0/A to 650.0 set slew limit on ru\_rq\_blk.reg\_n.lat\_0/A to 650.0 set slew limit on iu\_rst\_fst.reg\_n.lat\_0/A to 650.0 set slew limit on iu\_restart.reg\_n.lat\_0/A to 650.0 set slew limit on ia\_to\_if.reg\_n.lat\_0/A to 650.0 set slew limit on frc\_mmode.reg\_n.lat\_0/A to 650.0 set slew limit on local\_milli.reg\_n.lat\_0/A to 650.0 set slew limit on ia\_to\_if\_t1.reg\_n.lat\_0/A to 650.0 set slew limit on mia\_to\_if.reg\_n.lat\_0/A to 650.0 set slew limit on slow\_mode\_t1.reg\_n.lat\_0/A to 650.0 set slew limit on iq\_empty\_dly.reg\_n.lat\_0/A to 650.0 set slew limit on slow\_mode\_t2.reg\_n.lat\_0/A to 650.0 set slew limit on s390\_updt\_blk.reg\_n.lat\_0/A to 650.0 set slew limit on srlz\_nomatch.reg\_n.lat\_0/A to 650.0 set slew limit on slow\_mode.clockblock\_1/clka to 650.0 set load limit on slow\_mode.clockblock\_1/a\_clk to 10000.0 set slew limit on a\_clk to 650.0 set slew limit on slow\_mode.clockblock/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_1/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_2/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_3/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_4/a\_clk to 650.0 set slew limit on slow\_mode.clockblock\_5/a\_clk to 650.0 set load limit on slow\_mode.clockblock\_1/b\_clk to 10000.0 set slew limit on b\_clk to 650.0 set slew limit on slow\_mode.clockblock/b clk to 650.0 set slew limit on slow\_mode.clockblock\_1/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_2/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_3/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_4/b\_clk to 650.0 set slew limit on slow\_mode.clockblock\_5/b\_clk to 650.0 set load limit on slow\_mode.clockblock\_1/clkg to 10000.0 set slew limit on clkg to 650.0 set slew limit on slow\_mode.clockblock/clkg to 650.0 set slew limit on slow\_mode.clockblock\_1/clkg to 650.0 set slew limit on slow\_mode.clockblock\_2/clkg to 650.0 set load limit on slow\_mode.clockblock\_1/scan\_enable to 10000.0 set slew limit on scan\_enable to 650.0 set slew limit on slow\_mode.clockblock/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_1/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_2/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_3/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_4/scan\_enable to 650.0 set slew limit on slow\_mode.clockblock\_5/scan\_enable to 650.0 set load limit on slow\_mode.clockblock\_1/clkl\_mode4 to 10000.0 set slew limit on gptr\_latch/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode4 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode4 to it on slow\_mode.clockblock\_5/clkl\_mode4 to 650.0 set load limit on slow\_mode.clockblock\_1/clkl\_mode5 to 10000.0 set slew limit on gptr\_latch/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode5 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode5 to 650.0 set load limit on slow\_mode.clockblock\_1/clkl\_mode6 to 10000.0 set slew limit on gptr\_latch/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode6 to 650.0 set load limit on slow\_mode.clockblock\_1/clkl\_mode7 to 10000.0 set slew limit on clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode7 to 650.0 set slew limit on

```
slow mode.clockblock_3/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode7 to 650.0 set load limit on
slow mode.clockblock_1/clkl_mode8 to 10000.0 set slew limit on gptr_latch/clkl_mode8 to 650.0 set slew
limit on slow mode.clockblock/clkl mode8 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode8
to 650.0 set slew limit on slow mode, clockblock 2/clkl mode8 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode8 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode8 to 650.0 set load limit on
slow mode.clockblock 1/test c1 to 10000.0 set slew limit on test_c1 to 650.0 set slew limit on
slow_mode.clockblock/test_c1 to 650.0 set slew limit on slow_mode.clockblock_1/test_c1 to 650.0 set
slew limit on slow_mode.clockblock_2/test_c1 to 650.0 set slew limit on slow_mode.clockblock_3/test_c1
to 650.0 set slew limit on slow mode.clockblock_4/test_c1 to 650.0 set slew limit on
slow mode.clockblock_5/test_c1 to 650.0 slow_mode.clockblock_2 cb_clk_32_1 set load limit on
slow mode.clockblock 2/c1 to 10000.0 set slew limit on bce_hold_aa.reg_n.lat_0/C1 to 650.0 set slew
limit on srlz_actn.reg_n.lat_0/C1 to 650.0 set slew limit on srlz_actn.reg_n.lat_1/C1 to 650.0 set slew limit
on op_44_dcd.reg_n.lat_0/C1 to 650.0 set slew limit on op_cmp_tr.reg_n.lat_0/C1 to 650.0 set slew limit
on num_dcd.reg_n.lat_0/C1 to 650.0 set slew limit on num_dcd.reg_n.lat_1/C1 to 650.0 set slew limit on
mia_to_if_t1.reg_n.lat_0/C1 to 650.0 set slew limit on eu_op_encode.reg_n.lat_0/C1 to 650.0 set slew
limit on eu_op_encode.reg_n.lat_1/C1 to 650.0 set slew limit on eu_op_encode.reg_n.lat_2/C1 to 650.0
set slew limit on eu_op_encode.reg_n.lat_3/C1 to 650.0 set slew limit on eu_op_encode.reg_n.lat_4/C1
to 650.0 set slew limit on eu_op_encode.req_n.lat_5/C1 to 650.0 set slew limit on
slow_mode.clockblock_2/c1 to 650.0 set load limit on slow_mode.clockblock_2/c2 to 10000.0 set slew
limit on bce_hold_aa.req_n.lat_0/B to 650.0 set slew limit on srlz_actn.reg_n.lat_0/B to 650.0 set slew
limit on srlz actn.reg_n.lat_1/B to 650.0 set slew limit on op_44_dcd.reg_n.lat_0/B to 650.0 set slew limit
on op_cmp_tr.reg_n.lat_0/B to 650.0 set slew limit on num_dcd.reg_n.lat_0/B to 650.0 set slew limit on
num_dcd.reg_n.lat_1/B to 650.0 set slew limit on mia_to_if_t1.reg_n.lat_0/B to 650.0 set slew limit on
eu op encode.reg n.lat 0/B to 650.0 set slew limit on eu op encode.reg n.lat 1/B to 650.0 set slew
limit on eu_op_encode.reg_n.lat_2/B to 650.0 set slew limit on eu_op_encode.reg_n.lat_3/B to 650.0 set
slew limit on eu_op_encode.reg_n.lat_4/B to 650.0 set slew limit on eu_op_encode.reg_n.lat_5/B to 650.0
ock_2/c2 to 650.0 set load limit on slow_mode.clockblock_2/clka to 10000.0 set slew limit on
bce_hold_aa.reg_n.lat_0/A to 650.0 set slew limit on srlz_actn.reg_n.lat_0/A to 650.0 set slew limit on
srlz_actn.reg_n.lat_1/A to 650.0 set slew limit on op_44_dcd.reg_n.lat_0/A to 650.0 set slew limit on
op_cmp_tr.reg_n.lat_0/A to 650.0 set slew limit on num_dcd.reg_n.lat_0/A to 650.0 set slew limit on
num_dcd.reg_n.lat_1/A to 650.0 set slew limit on mia_to_if_t1.reg_n.lat_0/A to 650.0 set slew limit on
eu op encode.reg_n.lat_0/A to 650.0 set slew limit on eu_op_encode.reg_n.lat_1/A to 650.0 set slew
limit on eu_op_encode.reg_n.lat_2/A to 650.0 set slew limit on eu_op_encode.reg_n.lat_3/A to 650.0 set
slew limit on eu_op_encode.reg_n.lat_4/A to 650.0 set slew limit on eu_op_encode.reg_n.lat_5/A to 650.0
set slew limit on slow_mode.clockblock_2/clka to 650.0 set load limit on slow_mode.clockblock_2/a_clk to
10000.0 set slew limit on a clk to 650.0 set slew limit on slow mode.clockblock/a clk to 650.0 set slew
limit on slow mode.clockblock 1/a_clk to 650.0 set slew limit on slow_mode.clockblock_2/a_clk to 650.0
set slew limit on slow mode.clockblock 3/a clk to 650.0 set slew limit on slow_mode.clockblock_4/a_clk
to 650.0 set slew limit on slow mode.clockblock 5/a clk to 650.0 set load limit on
slow mode.clockblock 2/b_clk to 10000.0 set slew limit on b_clk to 650.0 set slew limit on
slow mode.clockblock/b clk to 650.0 set slew limit on slow_mode.clockblock_1/b_clk to 650.0 set slew
limit on slow_mode.clockblock_2/b_clk to 650.0 set slew limit on slow_mode.clockblock_3/b_clk to 650.0
set slew limit on slow_mode.clockblock_4/b_clk to 650.0 set slew limit on slow_mode.clockblock_5/b_clk
to 650.0 set load limit on slow mode.clockblock 2/clkg to 10000.0 set slew limit on clkg to 650.0 set slew
limit on slow_mode.clockblock/clkg to 650.0 set slew limit on slow_mode.clockblock_1/clkg to 650.0 set
slew limit on slow_mode.clockblock_2/clkg to 650.0 set load limit on
slow_mode.clockblock_2/scan_enable to 10000.0 set slew limit on scan_enable to 650.0 set slew limit on
slow_mode.clockblock/scan_enable to 650.0 set slew limit on slow_mode.clockblock_1/scan_enable to
650.0 set slew limit on slow mode.clockblock 2/scan enable to 650.0 set slew limit on
slow_mode.clockblock_3/scan_enable to 650.0 set slew limit on slow_mode.clockblock_4/scan_enable to
650.0 set slew limit on slow_mode.clockblock_5/scan_enable to 650.0 set load limit on
slow_mode.clockblock_2/clkl_mode4 to 10000.0 set slew limit on gptr_latch/clkl_mode4 to 650.0 set slew
limit on slow_mode.clockblock/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode4
```

```
to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode4 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode4 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode4 to 650.0 set load limit on
slow_mode.clockblock_2/clkl_mode5 to 10000.0 set slew limit on gptr_latch/clkl_mode5 to 650.0 set slew
limit on slow_mode.clockblock/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode5
 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode5 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode5 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode5 to 650.0 set load limit on
slow_mode.clockblock_2/clkl_mode6 to 10000.0 set slew limit on gptr_latch/clkl_mode6 to 650.0 set slew
limit on slow_mode.clockblock/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode6
to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode6 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode6 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode6 to 650.0 set load limit on
slow_mode.clockblock_2/clkl_mode7 to 10000.0 set slew limit on clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode7 to
limit on slow_mode.clockblock_2/clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode7 to 650.0 set load limit on
slow_mode.clockblock_2/clkl_mode8 to 10000.0 set slew limit on gptr_latch/clkl_mode8 to 650.0 set slew
limit on slow_mode.clockblock/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_1/clkl_mode8
to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode8 to 650.0 set slew limit on
slow_mode.clockblock_3/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_4/clkl_mode8 to
650.0 set slew limit on slow_mode.clockblock_5/clkl_mode8 to 650.0 set load limit on
slow_mode.clockblock_2/test_c1 to 10000.0 set slew limit on test_c1 to 650.0 set slew limit on
slow_mode.clockblock/test_c1 to 650.0 set slew limit on slow_mode.clockblock_1/test_c1 to 650.0 set
slew limit on slow_mode.clockblock_2/test_c1 to 650.0 set slew limit on slow_mode.clockblock_3/test_c1
to 650.0 set slew limit on slow_mode.clockblock_4/test_c1 to 650.0 set slew limit on
slow_mode.clockblock_5/test_c1 to 650.0 slow_mode.clockblock_3 cb_clk_32_1 set load limit on
slow_mode.clockblock_3/c1 to 10000.0 set slew limit on eu_op_encode.reg_n.lat_6/C1 to 650.0 set slew
limit on eu_op_encode.reg_n.lat_7/C1 to 650.0 set slew limit on eu_op_encode.reg_n.lat_8/C1 to 650.0
set slew limit on eu_op_encode.reg_n.lat_9/C1 to 650.0 set slew limit on eu_op_encode.reg_n.lat_10/C1
to 650.0 set slew limit on eu_op_encode.reg_n.lat_11/C1 to 650.0 set slew limit on
frc_blk_1cyc.reg_n.lat_0/C1 to 650.0 set slew limit on local_milli_t1.reg_n.lat_0/C1 to 650.0 set slew limit
on local_milli_t2.reg_n.lat_0/C1 to 650.0 set slew limit on bht_block.reg_n.lat_0/C1 to 650.0 set slew limit
on srlz_blk.reg_n.lat_0/C1 to 650.0 set slew limit on exc_cond.reg_n.lat_0/C1 to 650.0 set slew limit on
slow_mode_dly.reg_n.lat_0/C1 to 650.0 set slew limit on dcd_succ_disable_scan.reg_n.lat_0/C1 to 650.0
set slew limit on slow_mode.clockblock_3/c1 to 650.0 set load limit on slow_mode.clockblock_3/c2 to
10000.0 set slew limit on eu_op_encode.reg_n.lat_6/B to 650.0 set slew limit on
eu_op_encode.reg_n.lat_7/B to 650.0 set slew limit on eu_op_encode.reg_n.lat_8/B to 650.0 set slew
limit on eu_op_encode.reg_n.lat_9/B to 650.0 set slew limit on eu_op_encode.reg_n.lat_10/B to 650.0 set
slew limit on eu_op_encode.reg_n.lat_11/B to 650.0 set slew limit on frc_blk_1cyc.reg_n.lat_0/B to 650.0
set slew limit on local_milli_t1.reg_n.lat_0/B to 650.0 set slew limit on local_milli_t2.reg_n.lat_0/B to 650.0
set slew limit on bht_block.reg_n.lat_0/B to 650.0 set slew limit on srlz_blk.reg_n.lat_0/B to 650.0 set slew
limit on exc_cond.reg_n.lat_0/B to 650.0 set slew limit on slow_mode_dly.reg_n.lat_0/B to 650.0 set slew
limit on dcd_succ_disable_scan.reg_n.lat_0/B to 650.0 set slew limit on slow_mode.clockblock_3/c2 to
650.0 set load limit on slow_mode.clockblock_3/clka to 10000.0 set slew limit on
eu_op_encode.reg_n.lat_6/A to 650.0 set slew limit on eu_op_encode.reg_n.lat_7/A to 650.0 set slew
limit on eu_op_encode.reg_n.lat_8/A to 650.0 set slew limit on eu_op_encode.reg_n.lat_9/A to 650.0 set
slew limit on eu_op_encode.reg_n.lat_10/A to 650.0 set slew limit on eu_op_encode.reg_n.lat_11/A to
650.0 set slew limit on frc_blk_1cyc.reg_n.lat_0/A to 650.0 set slew limit on local_milli_t1.reg_n.lat_0/A to
650.0 set slew limit on local_milli_t2.reg_n.lat_0/A to 650.0 set slew limit on bht_block.reg_n.lat_0/A to
650.0 set slew limit on srlz_blk.reg_n.lat_0/A to 650.0 set slew limit on exc_cond.reg_n.lat_0/A to 650.0
set slew limit on slow_mode_dly.reg_n.lat_0/A to 650.0 set slew limit on
dcd_succ_disable_scan.reg_n.lat_0/A to 650.0 set slew limit on slow_mode.clockblock_3/clka to 650.0
set load limit on slow_mode.clockblock_3/a_clk to 10000.0 set slew limit on a_clk to 650.0 set slew limit
```

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on slow_mode.clockblock/a_clk to 650.0 set slew limit on slow_mode.clockblock_1/a_clk to 650.0 set
.clockblock_3/a_clk to 650.0 set slew limit on slow_mode.clockblock_4/a_clk to 650.0 set slew limit on
slow mode.clockblock 5/a clk to 650.0 set load limit on slow_mode.clockblock_3/b_clk to 10000.0 set
slew limit on b_clk to 650.0 set slew limit on slow_mode.clockblock/b_clk to 650.0 set slew limit on
slow mode.clockblock 1/b clk to 650.0 set slew limit on slow_mode.clockblock_2/b_clk to 650.0 set slew
limit on slow mode.clockblock_3/b_clk to 650.0 set slew limit on slow_mode.clockblock_4/b_clk to 650.0
set slew limit on slow mode.clockblock_5/b_clk to 650.0 set load limit on slow_mode.clockblock_3/clkg to
10000.0 set slew limit on clkg2 to 650.0 set slew limit on slow_mode.clockblock_3/clkg to 650.0 set slew
limit on slow_mode.clockblock_4/clkg to 650.0 set slew limit on slow_mode.clockblock_5/clkg to 650.0 set
load limit on slow_mode.clockblock_3/scan_enable to 10000.0 set slew limit on scan_enable to 650.0 set
slew limit on slow_mode.clockblock/scan_enable to 650.0 set slew limit on
slow_mode.clockblock_1/scan_enable to 650.0 set slew limit on slow_mode.clockblock_2/scan_enable to
650.0 set slew limit on slow mode.clockblock 3/scan_enable to 650.0 set slew limit on
slow mode.clockblock 4/scan enable to 650.0 set slew limit on slow_mode.clockblock_5/scan_enable to
650.0 set load limit on slow_mode.clockblock_3/clkl_mode4 to 10000.0 set slew limit on
gptr_latch/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode4 to 650.0 set slew limit
on slow_mode.clockblock_1/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode4 to
650.0 set slew limit on slow mode.clockblock_3/clkl_mode4 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode4 to
650.0 set load limit on slow_mode.clockblock_3/clkl_mode5 to 10000.0 set slew limit on
gptr_latch/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode5 to 650.0 set slew limit
on slow mode.clockblock_1/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode5 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode5 to 650.0 set slew limit on
slow mode.clockblock_4/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode5 to
650.0 set load limit on slow mode.clockblock 3/clkl mode6 to 10000.0 set slew limit on
gptr_latch/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode6 to 650.0 set slew limit
on slow mode.clockblock 1/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode6 to
650.0 set slew limit on slow mode.clockblock 3/clkl mode6 to 650.0 set slew limit on
slow mode.clockblock_4/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode6 to
650.0 set load limit on slow_mode.clockblock_3/clkl_mode7 to 10000.0 set slew limit on clkl_mode7 to
650.0 set slew limit on slow mode.clockblock/clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock_1/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode7 to 650.0 set slew limit on
slow mode.clockblock 4/clkl mode7 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode7 to
650.0 set load limit on slow_mode.clockblock_3/clkl_mode8 to 10000.0 set slew limit on
aptr latch/clkl mode8 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode8 to 650.0 set slew limit
on slow mode.clockblock_1/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode8 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode8 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode8 to
650.0 set load limit on slow mode.clockblock 3/test c1 to 10000.0 set slew limit on test_c1 to 650.0 set
slew limit on slow mode.clockblock/test_c1 to 650.0 set slew limit on slow_mode.clockblock_1/test_c1 to
650.0 set slew limit on slow_mode.clockblock_2/test_c1 to 650.0 set slew limit on
slow_mode.clockblock_3/test_c1 to 650.0 set slew limit on slow_mode.clockblock_4/test_c1 to 650.0 set
o 650.0 slow_mode.clockblock_4 cb_clk_32_1 set load limit on slow_mode.clockblock_4/c1 to 10000.0
set slew limit on dcd_succ_disable_scan.reg_n.lat_1/C1 to 650.0 set slew limit on
dcd succ disable scan.reg_n.lat_2/C1 to 650.0 set slew limit on drain_blk.reg_n.lat_0/C1 to 650.0 set
slew limit on dcd_ilc.reg_n.lat_0/C1 to 650.0 set slew limit on dcd_ilc.reg_n.lat_1/C1 to 650.0 set slew
limit on slow_mode_blk.reg_n.lat_0/C1 to 650.0 set slew limit on op_cmp_44.reg_n.lat_0/C1 to 650.0 set
slew limit on op cmp dsbl.reg_n.lat_0/C1 to 650.0 set slew limit on eu_frc_milli.reg_n.lat_0/C1 to 650.0
set slew limit on bcr_store_stat.reg_n.lat_0/C1 to 650.0 set slew limit on exc_info.reg_n.lat_0/C1 to 650.0
set slew limit on exc_info.reg_n.lat_1/C1 to 650.0 set slew limit on exc_info.reg_n.lat_2/C1 to 650.0 set
slew limit on exc_info.reg_n.lat_3/C1 to 650.0 set slew limit on slow_mode.clockblock_4/c1 to 650.0 set
load limit on slow mode.clockblock_4/c2 to 10000.0 set slew limit on
dcd_succ_disable_scan.reg_n.lat_1/B to 650.0 set slew limit on dcd_succ_disable_scan.reg_n.lat_2/B to
650.0 set slew limit on drain_blk.reg_n.lat_0/B to 650.0 set slew limit on dcd_ilc.reg_n.lat_0/B to 650.0 set
```

```
slew limit on dcd_ilc.reg_n.lat_1/B to 650.0 set slew limit on slow_mode_blk.reg_n.lat_0/B to 650.0 set
slew limit on op_cmp_44.reg_n.lat_0/B to 650.0 set slew limit on op_cmp_dsbl.reg_n.lat_0/B to 650.0 set
slew limit on eu_frc_milli.reg_n.lat_0/B to 650.0 set slew limit on bcr_store_stat.reg_n.lat_0/B to 650.0 set
slew limit on exc_info.reg_n.lat_0/B to 650.0 set slew limit on exc_info.reg_n.lat_1/B to 650.0 set slew
limit on exc_info.reg_n.lat_2/B to 650.0 set slew limit on exc_info.reg_n.lat_3/B to 650.0 set slew limit on
slow_mode.clockblock_4/c2 to 650.0 set load limit on slow_mode.clockblock_4/clka to 10000.0 set slew
limit on dcd_succ_disable_scan.reg_n.lat_1/A to 650.0 set slew limit on
dcd_succ_disable_scan.reg_n.lat_2/A to 650.0 set slew limit on drain_blk.reg_n.lat_0/A to 650.0 set slew
limit on dcd_ilc.reg_n.lat_0/A to 650.0 set slew limit on dcd_ilc.reg_n.lat_1/A to 650.0 set slew limit on
slow_mode_blk.reg_n.lat_0/A to 650.0 set slew limit on op_cmp_44.reg_n.lat_0/A to 650.0 set slew limit
on op_cmp_dsbl.reg_n.lat_0/A to 650.0 set slew limit on eu_frc_milli.reg_n.lat_0/A to 650.0 set slew limit
on bcr_store_stat.reg_n.lat_0/A to 650.0 set slew limit on exc_info.reg_n.lat_0/A to 650.0 set slew limit on
exc_info.reg_n.lat_1/A to 650.0 set slew limit on exc_info.reg_n.lat_2/A to 650.0 set slew limit on
exc_info.reg_n.lat_3/A to 650.0 set slew limit on slow_mode.clockblock_4/clka to 650.0 set load limit on
slow_mode.clockblock_4/a_clk to 10000.0 set slew limit on a_clk to 650.0 set slew limit on
slow_mode.clockblock/a_clk to 650.0 set slew limit on slow_mode.clockblock_1/a_clk to 650.0 set slew
limit on slow_mode.clockblock_2/a_clk to 650.0 set slew limit on slow_mode.clockblock_3/a_clk to 650.0
set slew limit on slow_mode.clockblock_4/a_clk to 650.0 set slew limit on slow_mode.clockblock_5/a_clk
to 650.0 set load limit on slow_mode.clockblock_4/b_clk to 10000.0 set slew limit on b_clk to 650.0 set
slew limit on slow_mode.clockblock/b_clk to 650.0 set slew limit on slow_mode.clockblock_1/b_clk to
650.0 set slew limit on slow_mode.clockblock_2/b_clk to 650.0 set slew limit on
slow_mode.clockblock_3/b_clk to 650.0 set slew limit on slow_mode.clockblock_4/b_clk to 650.0 set slew
limit on slow_mode.clockblock_5/b_clk to 650.0 set load limit on slow_mode.clockblock_4/clkg to 10000.0
set slew limit on clkg2 to 650.0 set slew limit on slow_mode.clockblock_3/clkg to 650.0 set slew limit on
slow_mode.clockblock_4/clkg to 650.0 set slew limit on slow_mode.clockblock_5/clkg to 650.0 set load
limit on slow_mode.clockblock_4/scan_enable to 10000.0 set slew limit on scan_enable to 650.0 set slew
limit on slow_mode.clockblock/scan_enable to 650.0 set slew limit on
slow_mode.clockblock_1/scan_enable to 650.0 set slew limit on slow_mode.clockblock_2/scan_enable to
de.clockblock_4/scan_enable to 650.0 set slew limit on slow_mode.clockblock_5/scan_enable to 650.0
set load limit on slow_mode.clockblock_4/clkl_mode4 to 10000.0 set slew limit on gptr_latch/clkl_mode4
to 650.0 set slew limit on slow_mode.clockblock/clkl_mode4 to 650.0 set slew limit on
slow_mode.clockblock_1/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode4 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode4 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode4 to
650.0 set load limit on slow_mode.clockblock_4/clkl_mode5 to 10000.0 set slew limit on
gptr_latch/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode5 to 650.0 set slew limit
on slow_mode.clockblock_1/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode5 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode5 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode5 to
650.0 set load limit on slow_mode.clockblock_4/clkl_mode6 to 10000.0 set slew limit on
gptr_latch/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode6 to 650.0 set slew limit
on slow_mode.clockblock_1/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode6 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode6 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode6 to
650.0 set load limit on slow_mode.clockblock_4/clkl_mode7 to 10000.0 set slew limit on clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock/clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock_1/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode7 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode7 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode7 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode7 to
650.0 set load limit on slow_mode.clockblock_4/clkl_mode8 to 10000.0 set slew limit on
gptr_latch/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode8 to 650.0 set slew limit
on slow_mode.clockblock_1/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode8 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode8 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode8 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode8 to
650.0 set load limit on slow_mode.clockblock_4/test_c1 to 10000.0 set slew limit on test_c1 to 650.0 set
```

```
slew limit on slow_mode.clockblock/test_c1 to 650.0.set slew limit on slow_mode.clockblock_1/test_c1 to
650.0 set slew limit on slow_mode.clockblock_2/test_c1 to 650.0 set slew limit on
slow_mode.clockblock_3/test_c1 to 650.0 set slew limit on slow_mode.clockblock_4/test_c1 to 650.0 set
slew limit on slow_mode.clockblock_5/test_c1 to 650.0 slow_mode.clockblock_5 cb_clk_32_1 set load
limit on slow mode.clockblock 5/c1 to 10000.0 set slew limit on spare.reg_n.lat_0/C1 to 650.0 set slew
limit on mcset_e1.reg_n.lat_0/C1 to 650.0 set slew limit on eu_iu_spare.reg_n.lat_0/C1 to 650.0 set slew
limit on dsbl ovrlp blk.reg n.lat 0/C1 to 650.0 set slew limit on inst_fetch.reg_n.lat_0/C1 to 650.0 set
slew limit on iu_dsbl_ovrlp.req_n.lat_0/C1 to 650.0 set slew limit on ex_in_prog.reg_n.lat_0/C1 to 650.0
set slew limit on blk_dcd.reg_n.lat_0/C1 to 650.0 set slew limit on blk_dcd.reg_n.lat_1/C1 to 650.0 set
slew limit on blk_dcd.reg_n.lat_2/C1 to 650.0 set slew limit on blk_dcd.reg_n.lat_3/C1 to 650.0 set slew
limit on dcd_succ_dly.reg_n.lat_0/C1 to 650.0 set slew limit on exec_recov.reg_n.lat_0/C1 to 650.0 set
slew limit on ru_updt_dly.reg_n.lat_0/C1 to 650.0 set slew limit on slow_mode.clockblock_5/c1 to 650.0
set load limit on slow_mode.clockblock_5/c2 to 10000.0 set slew limit on spare.reg_n.lat_0/B to 650.0 set
slew limit on mcset_e1.reg_n.lat_0/B to 650.0 set slew limit on eu_iu_spare.reg_n.lat_0/B to 650.0 set
.0 set slew limit on iu_dsbl_ovrlp.reg_n.lat_0/B to 650.0 set slew limit on ex_in_prog.reg_n.lat_0/B to
650.0 set slew limit on blk_dcd.reg_n.lat_0/B to 650.0 set slew limit on blk_dcd.reg_n.lat_1/B to 650.0 set
slew limit on blk_dcd.reg_n.lat_2/B to 650.0 set slew limit on blk_dcd.reg_n.lat_3/B to 650.0 set slew limit
on dcd_succ_dly.req_n.lat_0/B to 650.0 set slew limit on exec_recov.reg_n.lat_0/B to 650.0 set slew limit
on ru updt dly.reg n.lat 0/B to 650.0 set slew limit on slow_mode.clockblock_5/c2 to 650.0 set load limit
on slow_mode.clockblock_5/clka to 10000.0 set slew limit on spare.reg_n.lat_0/A to 650.0 set slew limit
on mcset_e1.reg_n.lat_0/A to 650.0 set slew limit on eu_iu_spare.reg_n.lat_0/A to 650.0 set slew limit on
dsbl_ovrlp_blk.reg_n.lat_0/A to 650.0 set slew limit on inst_fetch.reg_n.lat_0/A to 650.0 set slew limit on
iu dsbl ovrlp.reg n.lat 0/A to 650.0 set slew limit on ex_in_prog.reg_n.lat_0/A to 650.0 set slew limit on
blk_dcd.reg_n.lat_0/A to 650.0 set slew limit on blk_dcd.reg_n.lat_1/A to 650.0 set slew limit on
blk_dcd.reg_n.lat_2/A to 650.0 set slew limit on blk_dcd.reg_n.lat_3/A to 650.0 set slew limit on
dcd succ dly.req_n.lat_0/A to 650.0 set slew limit on exec_recov.reg_n.lat_0/A to 650.0 set slew limit on
ru updt dly.reg n.lat 0/A to 650.0 set slew limit on slow_mode.clockblock_5/clka to 650.0 set load limit
on slow mode.clockblock 5/a clk to 10000.0 set slew limit on a_clk to 650.0 set slew limit on
slow_mode.clockblock/a_clk to 650.0 set slew limit on slow_mode.clockblock_1/a_clk to 650.0 set slew
limit on slow_mode.clockblock_2/a_clk to 650.0 set slew limit on slow_mode.clockblock_3/a_clk to 650.0
set slew limit on slow mode.clockblock_4/a_clk to 650.0 set slew limit on slow_mode.clockblock_5/a_clk
to 650.0 set load limit on slow_mode.clockblock_5/b_clk to 10000.0 set slew limit on b_clk to 650.0 set
slew limit on slow_mode.clockblock/b_clk to 650.0 set slew limit on slow_mode.clockblock_1/b_clk to
650.0 set slew limit on slow_mode.clockblock_2/b_clk to 650.0 set slew limit on
slow mode.clockblock 3/b clk to 650.0 set slew limit on slow_mode.clockblock_4/b_clk to 650.0 set slew
limit on slow_mode.clockblock_5/b_clk to 650.0 set load limit on slow_mode.clockblock_5/clkg to 10000.0
set slew limit on clkq2 to 650.0 set slew limit on slow_mode.clockblock_3/clkg to 650.0 set slew limit on
slow mode.clockblock 4/clkg to 650.0 set slew limit on slow_mode.clockblock_5/clkg to 650.0 set load
limit on slow_mode.clockblock_5/scan_enable to 10000.0 set slew limit on scan_enable to 650.0 set slew
limit on slow mode.clockblock/scan enable to 650.0 set slew limit on
slow mode.clockblock_1/scan_enable to 650.0 set slew limit on slow_mode.clockblock_2/scan_enable to
650.0 set slew limit on slow mode.clockblock 3/scan enable to 650.0 set slew limit on
slow_mode.clockblock_4/scan_enable to 650.0 set slew limit on slow_mode.clockblock_5/scan_enable to
650.0 set load limit on slow_mode.clockblock_5/clkl_mode4 to 10000.0 set slew limit on
gptr_latch/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode4 to 650.0 set slew limit
on slow_mode.clockblock_1/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode4 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode4 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode4 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode4 to
650.0 set load limit on slow_mode.clockblock_5/clkl_mode5 to 10000.0 set slew limit on
aptr latch/clkl mode5 to 650.0 set slew limit on slow mode.clockblock/clkl_mode5 to 650.0 set slew limit
on slow_mode.clockblock_1/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_2/clkl_mode5 to
650.0 set slew limit on slow_mode.clockblock_3/clkl_mode5 to 650.0 set slew limit on
slow_mode.clockblock_4/clkl_mode5 to 650.0 set slew limit on slow_mode.clockblock_5/clkl_mode5 to
650.0 set load limit on slow_mode.clockblock_5/clkl_mode6 to 10000.0 set slew limit on
gptr_latch/clkl_mode6 to 650.0 set slew limit on slow_mode.clockblock/clkl_mode6 to 650.0 set slew limit
```

\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode6 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode6 to 650.0 set load limit on slow\_mode.clockblock\_5/clkl\_mode7 to 10000.0 set slew limit on clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode7 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode7 to 650.0 set load limit on slow\_mode.clockblock\_5/clkl\_mode8 to 10000.0 set slew limit on gptr\_latch/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_1/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_2/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_3/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_4/clkl\_mode8 to 650.0 set slew limit on slow\_mode.clockblock\_5/clkl\_mode8 to 650.0 set load limit on slow\_mode.clockblock\_5/test\_c1 to 10000.0 set slew limit on test\_c1 to 650.0 set slew limit on slow\_mode.clockblock/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_1/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_2/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_3/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_4/test\_c1 to 650.0 set slew limit on slow\_mode.clockblock\_5/test\_c1 to 650.0 > libanal\_hide -library CC8S libanal\_unhide -design /CC8S/cs invvn\* > libanal\_unhide -design /CC8S/cs\_nnd2n\* > libanal\_unhide -design /CC8S/cs\_nnd3n\* > libanal\_unhide -design /CC8S/cs\_nnd4n\* > libanal\_unhide -design /CC8S/cs nor2n\* > libanal\_unhide -design /CC8S/cs\_nor3n\* > libanal\_unhide -design /CC8S/cs ao12n\* > libanal\_unhide -design /CC8S/cs\_ao22n\* > libanal\_unhide -design /CC8S/cs\_oa21n\* > libanal\_unhide -design /CC8S/cs\_oa22n\* > libanal\_unhide -design /CC8S/cs invvn\* > libanal\_unhide -design /CC8S/cs\_xbn2n\* > libanal\_unhide -design /CC8S/cs xbo2n\* > libanal\_build -library CC8S -slibrary SIZELESS [ET-0203]:Timing top level created for design: def\_proto, analysis mode: default. libanal\_model -library SIZELESS -clus\_ratio -clus\_move -... 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model_prim: Using inverter cs_invvn01c_sl: delay=52.23 slew=70.09 load=5.67
                          > load_units -femto 42.0
                                                            > time_units -pico -value 100
set_prim_mode 1
create pseudo reg -library CC8S -register cl invvn05d -i...
                                                                   > echo {=== Finish libanal ===} ===
                       > echo SYNZ_READY SYNZ_READY SYNZPROMPT
Finish libanal ===
□[10Cif { [ catch { ; puts "***** start Synzilla: ltc == $CTE::run_synzilla_ltc, mask_groups ==
$CTE::synzilla mask group";; observe -ci; source cte_setup_timer.tcl; source cte_set_rc.tcl;;
CTE::cte_setup_timer;; opt_and_map $CTE::synzilla_mask_group DEFAULT $CTE::run_synzilla_ltc
$CTE::synzilla_complex_regs; puts "***** end Synzilla *****"; } result ] } { exit } ***** start Synzilla: Itc
== 0, mask groups == 0
                            > observe -ci
                                              > source cte_setup_timer.tcl Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_setup_timer.tcl
cte_set_rc.tcl Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_set_rc.tcl
> read timer parms -file /afs/apd/func/vlsi/alliance00/tim... ICM-015 I: >Begin...Parm Reader
                                                                                                     for
file /afs/apd/func/vlsi/alliance00/timing/parms/cpsynz.parms. ICM-016 I: <End.....Parm Reader.
                                        > set_slew_propagation -propagated
                                                                                      > set timer parm
> set_cap_limit_calc -type_zero
-name netcalc.net-delay-mode -value no-rcest [ET-1737]: The parameter 'netcalc.net-delay-mode' could
                     Use command 'create_timer_parm' to create parameter. {setting nominal delay
not be located.
                                                   > set vdd -vdd best 1.7 -vdd worst 1.45
               > set delay mode -nominal
mode}
                          > set temp -temp best -10 -temp_worst 10 -temp_nominal 10
-vdd nominal 1.45
hide clock tree [ET-0601]: The model build for block: gptr_latch, cell name: cb_mode_block failed.
                                                                          > read phase_file -file
Default modelling will be used for this block. 0 gates were hidden.
/afs/apd/func/vlsi/alliance00/bscc... [ET-0018]:>Begin...PHASE reader
/afs/apd/func/vlsi/alliance00/bscc8/v4/ndr/a00.phase. [ET-0019]:<End.....PHASE reader.
                                                                                                      >
set default slew-slew 151 Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/synzFuncs.tcl
                                                                                  > set_load_limit -cap
                                                > set load limit -cap 1001 -ports {iu_eu_opcode_cmp
141 -ports {op_dsbl_after eu_iu_spar...
                 > read_assertions -path /afs/apd/func/vlsi/alliance00/timi... [ET-0018]:>Begin...PIS
iu_rcv...
               for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pis.
reader
[ET-0016]:Pin/Net: aa blk dcd prtl not found on line no: 31. [ET-0016]:Pin/Net: clkg0 not found on line
no: 132. [ET-0016]:Pin/Net: clkg 0 not found on line no: 133. [ET-0016]:Pin/Net: clkg_00 not found on
in/Net: clkq1 not found on line no: 135. [ET-0016]:Pin/Net: clkq_1 not found on line no: 136.
[ET-0016]:Pin/Net: clkg_01 not found on line no: 137. [ET-0016]:Pin/Net: clkg_2 not found on line no:
139. [ET-0016]:Pin/Net: clkg_02 not found on line no: 140. [ET-0016]:Pin/Net: clkg3 not found on line no:
141. [ET-0016]:Pin/Net: clkg_3 not found on line no: 142. [ET-0016]:Pin/Net: clkg_03 not found on line
```

```
no: 143. [ET-0016]:Pin/Net: clkg4 not found on line no: 144. [ET-0016]:Pin/Net: clkg_4 not found on line
no: 145. [ET-0016]:Pin/Net: clkg_04 not found on line no: 146. [ET-0016]:Pin/Net: clkg5 not found on line
no: 147. [ET-0016]:Pin/Net: clkg_5 not found on line no: 148. [ET-0016]:Pin/Net: clkg_05 not found on
line no: 149. [ET-0016]:Pin/Net: clkg6 not found on line no: 150. [ET-0016]:Pin/Net: clkg_6 not found on
line no: 151. [ET-0016]:Pin/Net: clkg_06 not found on line no: 152. [ET-0016]:Pin/Net: clkg7 not found on
line no: 153. [ET-0016]:Pin/Net: clkg_7 not found on line no: 154. [ET-0016]:Pin/Net: clkg_07 not found
on line no: 155. [ET-0016]:Pin/Net: clkg8 not found on line no: 156. [ET-0016]:Pin/Net: clkg_8 not found
on line no: 157. [ET-0016]:Pin/Net: clkg_08 not found on line no: 158. [ET-0016]:Pin/Net: clkg9 not found
on line no: 159. [ET-0016]:Pin/Net: clkg_9 not found on line no: 160. [ET-0016]:Pin/Net: clkg_09 not
found on line no: 161. [ET-0016]:Pin/Net: clkg11 not found on line no: 162. [ET-0016]:Pin/Net: clkg22 not
found on line no: 163. [ET-0016]:Pin/Net: clkg33 not found on line no: 164. [ET-0019]:<End.....PIS
              [ET-0018]:>Begin...ETA reader
                                                     for file
/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.eta. [ET-0019]:<End.....ETA reader.
[ET-0018]:>Begin...POS reader
                                       for file
/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pos. [ET-0019]:<End.....POS reader.
> hnl::all inputs
                          > get_asserted_phases -pin op_dsbl_after -at
get_asserted_phases -pin eu_iu_spare1 -at
                                                     > get_asserted_phases -pin second op lat -at
> get_asserted_phases -pin mcr41_trap -at
                                                    > get_asserted_phases -pin ifet_xcptn -at
> get_asserted_phases -pin iu_eu_xcpt_pend -at
                                                          > get_asserted_phases -pin ig_blk_d1 -at
> get_asserted_phases -pin clkl_mode7 -at Pin: NO PHASES for clkl_mode7: asserting default C3+R
> set_arrival -time 401 -phase C3+R -ports clkl_mode7 -late
                                                                      > set_arrival -time 101 -phase
C3+R -ports clkl_mode7 -early
                                        > get_asserted_phases -pin dcd_op 44 -at
get_asserted_phases -pin ru_write_in_iq -at
                                                     > get_asserted_phases -pin a_clk -at Pin: NO
PHASES for a_clk: asserting default C3+R
                                                     > set_arrival -time 401 -phase C3+R -ports a clk
-late
                > set_arrival -time 101 -phase C3+R -ports a_clk -early
                                                                               > get_asserted phases
-pin b_clk -at Pin: NO PHASES for b_clk: asserting default C3+R
                                                                           > set_arrival -time 401
-phase C3+R -ports b clk -late
                                         > set_arrival -time 101 -phase C3+R -ports b_clk -early
> get_asserted_phases -pin ru_iu_rcvy_rst -at
                                                       > get_asserted_phases -pin
eu_iu_enter_slow md -at
                                   > get_asserted_phases -pin id_instr_stores -at
qet_asserted_phases -pin op_inq_stores -at
                                                     > get_asserted_phases -pin test_c1 -at Pin: NO
PHASES for test_c1: asserting default C3+R
                                                       > set_arrival -time 401 -phase C3+R -ports
test_c1 -late
                       > set_arrival -time 101 -phase C3+R -ports test_c1 -early
get_asserted_phases -pin iq_blk_aa -at
                                                 > get_asserted_phases -pin aa ofc available -at
> get_asserted_phases -pin eu_iu_mmode -at
                                                       > get_asserted_phases -pin eu_iu_mcset_e1 -at
_asserted_phases -pin ru_98_43 -at
                                             > get_asserted_phases -pin srlz_op_match -at
get_asserted_phases -pin first_op_lat -at
                                                  > get_asserted_phases -pin zero branches -at
> get_asserted_phases -pin dcd mcr41 blk -at
                                                        > get_asserted_phases -pin xu_iu_xlat busy
             > get_asserted_phases -pin du_iu_hold_aa_req -at
-at
                                                                        > get_asserted_phases -pin
eu_iu fpu end op -at
                               > get_asserted_phases -pin eu_iu_misc_hold -at
get_asserted_phases -pin op_cmp_raw -at
                                                    > get_asserted_phases -pin op_dsbl_before -at
> get_asserted_phases -pin op_drain -at
                                                 > get_asserted_phases -pin eu_iu_fxu_end_op -at
> get_asserted_phases -pin op mcend raw -at
                                                        > get_asserted_phases -pin eu_iu_br_wrong
             > get_asserted_phases -pin need_opnd_req -at
-at
                                                                     > get_asserted_phases -pin
legal bht br-at
                         > get_asserted_phases -pin clkg -at
                                                                      > get_asserted_phases -pin
bht_branch_req -at Pin: NO PHASES for bht_branch_req: asserting default C3+R
set_arrival -time 401 -phase C3+R -ports bht_branch_req ...
                                                                     > set_arrival -time 101 -phase
C3+R -ports bht_branch_req ...
                                        > get_asserted_phases -pin id_ex_in_mm -at
get_asserted_phases -pin du_iu_quiesced -at
                                                      > get_asserted_phases -pin iu_op_cmp_hit_a -at
> get_asserted_phases -pin iu_op cmp hit b -at
                                                          > get_asserted_phases -pin iu_op_cmp_hit_c
            > get_asserted_phases -pin iu_op_cmp_hit_d -at
                                                                      > get_asserted_phases -pin
dcd_frc_milli -at
                         > get_asserted_phases -pin iq_empty -at
                                                                           > get_asserted_phases
-pin op serialize -at
                             > get_asserted_phases -pin gptr_scan_in -at Pin: NO PHASES for
gptr_scan_in: asserting default C3+R
                                                > set_arrival -time 401 -phase C3+R -ports
gptr scan in -late
                            > set_arrival -time 101 -phase C3+R -ports gptr_scan_in -e...
qet_asserted_phases -pin aa_agi_lat -at
                                                 > get_asserted_phases -pin branch_request -at
```

```
> get_asserted_phases -pin ru_9a_52 -at
                                                  > get_asserted_phases -pin bu_iu_quiesced -at
                                                       > get_asserted_phases -pin op_eim_dcd -at
> get_asserted_phases -pin dcd_blk_dsucc -at
                                                             > get_asserted_phases -pin scan_in -at
> get_asserted_phases -pin iqmcode_mod_390gr -at
                                                               > set_arrival -time 401 -phase C3+R
Pin: NO PHASES for scan_in: asserting default C3+R
                              > set arrival -time 101 -phase C3+R -ports scan in -early
-ports scan_in -late
get asserted phases -pin eu_iu_e1_exc_cond -at
                                                          > get_asserted_phases -pin
                              > get_asserted_phases -pin eu_iu_fpu_excpn -at
aa ofc block reg -at
get_asserted_phases -pin block_aa_branch -at
                                                       > get_asserted_phases -pin ru_iu_rq_blk -at
                                                        > get_asserted_phases -pin ireg_valid -at
> get_asserted_phases -pin op_chkpt_synch -at
                                                  > get_asserted_phases -pin three_branches -at
> get_asserted_phases -pin ru_9a_36 -at
> get_asserted_phases -pin bht_block_dcd -at Pin: NO PHASES for bht_block_dcd: asserting default
                                                                                        > set_arrival
                 > set arrival -time 401 -phase C3+R -ports bht_block_dcd -...
C3+R
                                                        > get asserted phases -pin ru 9a 20 -at
-time 101 -phase C3+R -ports bht_block_dcd -...
                                                            > get asserted phases -pin gptr a clk -at
> get_asserted_phases -pin iu_eu_data_blocked -at
                                                                  > set_arrival -time 401 -phase C3+R
Pin: NO PHASES for gptr_a_clk: asserting default C3+R
> get_asserted_phases -pin gptr_b_clk -at Pin: NO PHASES for gptr_b_clk: asserting default C3+R
                                                                    > set arrival -time 101 -phase
> set arrival -time 401 -phase C3+R -ports gptr_b_clk -late
                                      > get_asserted_phases -pin op_is_44 -at
C3+R -ports aptr b clk -early
                                                  > get_asserted_phases -pin clkg2 -at
get_asserted_phases -pin inst_fetches -at
get_asserted_phases -pin eu_iu_fxu_exc_cond -at
                                                          > get_asserted_phases -pin ru_9a_04 -at
                                                      > get_asserted_phases -pin scan_enable -at
> get_asserted_phases -pin br_wrong_targ -at
> get_asserted_phases -pin du_iu_store_status(0) -at
                                                             > get_asserted_phases -pin
                                  > get_asserted_phases -pin du_iu_store_status(2) -at
                                                                                                >
du_iu_store_status(1) -at
get asserted_phases -pin eu_iu_srlz_op_actn(0) -at
                                                            > get_asserted_phases -pin
                                   > get_asserted_phases -pin ru_9a_0001(0) -at
eu iu srlz_op_actn(1) -at
get_asserted_phases -pin ru_9a_0001(1) -at
                                                     > get_asserted_phases -pin ireg_0_1(0) -at
                                                   > get_asserted_phases -pin num_dcd_cyl(0) -at
> get asserted_phases -pin ireg_0_1(1) -at
> get_asserted_phases -pin num_dcd_cyl(1) -at
                                                        > get asserted phases -pin ru_9a_3233(32)
                                                                     > get_asserted_phases -pin
             > get_asserted_phases -pin ru_9a_3233(33) -at
                                   > get_asserted_phases -pin eu_iu_interrupt_info(1) -at
eu iu interrupt_info(0) -at
                                                            > get_asserted_phases -pin
get_asserted_phases -pin eu_iu_interrupt_info(2) -at
                                   > get_asserted_phases -pin ru_9a_1617(16) -at
eu_iu_interrupt_info(3) -at
                                                      > get_asserted_phases -pin
get_asserted_phases -pin ru_9a_1617(17) -at
eu_iu_srlz_op_encode(0) -at
                                      > get_asserted_phases -pin eu_iu_srlz_op_encode(1) -at
                                                                 > get_asserted_phases -pin
> get_asserted_phases -pin eu_iu_srlz_op_encode(2) -at
                                      > get_asserted_phases -pin eu_iu_srlz_op_encode(4) -at
eu iu srlz op encode(3) -at
                                                                 > get_asserted_phases -pin
> get asserted_phases -pin eu_iu_srlz_op_encode(5) -at
                                      > get_asserted_phases -pin eu_iu_srlz_op_encode(7) -at
eu iu srlz op encode(6) -at
                                                                 > get asserted_phases -pin
> get asserted phases -pin eu iu srlz op encode(8) -at
                                      > get asserted_phases -pin eu_iu_srlz_op_encode(10) -at
eu iu srlz op encode(9) -at
> get asserted phases -pin eu_iu_srlz_op_encode(11) -at
                                                                  > get_asserted_phases -pin
                             > get_asserted_phases -pin ru_9a_4849(49) -at
ru_9a_4849(48) -at
                                                    > get_asserted_phases -pin ireg_1631(23) -at
get_asserted_phases -pin ireg_1631(22) -at
> get_asserted_phases -pin ireg_1631(24) -at
                                                      > get_asserted_phases -pin ireg_1631(25) -at
                                                      > get_asserted_phases -pin ireg_1631(27) -at
> get_asserted_phases -pin ireg_1631(26) -at
                                                      > get_asserted_phases -pin ireg_1631(29) -at
> get_asserted_phases -pin ireg_1631(28) -at
                                                     > hnl::all_outputs
> get asserted phases -pin ireg 1631(30) -at
get_asserted_phases -pin iu_eu_opcode_cmp -rat
                                                          > get_asserted_phases -pin iu_rcvry_reset
                                                                    > get_asserted_phases -pin
              > get_asserted_phases -pin iu_reset_op_c -rat
dcd_succ_last_t1 -rat Pin: NO PHASES for dcd_succ_last_t1:
                                                                        > set_required -time 999
-phase C3+R -ports dcd_succ_last_...
                                                > set_required -time -999 -phase C3+R -ports
                          > get_asserted_phases -pin iu_milli_mode -rat
dcd_succ_last...
     > set_required -time 999 -phase C3+R -ports iu_reset_op_c_...
                                                                             > set_required -time -999
                                             > get_asserted_phases -pin dcd_succ_last -rat
-phase C3+R -ports iu_reset_op_c...
                                                            > get_asserted_phases -pin
> get_asserted_phases -pin iu_eu_op_nomatch -rat
```

```
ds_1st_maybe -rat
                             > get_asserted_phases -pin id_xcute_targ -rat
get_asserted_phases -pin xc_frc_ia_to_if_t1 -rat
                                                          > get_asserted_phases -pin dcd_success_tr
              > get_asserted_phases -pin dsucc_or_agi_n -rat
                                                                        > get_asserted_phases -pin
dsucc_or_agi -rat
                            > get_asserted_phases -pin iu_slow_mode -rat
get_asserted_phases -pin slwmd_blk_n -rat
                                                     > get_asserted_phases -pin xc_frc_milli -rat
> get_asserted_phases -pin dcd_succ_first t1 -rat
                                                           > get_asserted_phases -pin iu_reset_all -rat
> get_asserted_phases -pin iu_milli_mode_t1 -rat
                                                          > get_asserted_phases -pin
iu_milli_mode_t2 -rat
                               > get_asserted_phases -pin iu_milli_mode_t3 -rat
get_asserted_phases -pin xc_frc_milli_t1 -rat
                                                      > get_asserted_phases -pin iu_exc_cond -rat
> get_asserted_phases -pin slow_mode_tr -rat
                                                        > get_asserted_phases -pin iu_eu_slow_mode
              > get_asserted_phases -pin dcd_success -rat
                                                                    > get_asserted_phases -pin
iu_milli_mode_tr -rat
                              > get_asserted_phases -pin iu_reset_if -rat
get_asserted_phases -pin exc_cond tr -rat
                                                    > get_asserted_phases -pin dcd_succ_first -rat
> get_asserted_phases -pin execute_recovery -rat
                                                           > get_asserted_phases -pin execute_xcptn
              > get_asserted_phases -pin xc_frc_ia_to_if -rat
                                                                      > get_asserted_phases -pin
iu_slow_mode_t1 -rat Pin: NO PHASES for iu_slow_mode_t1:
                                                                         > set_required -time 999
-phase C3+R -ports iu_slow_mode_t...
                                                 > set_required -time -999 -phase C3+R -ports
iu_slow_mode_...
                           > get_asserted_phases -pin gptr_scan_out -rat Pin: NO PHASES for
gptr scan out:
                           > set_required -time 999 -phase C3+R -ports gptr_scan_out ...
set_required -time -999 -phase C3+R -ports gptr_scan_out...
                                                                     > get_asserted_phases -pin
iu reset fst -rat
                          > get_asserted_phases -pin scan_out -rat Pin: NO PHASES for scan_out:
> set_required -time 999 -phase C3+R -ports scan_out -late
                                                                     > set_required -time -999 -phase
C3+R -ports scan out -early
                                      > get_asserted_phases -pin iu_eu_dcd_succ_tr -rat
get_asserted_phases -pin idcdsuc_err -rat Pin: NO PHASES for idcdsuc_err:
                                                                                       > set required
-time 999 -phase C3+R -ports idcdsuc_err -late
                                                         > set_required -time -999 -phase C3+R -ports
                         > get_asserted_phases -pin frc_milli -rat
idcdsuc err -...
                                                                          > get_asserted_phases -pin
iu_intrupt_info(0) -rat
                               > get_asserted_phases -pin iu_intrupt_info(1) -rat
get_asserted_phases -pin iu_intrupt_info(2) -rat
                                                        > get_asserted_phases -pin iu_intrupt_info(3)
              > get_asserted_phases -pin blk_dcd_info_tr(0) -rat
-rat
                                                                         > get_asserted_phases -pin
blk_dcd_info_tr(1) -rat
                                > get_asserted_phases -pin blk_dcd_info_tr(2) -rat
get_asserted_phases -pin blk_dcd_info_tr(3) -rat
                                                         > get_asserted_phases -pin
iu_srlz_op_encode(0) -rat
                                   > get_asserted_phases -pin iu_srlz_op_encode(1) -rat
                                                                                                 >
get_asserted_phases -pin iu_srlz_op_encode(2) -rat
                                                             > get_asserted_phases -pin
iu_srlz_op_encode(3) -rat
                                   > get_asserted_phases -pin iu_srlz_op_encode(4) -rat
                                                                                                 >
-pin iu_srlz_op_encode(6) -rat
                                        > get_asserted_phases -pin iu_srlz_op_encode(7) -rat
> get_asserted_phases -pin iu_srlz_op_encode(8) -rat
                                                              > get_asserted_phases -pin
iu_srlz_op_encode(9) -rat
                                   > get_asserted_phases -pin iu_srlz_op_encode(10) -rat
                                                                                                  >
get_asserted_phases -pin iu_srlz_op_encode(11) -rat
                                                              > get_asserted_phases -pin
decode ilc(0) -rat
                           > get_asserted_phases -pin decode_ilc(1) -rat
get_asserted_phases -pin srlz_actn_tr(0) -rat
                                                      > get_asserted_phases -pin srlz actn tr(1) -rat
> get_asserted_phases -pin intrpt_info_tr(0) -rat
                                                        > get_asserted_phases -pin intrpt info tr(1)
-rat
             > get_asserted_phases -pin intrpt_info_tr(2) -rat
                                                                      > get_asserted_phases -pin
intrpt_info_tr(3) -rat
                             > get_asserted_phases -pin op_44_info_tr(0) -rat
get_asserted_phases -pin op_44_info_tr(1) -rat
                                                       > get_asserted_phases -pin dcd_c_cnt(0) -rat
> get_asserted_phases -pin dcd_c_cnt(1) -rat
                                                     > read dcadi file -file
/afs/apd/func/vlsi/alliance00/bscc... [ET-0018]:>Begin...ETE DCADJ reader
                                                                                for file
/afs/apd/func/vlsi/alliance00/bscc8/v5/ndr/a00.dcadj. [ET-0019]:<End.....ETE DCADJ reader.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/main.tcl
hnl_idesign_get_name __CiType_13_30da5570
                                                      > use_pseudo_reg -idesign
 _CiType_13_30da5570 [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3,
analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
```

```
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
0 0 S 0 0 3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2 M IN 1 1 IN 0 0 0 S 0 0 3, analysis mode: SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting `
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]: Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode: SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
```

```
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below: [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
OW_CHIP, and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3,
analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0 3, analysis mode:SLOW CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP.
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting
timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: L1L2_M_IN_1_1_IN_0_0_0_S_0_0_3, analysis
mode:SLOW_CHIP, and below.
                                    > hnl_idesign_get_design __CiType_13_30da5570
hnl_design_get_library CiType 25 30e9d698
                                                  > hnl_library_get_name __CiType 23 30e9eb40
> echo {mask_group 0} mask_group 0 [hnl_attr]: Attributes registered for copy for type: PORT.
MASK_ANYTHING_MASKED_ON_PORT [hnl_attr]: Attributes registered for copy for type: CELL.
MASK_ANYTHING_MASKED_ON_CELL MASK_USER_CELL_NOCHANGE
SUGGESTED_LIBRARY_CELL SUGGESTED_PARALLEL_FANOUT SUGGESTED_SIZE
SUGGESTED_SWAP SYN_USAGE_BOX_HIDE [hnl_attr]: Attributes registered for copy for type: PIN.
MASK_ANYTHING_MASKED_ON_PIN MASK_USER_PIN_NOCHANGE
MASK_USER_PIN_NONEWNET SUGGESTED_SERIAL_FANOUT SYN_SAS_NAME [hnl attr]:
Attributes registered for copy for type: NET. MASK_ANYTHING_MASKED_ON_NET [hnl_attr]: 0 port(s)
have attribute(s) registered for copy. [hnl_attr]: 187 cell(s) have attribute(s) registered for copy. [hnl_attr]:
0 net(s) have attribute(s) registered for copy. [hnl_attr]: 2730 pin(s) have attribute(s) registered for copy.
> set_slew_propagation -estimate
                                     > cds continuous -fast
                                                                  > echo {=== Optimization
process ===} === Optimization process ===
                                               > pipo_buffer_insert [pipo_buffer]: Inserted 10
```

```
buffers Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/optz.tcl
freeze_net_loads -set -limit [TIMER-6412]: Asserted load on 369 inet(s).
                                                                          > ps Design
                                  1 instances 0 upcells
                                                         122 IN ports 73 OUT ports
/HISVHDL/IDCDSUC has:
801 cells (516 AND; 5 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                                0 buses
                                                                                2.71 pins per
                                              2770 pins (623 inversions)
1022 nets (0 multiply-driven; 0 undriven)
                                                                                 > ps Design
                                                         22 max fanout
           1675 literals 19 levels
                                  10 max fanin
net
                                              713 cells (433 AND; 0 XOR; 0 SEQ; 0 TRI; 280
           122 IN ports 73 OUT ports
pcells
                                              934 nets (0 multiply-driven; 0 undriven)
LINKED: 0 UNLINKED: 0 DC)
                                  0 buses
                                                         1597 literals 16 levels
                                                                                10 max fanin
                                  2.79 pins per net
2604 pins (608 inversions)
42 max fanout Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/custom_report.tcl
                                                              > ps -cell Design
> echo {Custom Synzilla Report} Custom Synzilla Report
                                                         122 IN ports 73 OUT ports
/HISVHDL/IDCDSUC has:
                                  1 instances 0 upcells
713 cells (433 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                                0 buses
                                              2604 pins (608 inversions)
                                                                                2.79 pins per
934 nets (0 multiply-driven; 0 undriven)
                                                         42 max fanout
                                                                                Cell
           1597 literals 16 levels
                                  10 max fanin
                       FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                                            0)
Information
                                                         cb clk_32_1 (ncount
                                                                                6: area
                (ncount 83: area
PSEUDO_REG
                                     0)
                       cb_mode_block (ncount 1: area
                                                         70)
                                                         Total Area = 570 (Comb = 20:
cs invvn01c_sl (ncount 10: area
                                  20)
                             > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550
             for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Report
Sun Apr 18 21:52:02 1999 Part : IDCDSUC Mode : Late Mode / Nominal
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
                        Max. Slack: 1.13427E+38 Sort Field: Slack
-1.13427E+38
                                     Abbreviation Comparison/Description ------
Endpoints: 2 Cause of Slack
                                                            Slack due to a point downstream on
                          Slack Continuation
                                                  SIkCont
  _____
                                        ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                              RAT
                               ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                              ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
Gating Setup
                   ClkGSet
                                                             ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                  ClkGHld
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                             CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                      Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                      Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        ClkPW
ClockPulseWidth
                                                     ( CLOCK1 ARRIVAL TIME + CLOCK
                                          ClkSep
TRAILING EDGE ) ClockSeparation
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                       ALTest
                                                                                  (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
           Slack discontinuity due to failed test
                                              Num/
ATLimit
                                           Delay/ Failed Test/ Test PinName
LimitedAT/
                                                   P Func T.Adj NetName
           AT Slack Slew CL FO Cell
E Phase
                                                                          2468 -1147
                    1 drain_blk.reg_n.lat_0/BASE_REG/a
                                                                 FC3+R
                                       39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
27 1 cl invvn
                      05d cl invvn05d
                                                         1200 c1 ---->
                    60 238 14 cl invvn
                                                05d
F C3-
         160
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                                            27 1 AND
                                                FC3+R
                                                          2468 -1147
                                                                                AND
                                      2516 -1147
                                                     0
                                                         21 1 AND
                                                                                        -48
                            R C3+R
/DELAY_ELEMENT/IN1
                                                                        21 1 PSEUDO_REG
                                                      2516 -1147
                                                                     0
a ----> drain_blk.reg_n.lat_0/a
                                            R C3+R
                 0 a ----> C89/OUT
                                                            R C3+R
                                                                      2516 -1147
                                                                                     0
                                                                                         21
PSEUDO_REG
                                                                         F C3+R
                                                                                   2463
                                         C89/IN1
                    AND
                             0 N89 ---->
1 AND
                                            52 drain_blk_in ---->{a}
         0 21 1 AND
                                    AND
-1147
                                               FC3+R 2463 -1147
                                                                           21 1 AND
M#2.EXPRESSION#104EXPR0/OUT
                                                                                    2307
          0 drain_blk_in ----> M#2.EXPRESSION#104EXPR0/IN1
                                                                          F C3+R
AND
                                            157 NET667 ---->{b} M#2.OR_VECT#3/OUT
         0 21 1 AND
                                    AND
 -1147
```

```
FC3+R 2307 -1147 0 21 1 AND
                                        AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 F C3+R 2046 -1147 0 21 1 AND
     261 drain_cond(8) ---->{c} M#2.EXPRESSION#103EXPR0/OUT
                                                               F C3+R 2046
-1147 0 21 1 AND AND 0 drain_cond(8) ---->
M#2.EXPREŞSION#103EXPR0/IN2 R C3+R 1941 -1147
                                    R C3+R 1941 -1147 0 37 2 AND
      104 stores_in_l2 ---->{d} M#2.EXPRESSION#94EXPR0/OUT
                                                             R C3+R 1941
-1147 0 37 2 AND AND 0 stores_in_l2 ----> M#2.EXPRESSION#94EXPR0/IN3 R C3+R 1784 -11
                                   R C3+R 1784 -1147 0 53 3 AND
AND 157 NET994 ---->{e} M#2.EXPRESSION#92EXPR2/OUT
                                                          R C3+R 1784
      0 53 3 AND AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2
F C3+R 1680 -1147 0 1222 7 AND AND 104 dcd_success ---->{f}
M#2.EXPRESSION#131EXPR0/OUT F C3+R 1680 -1147 0 1222 7 AND
AND 0 dcd_success ---> M#2.EXPRESSION#131EXPR0/IN1
                                                           F C3+R 1471
-1147 0 37 2 AND AND 209 slow_blks_s ---->{g}
M#2.EXPRESSION#124EXPR0/OUT F C3+R 1471 -1147
                                     F C3+R 1471 -1147 0 37 2 AND
     0 slow_blks_s ----> M#2.EXPRESSION#124EXPR0/IN1
                                                           R C3+R 1367
-1147 0 21 1 AND AND 104 NET749 ---->{h}
M#2.EXPRESSION#124EXPR1/OUT R C3+R 1367 -11
                                  R C3+R 1367 -1147 0 21 1 AND
     0 NET749 ---> M#2.EXPRESSION#124EXPR1/IN1 F C3+R 1262 -1147
0 21 1 AND AND 104 NET750 ---->{i} M#2.EXPRESSION#124EXPR2/OUT F C3+R 1262 -1147 0 21 1 AND AND 0 NET750 ---->
M#2.EXPRESSION#124EXPR2/IN1 F C3+R 1105 -1147 0 37 2 AND
                                   F C3+R 1105 -1147 0 37 2 AND
AND 157 medium_blks ---->{j} M#2.EXPRESSION#122EXPR0/OUT -1147 0 37 2 AND AND 0 medium_blks ---->
                                                              F C3+R 1105
M#2.EXPRESSION#122EXPR0/IN1
                                   FC3+R 949 -1147 0 37 2 AND
     157 quick_blks ---->{k} M#2.EXPRESSION#121EXPR0/OUT
                                                          FC3+R
                                                                    949
      0 37 2 AND AND 0 quick_blks ---->
M#2.EXPRESSION#121EXPR0/IN2
                                    R C3+R 792 -1147 0 37 2 AND
2 -1147 0 37 2 AND AND 0 insn_blk_dcd ---> M#2.EXPRESSION#82EXPR0/IN2 R C3+R 687 -1147
                                    R C3+R 687 -1147 0 21 1 AND
AND 104 NET689 ---->{m} M#2.EXPRESSION#82EXPR1/OUT
                                                         R C3+R 687
-1147 0 21 1 AND AND 0 NET689 ----> M#2.EXPRESSION#82EXPR1/IN1 R C3+R 583 -1147 110 31 2 AND AND 104 three_branches ---->
                                   AND 104 three_branches ----> .
             R C3+R 583 -1147 110 31 2 PI
three branches
0 three_branches
-
------ 2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2477 -1105 0
0 21 1 AND AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
R C3+R 2322 -1105 0 21 1 AND AND 0 NET667 ----> M#2.OR_VECT#3/IN9 R C3+R 2061 -1105 0 21 1 AND
     261 drain_cond(8) ---->{c} M#2.EXPRESSION#103EXPR0/OUT
                                                              RC3+R
AND 104 stores_in_l2 ---->{d} M#2.EXPRESSION#94EXPR0/OUT
                                                          F C3+R 1956
-1105
     0 37 2 AND AND 0 stores in 12 ---->
```

```
M#2.EXPRESSION#94EXPR0/IN3
                                            FC3+R 1799 -1105
                                                                        FC3+R
       157 NET994 ---->{e} M#2.EXPRESSION#92EXPR2/OUT
                                                                                 1799
AND
                                           0 NET994 ---> M#2.EXPRESSION#92EXPR2/IN2
                                   AND
-1105
            53 3 AND
                                                           104 dcd_success ---->{f}
         1695 -1105
                        0 1222 7 AND
                                                   AND
R C3+R
                                                       1695 -1105
                                                                      0 1222 7 AND
M#2.EXPRESSION#131EXPR0/OUT
                                             R C3+R
        0 dcd_success ---> M#2.EXPRESSION#131EXPR0/IN1
                                                                         RC3+R
                                                                                   1486
AND
                                          209 slow_blks_s ---->{g}
                                   AND
            37 2 AND
-1105
M#2.EXPRESSION#124EXPR0/OUT
                                             RC3+R
                                                       1486 -1105
                                                                         37 2 AND
                                                                         F C3+R
                                                                                  1382
        0 slow_blks_s ---> M#2.EXPRESSION#124EXPR0/IN1
AND
                    104 NET749 ---->{h} M#2.EXPRESSION#124EXPR1/OUT
            AND
                                                AND
                                                         0 NET749 ---->
       1382 -1105
                      0 21 1 AND
C3+R
                                                      1277 -1105
                                                                        21 1 AND
M#2.EXPRESSION#124EXPR1/IN1
                                            R C3+R
       104 NET750 ---->{i} M#2.EXPRESSION#124EXPR2/OUT
                                                                        R C3+R 1277
AND
                                   AND
                                           0 NET750 ---->
-1105
            21 1 AND
                                                                        37 2 AND
M#2.EXPRESSION#124EXPR2/IN1
                                            R C3+R
                                                      1120 -1105
       157 medium_blks ---->{j} M#2.EXPRESSION#122EXPR0/OUT
                                                                                      1120
                                                                            R C3+R
                                            0 medium_blks ---->
            37 2 AND
                                   AND
-1105
                                            R C3+R
                                                       964 -1105
                                                                    0
                                                                        37 2 AND
M#2.EXPRESSION#122EXPR0/IN1
       157 quick_blks ---->{k} M#2.EXPRESSION#121EXPR0/OUT
                                                                          RC3+R
                                                                                    964
AND
                                            0 quick_blks ---->
            37 2 AND
                                   AND
-1105
M#2.EXPRESSION#121EXPR0/IN2
                                                      807 -1105
                                                                    0
                                                                        37 2 AND
                                             FC3+R
        157 insn_blk_dcd ---->{I} M#2.EXPRESSION#82EXPR0/OUT
                                                                           FC3+R
                                                                                     807
AND
                                            0 insn_blk_dcd ---->
            37 2 AND
                                   AND
-1105
        0
                                                                       21 1 AND
M#2.EXPRESSION#82EXPR0/IN2
                                                      702 -1105
                                            FC3+R
        104 NET689 ---->{m} M#2.EXPRESSION#82EXPR1/OUT
                                                                        FC3+R
                                            0 NET689 ----> M#2.EXPRESSION#82EXPR1/IN1
                                   AND
-1105
            21 1 AND
                                                          104 three branches ---->
                                                  AND
                            31 2 AND
FC3+R
          598 -1105
                       81
                                                                                         0
                                  FC3+R
                                                              31 2 PI
                                            598 -1105
                                                         81
three_branches
three_branches
                            > report_area [ET-0413]:Using default pin capacitance 0.200000 for
boundary output pin iu_reset_op_c_t1. [ET-0027]:No subsequent messages of this type will be reported.
Increase timing debug level for complete set of these messages. [load_update]: Number of pin load
calculations: 83 since last stats [load_update]: Number of pin weight calculations: 0 since last stats
                                                                       > cputime Used 0.00
Design: /IDCDSUC - Area: 2731.154785, Area(Weight): 561.845093
                                                                 > pmove -cost 3 -dup -trace 0
cpu seconds or 00:00:00 wall time, used 0 bytes or 0 byte.
                                                                                > pmove
                                        > merge -cost 1 -dup -trace 0
> bmove -cost 4 -dup -trace 0
                                                                        > decomp -nand -ddi
                                > merge -cost 0 -dup -trace 0
-cost 0 -dup -trace 0
-dfi -no_xor Performing Circuit Decomposition for design IDCDSUC ... Performing NAND decomposition
...... Finished performing NAND decomposition NAND CPU time: 0.23 secs. NAND memory usage:
266240 bytes Performing DDI decomposition ... ... Finished performing DDI decomposition DDI CPU
time: 0.20 secs. DDI memory usage: 0 bytes Performing DFI decomposition ... ... Finished performing
DFI decomposition DFI CPU time: 0.07 secs. DFI memory usage: 0 bytes ....Finished Performing Circuit
Decomposition for design IDCDSUC Decomposition CPU time: 0.50 secs. Decomposition memory usage:
                          > merge -cost 0 -dup -trace 10 Merging Cella
266240 bytes
M#2.EXPRESSION#17EXPR0, Cellb C371, Cellc M#2.EXPRESSION#153EXPR1 Merging Cella
M#2.OR_VECT#2, Cellb C226, Cellc M#2.EXPRESSION#49EXPR1 Merging Cella
M#2.EXPRESSION#62EXPR4, Cellb C778, Cellc M#2.EXPRESSION#62EXPR3 Merging Cella
ella M#2.EXPRESSION#6EXPR0, Cellb C336, Cellc M#2.EXPRESSION#18EXPR1 Merging Cella
M#2.EXPRESSION#9EXPR0, Cellb C341, Cellc M#2.EXPRESSION#18EXPR2 Merging Cella
M#2.EXPRESSION#12EXPR0, Cellb C354, Cellc M#2.EXPRESSION#18EXPR3 Merging Cella
M#2.EXPRESSION#15EXPR0, Cellb C366, Cellc M#2.EXPRESSION#18EXPR4 Merging Cella
M#2.EXPRESSION#5EXPR0, Cellb C331, Cellc M#2.EXPRESSION#17EXPR1 Merging Cella
M#2.EXPRESSION#8EXPR0, Cellb C340, Cellc M#2.EXPRESSION#17EXPR2 Merging Cella
M#2.EXPRESSION#11EXPR0, Cellb C353, Cellc M#2.EXPRESSION#17EXPR3 Merging Cella
```

53 3 AND

```
M#2.EXPRESSION#14EXPR0, Cellb C364, Cellc M#2.EXPRESSION#17EXPR4 Merging Cella
M#2.EXPRESSION#114EXPR0, Cellb C498, Cellc M#2.EXPRESSION#124EXPR0 Merging Cella
M#2.EXPRESSION#90EXPR1, Cellb C713, Cellc M#2.EXPRESSION#90EXPR0 Merging Cella
M#2.EXPRESSION#125EXPR0, Cellb C432, Cellc M#2.EXPRESSION#134EXPR2 Merging Cella
M#2.EXPRESSION#123EXPR0, Cellb C415, Cellc M#2.EXPRESSION#125EXPR0 Merging Cella
M#2.EXPRESSION#126EXPR0, Cellb C438, Cellc M#2.EXPRESSION#132EXPR0 Merging Cella
M#2.EXPRESSION#107EXPR0, Cellb C705, Cellc M#2.EXPRESSION#108EXPR0 Merging Cella
M#2.EXPRESSION#88EXPR1, Cellb C339, Cellc M#2.EXPRESSION#88EXPR0 There were a total of 19
merge moves performed
                                      > fx_opt -s Number of connections before fx_opt: 1727
Number of connections after fx opt: 1540
                                                     > tgfs_redund -effort 100 -max_iteration 3
> pmove -cost 3 -dup -trace 0
                                          > bmove -cost 4 -dup -trace 0
-cost 1 -dup -trace 0
                                 > pmove -cost 0 -dup -trace 0
                                                                           > merge -cost 0 -dup
-trace 0
                     > decomp -nand -ddi -dfi -no_xor Performing Circuit Decomposition for design
IDCDSUC ... Performing NAND decomposition ... ... Finished performing NAND decomposition NAND
CPU time: 0.08 secs. NAND memory usage: 0 bytes Performing DDI decomposition ... ... Finished
performing DDI decomposition DDI CPU time: 0.00 secs. DDI memory usage: 0 bytes Performing DFI
decomposition ... ... Finished performing DFI decomposition DFI CPU time: 0.05 secs. DFI memory
usage: 0 bytes ... Finished Performing Circuit Decomposition for design IDCDSUC Decomposition CPU
time: 0.13 secs. Decomposition memory usage: 0 bytes
                                                                 > merge -cost 0 -dup -trace 10
Merging Cella C1114, Cellb C1175, Cellc M#2.EXPRESSION#77EXPR1 Merging Cella C1132, Cellb
C1190, Cellc M#2.EXPRESSION#85EXPR3 Merging Cella M#2.EXPRESSION#147EXPR2, Cellb C225,
Cellc C899 Merging Cella C1120, Cellb C1214, Cellc M#2.EXPRESSION#111EXPR7 Merging Cella
C1045, Cellb C1170, Cellc M#2.EXPRESSION#155EXPR1 Merging Cella
M#2.EXPRESSION#92EXPR0, Cellb C1283, Cellc M#2.EXPRESSION#169EXPR1 Merging Cella
M#2.EXPRESSION#94EXPR0, Cellb C1284, Cellc M#2.EXPRESSION#169EXPR2 Merging Cella
C1047, Cellb C1192, Cellc M#2.EXPRESSION#170EXPR0 Merging Cella C1126, Cellb C1230, Cellc
M#2.EXPRESSION#141EXPR1 Merging Cella C1155, Cellb C1356, Cellc M#2.EXPRESSION#6EXPR0
Merging Cella C1156, Cellb C1358, Cellc M#2.EXPRESSION#9EXPR0 Merging Cella C1157, Cellb
C1360, Cellc M#2.EXPRESSION#12EXPR0 Merging Cella C1158, Cellb C1362, Cellc
M#2.EXPRESSION#15EXPR0 Merging Cella C934, Cellb C1335, Cellc C1075 There were a total of 14
merge moves performed
                                      > fx_opt -s Number of connections before fx_opt: 1524
Number of connections after fx opt: 1508
                                                     > tgfs_redund -effort 100 -max_iteration 3
> ps Design /HISVHDL/IDCDSUC has:
                                                                      122 IN ports 73 OUT ports
                                               1 instances 0 upcells
745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                                  0 buses
966 nets (0 multiply-driven; 0 undriven)
                                               2547 pins (465 inversions)
                                                                                  2.64 pins per
           1508 literals 21 levels
                                   10 max fanin
                                                           19 max fanout
tafs_redund -effort 100 -max_iteration 3
                                               > echo {Custom Synzilla Report} Custom Synzilla
22 IN ports 73 OUT ports
                                   745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0
UNLINKED; 0 DC)
                       0 buses
                                   966 nets (0 multiply-driven; 0 undriven)
                                                                                  2547 pins
(465 inversions)
                       2.64 pins per net
                                               1508 literals 21 levels
                                                                      10 max fanin
19 max fanout
                       Cell Information
                                                          FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180: area
                     0)
                                                               (ncount 83: area
                                               PSEUDO_REG
cb clk 32 1 (ncount
                      6: area
                                480)
                                                          cb_mode_block (ncount
                                                                                   1: area
                       cs_invvn01c_sl (ncount
                                              10 : area
                                                                                  Total Area =
570 (Comb = 20 : Non-Comb = 550)
                                            > write_end_point_report -points 2
[ET-0018]:>Begin...New EndPoint Report
                                            for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report.
                                           Sun Apr 18 21:52:17 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                           EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                       Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack
                                          Abbreviation Comparison/Description
                          Slack Continuation
                                                  SIkCont
                                                             Slack due to a point downstream on
path Required Arrival Time
                              RAT
                                         ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT
                                ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                              ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                   ClkGSet
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                   ClkGHld
                                                              ( DATA ARRIVAL TIME - CLOCK
```

```
CIKTPW
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                           Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                           Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
        ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
                            ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                    CIkPW
ClockPulseWidth
                                    ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                            ALTest
                                                                       (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
         Slack discontinuity due to failed test
                                       Num/
ATLimit
                                     Delay/ Failed Test/ Test PinName
LimitedAT/
                                            P Func T.Adj NetName
E Phase AT Slack Slew CL FO Cell
------
                                                        F C3+R · 2849 -1528
                 1 drain blk.reg_n.lat_0/BASE_REG/a
                                                                             0
                 05d cl_invvn05d 39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
27 1 cl_invvn
                 60 238 14 cl_invvn
                                  05d
                                                 1200 c1 ---->
F C3- 160
                                         F C3+R 2849 -1528
drain blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                              0 27 1 AND
       0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1
                                                              R C3+R 2897 -1528
                             -48 a ----> drain_blk.reg_n.lat_0/a
                                                                        R C3+R
                       AND
0 21 1 AND
                                        PSEUDO_REG 0 a ---->{a}
             0 21 1 PSEUDO_REG
2897 -1528
M#2.EXPRESSION#104EXPR0/OUT
                                        R C3+R 2897 -1528 0 21 1 AND
                                                           F C3+R 2740 -1528
        0 N687 ---> M#2.EXPRESSION#104EXPR0/IN1
                     AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
 21 1 AND
                     0 21 1 AND
                                            AND
                                                    0 NET667 ---->
F C3+R 2740 -1528
                                  R C3+R 2479 -1528 0 21 1 AND
M#2.OR VECT#3/IN9
                                                              R C3+R 2479 -1528
       261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT
                              0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
                     AND
0 21 1 AND
                                                   104 N1393 ---->{d} C1398/OUT
FC3+R
                     0 37 2 AND
                                            AND
       2374 -1528
                                                    0 N1393 ----> C1398/IN2
                     0 37 2 AND
                                            AND
FC3+R
        2374 -1528
                                                    104 N927 ----> C1297/OUT
        2270 -1528 0 53 3 AND
                                            AND
R C3+R
                   0 53 3 AND
                                            AND
                                                    0 N927 ---> C1297/IN1
RC3+R
        2270 -1528
                                                    52 N1292
                                            AND
FC3+R
        2218 -1528
                     0 21 1 AND
                                    F C3+R 2218 -1528
---->{e} C932/OUT
                                                         0 21 1 AND
                                                 R C3+R 2113 -1528
        0 N1292 ----> C932/IN1
AND
                      104 NET994 ---->{f} M#2.EXPRESSION#92EXPR2/OUT
                                                                               R
               AND
AND
                      21 1 AND
                                           AND
                                                   0 NET994 ---->
      2113 -1528
                    0
C3+R
                                       F C3+R 2009 -1528
                                                            0 1190 5 AND
M#2.EXPRESSION#92EXPR2/IN2
       104 N1098 ---->{g} C1103/OUT
                                                    F C3+R 2009 -1528
                                                                         0 1190
                                                                          1904
                         0 N1098 ---->
                                     C1103/IN1
                                                                   R C3+R
5 AND
                 AND
                                      104 N1097 ---->{h} C1102/OUT
        0 21 1 AND
-1528
                               AND
                                                     0 N1097 ----> C1102/IN14
        1904 -1528
                        21 1 AND
                                             AND
R C3+R
                                                    104 N1480 ---> C1485/OUT
                                             AND
        1800 -1528
                     0
                        21 1 AND
FC3+R
                                             AND
                                                    0 N1480 ----> C1485/IN1
        1800 -1528
                     0 21 1 AND
FC3+R
                                                    52 N1479 ---->{i} C1484/OUT
                                             AND
RC3+R
        1747 -1528
                        37 2 AND
                                                     0 N1479 ---> C1484/IN5
                                             AND
        1747 -1528
                        37 2 AND
RC3+R
                     0
                                                    157 N1498 ----> C1503/OUT
                        37 2 AND
                                             AND
FC3+R
        1591 -1528
                     0
                                                    0 N1498 ----> C1503/IN1
FC3+R
        1591 -1528
                     0
                        37 2 AND
                                            AND
                                                    52 N1497 ---->{j} C1502/OUT
        1539 -1528
                     0 21 1 AND
                                             AND
R C3+R
                                                    0 N1497 ----> C1502/IN10
                                             AND
R C3+R
        1539 -1528
                     0 21 1 AND
        1330 -1528
                                             AND
                                                    209 N1502 ---> C1507/OUT
FC3+R
                     0
                        37 2 AND
                                            AND
                                                     0 N1502 ---> C1507/IN1
        1330 -1528
                     0
                        37 2 AND
FC3+R
                                                    52 N1501 ---->{k} C1506/OUT
        1277 -1528
                        21 1 AND
                                             AND
R C3+R
                                   0 N1501 ---> C1506/IN2
                           AND
   0 21 1 AND
                                                  209 N1002 ---->{I} C1007/OUT
                                           AND
C3+R 1068 -1528
                    0 21 1 AND
                                                     0 N1002 ---> C1007/IN1
                                             AND
       1068 -1528
                    0 21 1 AND
FC3+R
```

```
AND
RC3+R
         912 -1528
                    0 21 1 AND
                                                   157 N1001 ---->{m} C1006/OUT
                                                    0 N1001 ----> C1006/IN1
R C3+R
         912 -1528
                    0 21 1 AND
                                           AND
        807 -1528
                    0 21 1 AND
                                                   104 N1314 ---> C1319/OUT
FC3+R
                                           AND
                    0 21 1 AND
        807 -1528
                                                   0 N1314 ----> C1319/IN1
FC3+R
                                           AND
         755 -1528
                    80 16 1 AND
                                            AND
                                                  52 op dsbl before ---->
R C3+R
                                                                              0
                             R C3+R 755 -1528
                                                  80 16 1 PI
op dsbl before
op dsbl before
                 2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2816 -1444
27 1 cl invvn
                 05d cl_invvn05d -12 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
F C3- 160
                 60 238 14 cl_invvn 05d
                                                1200 c1 ---->
drain blk.reg n.lat 0/DELAY ELEMENT/OUT R C3+R 2816 -1444 0 27 1 AND
AND "0" DEL'AY ----> "drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1
                                                             FC3+R 2870 -1444
                    AND -54 a ----> drain_blk.reg_n.lat_0/a
0 21 1 AND
                                                                       FC3+R
2870 -1444 0 21 1 PSEUDO_REG PSEUDO_REG 0 a ---->{a}
M#2.EXPRESSION#104EXPR0/OUT F C3+R 2870 -1444 0 21 1 AND
        0 N687 ---> M#2.EXPRESSION#104EXPR0/IN1
                                                           R C3+R 2713 -1444
                    AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
0 21 1 AND
R C3+R 2713 -1444
                     0 21 1 AND
                                          AND 0 NET667 ---->
                           F C3+R 2452 -1444 0 21 1 AND
M#2.OR_VECT#3/IN9
      261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT
                                                             FC3+R 2452 -1444
AND
0 21 1 AND
                    AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
       2347 -1444
                    0 37 2 AND
                                            AND
                                                   104 N1393 ---->{d} C1398/OUT
R C3+R
       2347 -1444 0 37 2 AND
                                            AND
                                                    0 N1393 ----> C1398/IN2
R C3+R
                                         AND
AND
AND
                                                   104 N927 ----> C1297/OUT
        2243 -1444 0 53 3 AND
FC3+R
       ·2243 -1444 0 53 3 AND
                                                   0 N927 ----> C1297/IN1
FC3+R
                    0 21 1 AND
                                                    52 N1292 ---->{e} C932/OUT
       2191 -1444
R C3+R
                                          AND
RC3+R
       2191 -1444
                     0 21 1 AND
                                                    0 N1292 ----> C932/IN1
FC3+R
       2086 -1444
                     0 21 1 AND
                                           AND
                                                   104 NET994 ---->{f}
       F C3+R 2086 -1444
                            0 21 1 AND
                                                   AND
                                                           0 NET994 --->
M#2.EXPRESSION#92EXPR2/IN2
                                      R C3+R 1982 -1444
                                                            0 1190 5 AND
      104 N1098 ---->{g} C1103/OUT
                                                    R C3+R 1982 -1444 0 1190
AND
                        0 N1098 ----> C1103/IN1
5 AND
                AND
                                                                  F C3+R 1877
                                      104 N1097 ---->{h} C1102/OUT
-1444
        0 21 1 AND
                              AND
FC3+R
        1877 -1444
                        21 1 AND
                                            AND
                                                    0 N1097 ----> C1102/IN14
RC3+R
        1773 -1444
                     0 21 1 AND
                                            AND
                                                   104 N1480 ---> C1485/OUT
RC3+R
        1773 -1444
                     0 21 1 AND
                                            AND
                                                    0 N1480 ---> C1485/IN1
        1720 -1444
                                                    52 N1479 ---->{i} C1484/OUT
                        37 2 AND
FC3+R
                     0
                                            AND
                                                    0 N1479 ---> C1484/IN5
FC3+R
        1720 -1444
                     0
                        37 2 AND
                                            AND
                                                   157 N1498 ----> C1503/OUT
RC3+R
        1564 -1444
                     0
                        37 2 AND
                                            AND
        1564 -1444
                                                    0 N1498 ----> C1503/IN1
                                            AND
RC3+R
                     0
                        37 2 AND
                                                    52 N1497 ---->{i} C1502/OUT
FC3+R
        1512 -1444
                     0 21 1 AND
                                            AND
FC3+R
        1512 -1444
                     0 21 1 AND
                                            AND
                                                    0 N1497 ----> C1502/IN10
                                                   209 N1502 ----> C1507/OUT
        1303 -1444
                     0 37 2 AND
R C3+R
                                            AND
                                                    0 N1502 ----> C1507/IN1
RC3+R
        1303 -1444
                     0 37 2 AND
                                            AND
                                                    52 N1501 ---->{k} C1506/OUT
FC3+R
        1250 -1444
                     0 21 1 AND
                                            AND
        1250 -1444
FC3+R
                     0 21 1 AND
                                            AND
                                                    0 N1501 ----> C1506/IN2
RC3+R
        1041 -1444
                     0 21 1 AND
                                            AND
                                                   209 N1002 ---->{I} C1007/OUT
RC3+R
        1041 -1444
                     0 21 1 AND
                                            AND
                                                    0 N1002 ----> C1007/IN1
         885 -1444
FC3+R
                     0 21 1 AND
                                            AND
                                                   157 N1001 ---->{m} C1006/OUT
         885 -1444
                                         - AND
                                                   0 N1001 ---> C1006/IN1
FC3+R
                     0 21 1 AND
         780 -1444
                                                   104 N1314 ---> C1319/OUT
                     0 21 1 AND
                                            AND
RC3+R
                                                    0 N1314 ---> C1319/IN1
         780 -1444 0 21 1 AND
RC3+R
                                            AND
                                                    52 op_dsbl_before ---->
         728 -1444
                    80 16 1 AND
                                            AND
FC3+R
                                                  80 16 1 PI
                              F C3+R 728 -1444
                                                                              0
op dsbl_before
```

```
______
                        0:15 wall time, used 1376256 bytes or 1 meg. > ps Design /HISVHDL/IDCDSUC has:
                                                   745 cells (465 AND; 0 XOR; 0 SEQ; 0
                   122 IN ports 73 OUT ports
instances 0 upcells
                                                   966 nets (0 multiply-driven; 0 undriven)
                                         0 buses
TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                   1508 literals 21 levels
                                                                       10 max fanin
                               2.64 pins per net
2547 pins (465 inversions)
                     > echo {Custom Synzilla Report} Custom Synzilla Report
19 max fanout
                                                              122 IN ports 73 OUT ports
                                         1 instances 0 upcells
-cell Design /HISVHDL/IDCDSUC has:
745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                        0 buses
966 nets (0 multiply-driven; 0 undriven)
                                         2547 pins (465 inversions)
                                                                        2.64 pins per
         1508 literals 21 levels
                                                                        Cell
                                                    19 max fanout
                              10 max fanin
                    FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                                     0)
                                                    cb_clk_32_1 (ncount
PSEUDO_REG (ncount 83: area 0)
                                                                        6: area
                    cb_mode_block (ncount 1: area
                                                    70)
                                                    Total Area = 570 (Comb = 20:
cs_invvn01c_sl (ncount 10 : area
                              20)
                         > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550
            for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Report
Sun Apr 18 21:52:18 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                     EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
                     Max. Slack: 1.13427E+38 Sort Field: Slack
                                                                       Max.
-1.13427E+38
                                 Abbreviation Comparison/Description ------
Endpoints: 2 Cause of Slack
                                                       Slack due to a point downstream on
                                             SIkCont
----- Slack Continuation
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
                           RAT
path Required Arrival Time
                           ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                 CIKGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
Gating Setup
                                                       ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                          ClkGHld
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                     CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                              Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                              Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
          ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                      ClkPW
ClockPulseWidth
                                                ( CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
                                      ClkSep
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
          Slack discontinuity due to failed test
                                         Num/
ATLimit
                                       Delay/ Failed Test/ Test PinName
LimitedAT/
                                              P Func T.Adj NetName
E Phase AT Slack Slew CL FO Cell
                                           -----
                                                          FC3+R 2849 -1528
                  1 drain_blk.reg_n.lat_0/BASE_REG/a
                    05d cl_invvn05d 39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
27 1 cl_invvn
                                           05d
                                                   1200 c1 ---->
                  60 238 14 cl_invvn
F C3-
        160
                                           FC3+R
                                                   2849 -1528
                                                                 0
                                                                    27 1 AND
drain blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                                 0 21 1 AND
                                                    2897 -1528
 drain blk.reg n.lat 0/DELAY_ELEMENT/IN1
                                           R C3+R
                                                           2897 -1528
                                                   R C3+R
       -48 a ---> drain blk.reg_n.lat_0/a
AND
                                     0 a ---->{a} M#2.EXPRESSION#104EXPR0/OUT
PSEUDO_REG
                      PSEUDO REG
                                                       0 N687 ---->
                                               AND
R C3+R 2897 -1528
                      0 21 1 AND
                                         F C3+R 2740 -1528
                                                               0 21 1 AND
M#2.EXPRESSION#104EXPR0/IN1
                                                             FC3+R 2740 -1528
       157 NET667 ---->{b} M#2.OR_VECT#3/OUT
AND
                                                                                  R
                              0 NET667 ----> M#2.OR_VECT#3/IN9
0 21 1 AND
                        AND
                                             AND
                                                    261 N685 ---->{c}
C3+R 2479 -1528
                     0
                       21 1 AND
                                                   2479 -1528 0 21 1 AND
                                          R C3+R
M#2.EXPRESSION#103EXPR0/OUT
         0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
                                                              F C3+R 2374 -1528
                                104 N1393 ---->{d} C1398/OUT
                         AND
0 37 2 AND
```

```
C3+R 2374 -1528
                  0 37 2 AND
                                       AND
                                                0 N1393 ---> C1398/IN2
R C3+R 2270 -1528
                   0 53 3 AND
                                          AND
                                                 104 N927 ----> C1297/OUT
        2270 -1528 0 53 3 AND
R C3+R
                                                  0 N927 ----> C1297/IN1
                                          AND
F C3+R 2218 -1528
                    0 21 1 AND
                                          AND
                                                 52 N1292
---->{e} C932/OUT
                                  F C3+R 2218 -1528 0 21 1 AND
AND
       0 N1292 ----> C932/IN1
                                              R C3+R 2113 -1528
AND
             AND
                    104 NET994 ---->{f} M#2.EXPRESSION#92EXPR2/OUT
                                                                           R
      2113 -1528 0 21 1 AND AND 0 NET994 ---->
C3+R
M#2.EXPRESSION#92EXPR2/IN2
                                     FC3+R 2009 -1528 0 1190 5 AND
AND
      104 N1098 ---->{g} C1103/OUT
                                                 F C3+R 2009 -1528
                                                                      0 1190
5 AND
               AND
                       0 N1098 ----> C1103/IN1
                                                               R C3+R 1904
-1528
       0 21 1 AND
                             AND
                                    104 N1097 ---->{h} C1102/OUT
      1904 -1528
R°C3+R
                       21 1 AND
                                          AND
                                                 0 N1097 ----> C1102/IN14
       1800 -1528
                    0 21 1 AND
                                                 104 N1480 ---> C1485/OUT
FC3+R
                                          AND
                                        AND
AND
AND
FC3+R
       1800 -1528
                    0 21 1 AND
                                                 0 N1480 ----> C1485/IN1
R C3+R
       1747 -1528
                    0 37 2 AND
                                                 52 N1479 ---->{i} C1484/OUT
R C3+R
       1747 -1528
                    0 37 2 AND
                                                 0 N1479 ----> C1484/IN5
FC3+R
       1591 -1528
                    0 37 2 AND
                                       AND 157 N1498 ----> C1503/OUT
FC3+R
                                                 0 N1498 ----> C1503/IN1
       1591 -1528
                    0 37 2 AND
                                       AND
       1539 -1528
R C3+R
                    0 21 1 AND
                                                 52 N1497 ---->{j} C1502/OUT
                                          AND
-> C1502/IN10
                               F C3+R 1330 -1528 0 37 2 AND
AND
      209 N1502 ---->
                    C1507/OUT
                                                F C3+R 1330 -1528
                                                                     0 37 2
AND
              AND
                      0 N1502 ---> C1507/IN1
                                                              R C3+R 1277
-1528
       0 21 1 AND
                             AND
                                    52 N1501 ---->{k} C1506/OUT
R C3+R
       1277 -1528
                       21 1 AND
                                          AND
                                                  0 N1501 ---> C1506/IN2
                                                 209 N1002 ---->{I} C1007/OUT
FC3+R
       1068 -1528
                    0 21 1 AND
                                          AND
                    0 21 1 AND
       1068 -1528
FC3+R
                                         AND
                                                 0 N1002 ----> C1007/IN1
        912 -1528
                    0 21 1 AND
                                        AND
R C3+R
                                                 157 N1001 ---->{m} C1006/OUT
                                     AND
        912 -1528
R C3+R
                    0 21 1 AND
                                                0 N1001 ----> C1006/IN1
                                     AND
F C3+R
        807 -1528
                   0 21 1 AND
                                                104 N1314 ---> C1319/OUT
F C3+R
        807 -1528
                   0 21 1 AND
                                         AND
                                                 0 N1314 ----> C1319/IN1
R C3+R
        755 -1528
                   80 16 1 AND
                                          AND
                                                52 op_dsbl_before ---->
op dsbl before
                            R C3+R 755 -1528
                                                80 16 1 PI
                                                                           0
op_dsbl_before
_____
                2 drain blk.reg n.lat 0/BASE REG/a R C3+R 2816 -1444
27 1 cl_invvn
                05d cl_invvn05d -12 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
            60 238 14 cl_invvn 05d 1200 c1 ----> at 0/DELAY ELEMENT/OUT R C3+R 2816 -1444
F C3- 160
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                          0 27 1 AND
AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 F C3+R 2870 -1444
                           -54 a ----> drain_blk.reg_n.lat_0/a
0 21 1 AND
                      AND
                                                                    FC3+R
2870 -1444 0 21 1 PSEUDO_REG
                                      PSEUDO_REG 0 a ---->{a}
M#2.EXPRESSION#104EXPR0/OUT
                                      F C3+R 2870 -1444 0 21 1 AND
AND 0 N687 ----> M#2.EXPRESSION#104EXPR0/IN1
                                                   R C3+R 2713 -1444
0 21 1 AND
                  AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
R C3+R 2713 -1444
                    0 21 1 AND
                                          AND 0 NET667 ---->
M#2.OR_VECT#3/IN9
                                F C3+R 2452 -1444 0 21 1 AND
      261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT
                                                          FC3+R 2452 -1444
0 21 1 AND
             AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
                    0 37 2 AND
R C3+R 2347 -1444
                                          AND
                                                 104 N1393 ---->{d} C1398/OUT
                                    AND
AND
                  0 37 2 AND
                                                 0 N1393 ----> C1398/IN2
104 N927 ----> C1297/OUT
       2347 -1444
R C3+R
                                      AND
FC3+R 2243 -1444
                    0 53 3 AND
      AND 0 N927 ----> C1297/IN1
                                                    R C3+R 2191 -1444
21 1 AND
                   AND
                          52 N1292 ---->{e} C932/OUT
                                                                   R C3+R
2191 -1444
            0 21 1 AND
                                 AND 0 N1292 ----> C932/IN1
```

```
AND
                                                           104 NET994 ---->{f}
         2086 -1444
                            21 1 AND
FC3+R
M#2.EXPRESSION#92EXPR2/OUT
                                              FC3+R
                                                       2086 -1444
                                                                      0 21 1 AND
         0 NET994 ---> M#2.EXPRESSION#92EXPR2/IN2
                                                                      RC3+R
                                                                                1982 -1444
AND
                                   104 N1098 ---->{g} C1103/OUT
                                                                                        R
0 1190 5 AND
                            AND
                                                           0 N1098 ----> C1103/IN1
                      0 1190 5 AND
                                                   AND
C3+R
       1982 -1444
                                                           104 N1097 ---->{h} C1102/OUT
                                                   AND
                            21 1 AND
FC3+R
         1877 -1444
                                                            0 N1097 ---> C1102/IN14
                            21 1 AND
                                                   AND
         1877 -1444
FC3+R
                                                           104 N1480 ----> C1485/OUT
                                                   AND
         1773 -1444
                            21 1 AND
R C3+R
                        0
                                                            0 N1480 ---> C1485/IN1
RC3+R
         1773 -1444
                            21 1 AND
                                                   AND
                                                            52 N1479 ---->{i} C1484/OUT
         1720 -1444
                        0
                            37 2 AND
                                                   AND
FC3+R
                                                            0 N1479 ---> C1484/IN5
         1720 -1444
                            37 2 AND
                                                   AND
FC3+R
                        0
                                                           157 N1498 ----> C1503/OUT
         1564 -1444
                            37 2 AND
                                                   AND
RC3+R
                        0
         1564 -1444
                            37 2 AND
                                                   AND
                                                            0 N1498 ----> C1503/IN1
                        0
R'C3+R
                            21 1 AND
                                                   AND
                                                            52 N1497 ---->{j} C1502/OUT
FC3+R
         1512 -1444
                        0
                                                            0 N1497 ---> C1502/IN10
                                                   AND
         1512 -1444
                            21 1 AND
                        0
FC3+R
                                                   AND
                                                           209 N1502 ---> C1507/OUT
                            37 2 AND
         1303 -1444
                         0
R C3+R
                                                            0 N1502 ----> C1507/IN1
                                                   AND
                            37 2 AND
RC3+R
         1303 -1444
                         0
                                                           52 N1501 ---->{k} C1506/OUT
                            21 1 AND
                                                   AND
FC3+R
         1250 -1444
                        0
                                                            0 N1501 ---> C1506/IN2
                            21 1 AND
                                                   AND
         1250 -1444
FC3+R
                        0
                                                           209 N1002 ---->{I} C1007/OUT
                                                   AND
                            21 1 AND
RC3+R
         1041
               -1444
                         0
                                                            0 N1002 ----> C1007/IN1
         1041 -1444
                                                   AND
                            21 1 AND
RC3+R
                        0
                                                           157 N1001 ---->{m} C1006/OUT
                                                   AND
          885 -1444
                        0
                            21 1 AND
FC3+R
                                                            0 N1001 ---> C1006/IN1
                                                   AND
          885 -1444
                            21 1 AND
FC3+R
                        0
                                                           104 N1314 ----> C1319/OUT
          780 -1444
                        0
                            21 1 AND
                                                   AND
RC3+R
                                                   AND
                                                            0 N1314 ----> C1319/IN1
          780 -1444
                        0
                            21 1 AND
RC3+R
                                            op_dsbl_before
                                                                               FC3+R
                     52 op_dsbl_before ---->
            AND
                                              0 op_dsbl_before
728 -1444
             80
                  16 1 PI
                            > cputime Used 1.04 cpu seconds or 00:00:01 wall time, used 0 bytes or 0 byte.
561.845093
                                                                     122 IN ports 73 OUT ports
> ps Design /HISVHDL/IDCDSUC has:
                                              1 instances 0 upcells
745 cells (465 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                                0 buses
                                              2547 pins (465 inversions)
                                                                                2.64 pins per
966 nets (0 multiply-driven; 0 undriven)
                                                                                  > ps Design
                                                         19 max fanout
           1508 literals 21 levels
                                  10 max fanin
net
                                   1 instances 0 upcells
                                                         122 IN ports 73 OUT ports
/HISVHDL/IDCDSUC has:
648 cells (368 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                                 0 buses
                                              2353 pins (553 inversions)
869 nets (0 multiply-driven; 0 undriven)
                                                                                2.71 pins per
                                   10 max fanin
                                                         20 max fanout
                                                                                 > decomp
            1411 literals 14 levels
net
-nand -ddi -dfi -no_xor Performing Circuit Decomposition for design IDCDSUC ... Performing NAND
decomposition ... ... Finished performing NAND decomposition NAND CPU time: 0.08 secs. NAND
memory usage: 0 bytes Performing DDI decomposition ... ... Finished performing DDI decomposition DDI
CPU time: 0.01 secs. DDI memory usage: 0 bytes Performing DFI decomposition ... ... Finished
performing DFI decomposition DFI CPU time: 0.06 secs. DFI memory usage: 0 bytes ....Finished
Performing Circuit Decomposition for design IDCDSUC Decomposition CPU time: 0.15 secs.
                                             > gf -area -t 10 Number of connections before gf:
Decomposition memory usage: 0 bytes
1508 Number of connections after gf: 1505 gf CPU time: 0.63 secs. gf memory usage: 0 bytes
> decomp -nand -ddi -dfi -no_xor Performing Circuit Decomposition for design IDCDSUC ... Performing
NAND decomposition ... ... Finished performing NAND decomposition NAND CPU time: 0.01 secs. NAND
memory usage: 0 bytes Performing DDI decomposition ... ... Finished performing DDI decomposition DDI
CPU time: 0.00 secs. DDI memory usage: 0 bytes Performing DFI decomposition ... ... Finished
performing DFI decomposition DFI CPU time: 0.00 secs. DFI memory usage: 0 bytes ....Finished
Performing Circuit Decomposition for design IDCDSUC Decomposition CPU time: 0.01 secs.
                                              > tqfs redund -effort 100 -max_iteration 3
 Decomposition memory usage: 0 bytes
 > equiv -time -trace 10 Processing on 0:20 levels Bdd Equivalence routine found 0 redundancies and 24
                                                > tqfs redund -effort 100 -max_iteration 3
 equivalences Processing on 21:20 levels
```

```
> ps Design /HISVHDL/IDCDSUC has:
                                             1 instances 0 upcells
                                                                    122 IN ports 73 OUT ports
722 cells (442 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                               0 buses
943 nets (0 multiply-driven; 0 undriven)
                                             2498 pins (486 inversions)
                                                                               2.65 pins per
           1482 literals 19 levels
                                  10 max fanin
                                                         20 max fanout
                                                                                 > ps Design
/HISVHDL/IDCDSUC has:
                                  1 instances 0 upcells
                                                         122 IN ports 73 OUT ports
722 cells (442 AND; 0 XOR; 0 SEQ; 0 TRI; 280 LINKED; 0 UNLINKED; 0 DC)
                                                                               0 buses
                                             2498 pins (486 inversions)
943 nets (0 multiply-driven; 0 undriven)
                                                                               2.65 pins per
           1482 literals 19 levels
                                  10 max fanin
                                                         20 max fanout
                                                                               > tgfs_redund
-effort 100 -report_only [TGFS-800]: Out of a total of 2822 faults identified 0 redundancies: could not
decide on: 0.
                   > echo {=== Optimization process finished ===} === Optimization process finished
             > echo {Custom Synzilla Report} Custom Synzilla Report
                                                                       > ps -cell Design
/HISVHDL/IDCDSUC has:
                                  1 instances 0 upcells
                                                         122 IN ports 73 OUT ports
KED; 0 DC) 0 buses 943 nets (0 multiply-driven; 0 undriven)
                                                                    2498 pins (486 inversions)
2.65 pins per net
                       1482 literals 19 levels
                                             10 max fanin
                                                                    20 max fanout
Cell Information
                                  FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                                                       0)
PSEUDO_REG
                (ncount 83 : area
                                                         cb_clk_32_1 (ncount 6: area
480)
                      cb_mode block (ncount 1: area
                                                         70)
cs invvn01c sl (ncount 10 : area
                                 20)
                                                         Total Area = 570 (Comb = 20:
Non-Comb = 550
                         > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
21:52:29 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                 EDA EinsTimer EndPoint
Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack
                                                     Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description
                                   -----
Continuation
                  SIkCont
                             Slack due to a point downstream on path Required Arrival Time
RAT
          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
                                                                               ClkGSet
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating
                      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
           ClkGHld
+ ADJUST ) Clock Tree Pulse Width
                                     CIKTPW
                                                 ( CLOCK LEADING EDGE + PULSE WIDTH <
CLOCK TRAILING EDGE ) Setup
                                                       ( DATA ARRIVAL TIME + SETUP <
                                             Setup
CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                              ( DATA ARRIVAL TIME - HOLD
                                                     Hold
> CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                          EndOfC
                                                                     ( DATA ARRIVAL TIME
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
                                                                     CIkPW
                                                                                (CLOCK
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation
                                                                                 ClkSep
(CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST) Loop
          ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
Arrival Time Limiting
                       ATLimit
                                 Slack discontinuity due to failed test
LimitedAT/
                                          Delay/ Failed Test/ Test PinName
E Phase
          AT Slack Slew CL FO Cell
                                                  P Func T.Adj NetName
                    1 drain_blk.reg_n.lat_0/BASE_REG/a
                                                               F C3+R
                                                                         2796 -1476
                     05d cl_invvn05d 39 DELAY Setup drain_blk.reg_n.lat_0/BASE_REG/c1
27 1 cl invvn
FC3-
        160
                   60 238 14 cl_invvn
                                               05d
                                                        1200 c1 ---->
drain_blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                               FC3+R
                                                        2796 -1476
                                                                       0 27 1 AND
         0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1.
                                                                      R C3+R
                                                                               2844 -1476
   21 1 AND
                                  -48 a ----> drain_blk.reg_n.lat_0/a
                          AND
                                                                                 R C3+R
2844 -1476
              0 21 1 PSEUDO REG
                                               PSEUDO_REG
                                                               0 a ---->\{a\}
M#2.EXPRESSION#104EXPR0/OUT
                                              RC3+R
                                                       2844 -1476
                                                                      0
                                                                          21 1 AND
AND
         0 N687 ---> M#2.EXPRESSION#104EXPR0/IN1
                                                                   FC3+R
                                                                            2688 -1476
                FC3+R
                        2688 -1476
                                        0 21 1 AND
                                                                  AND
                                                                           0 NET667 ---->
M#2.OR_VECT#3/IN9
                                      R C3+R
                                                2427 -1476
                                                               0 21 1 AND
        261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT
                                                                      R C3+R
                                                                               2427 -1476
   21 1 AND
                          AND
                                   0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
FC3+R
         2322 -1476
                        0 37 2 AND
                                                   AND
                                                          104 N1393 ---->{d} C1398/OUT
```

```
F C3+R 2322 -1476 0 37 2 AND AND 0 N1393 ----> C1398/IN2
R C3+R 2218 -1476 0 53 3 AND AND 104 N1292 ----> C1655/OR
R C3+R 2218 -1476 0 53 3 AND AND 0 N1292 ----> C1655/IN1
F C3+R 2165 -1476 0 21 1 AND AND 52 N1650 ----> {e} C932/OU
F C3+R 2165 -1476 0 21 1 AND AND 0 N1650 ----> C932/IN1
R C3+R 2061 -1476 0 21 1 AND AND 104 NET994 ----> {f}
M#2.EXPRESSION#92EXPR2/OUT R C3+R 2061 -1476 0 21 1 AND
                                                                                                                                             0 N1393 ----> C1398/IN2
                                                                                                                                              104 N1292 ----> C1655/OUT
                                                                                                                                             0 N1292 ----> C1655/IN1
                                                                                                                                               52 N1650 ---->{e} C932/OUT
                                                                                                                                              F C3+R 1956 -1476
AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2 F C3+R 1956 -1476 0 1190 5 AND AND 104 N1098 ----> {g} C1103/OUT F C3+R 1956 -1476 0 1190 5 AND AND 0 N1098 ----> C1103/IN1 R C3+R 1852 -1476 0 21 1 AND AND 104 N1097 ----> {h} C1102/OUT R C3+R 1852 -1476 0 21 1 AND AND 0 N1097 ----> C1102/IN14 F C3+R 1747 -1476 0 21 1 AND AND 104 N1692 ----> C1697/OUT F C3+R 1747 -1476 0 21 1 AND AND 0 N1692 ----> C1697/OUT R C3+R 1695 -1476 0 37 2 AND AND 52 N1479 ----> {i} C1484/OUT R C3+R 1539 -1476 0 37 2 AND AND 0 N1479 ----> C1726/OUT F C3+R 1539 -1476 0 37 2 AND AND 157 N1497 ----> C1726/OUT F C3+R 1539 -1476 0 37 2 AND AND 0 N1497 ----> C1726/OUT R C3+R 1486 -1476 0 21 1 AND AND 52 N1721 ----> {ij C1502/OUT R C3+R 1486 -1476 0 21 1 AND AND 0 N1721 ----> C1502/IN10 F C3+R 1277 -1476 0 37 2 AND AND 0 N1721 ----> C1502/IN10 F C3+R 1277 -1476 0 37 2 AND AND 0 N1723 ----> {k} C1506/OUT F C3+R 1277 -1476 0 37 2 AND AND 0 N1723 ----> {k} C1506/IN2 F C3+R 1277 -1476 0 37 2 AND AND 0 N1723 ----> {k} C1506/IN2 F C3+R 1277 -1476 0 37 2 AND AND 0 N1723 ----> {k} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} C1506/IN2 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} AND 157 N106 F C3+R 1068 -1476 0 21 1 AND AND 209 N1002 ----> {l} AND AND 209 N1002 ----> {l} AND AND 209 N100
                      0 NET994 ---> M#2.EXPRESSION#92EXPR2/IN2
                                                                                                                                                                       AND 157 N1001
                                                                              R C3+R 912 -1476 0 21 1 AND
 ---->{m} C1006/OUT
                                                                                                                                       FC3+R 807 -1476 0 21 1
 AND 0 N1001 ----> C1006/IN1
                                      AND 104 N1673 ----> C1678/OUT
                                                                                                                                                                                      F C3+R : 807
 AND
 -1476 0 21 1 AND AND 0 N1673 ----> C1678/IN1
R C3+R 755 -1476 80 16 1 AND AND 52 op_dsbl_before ----> op_dsbl_before R C3+R 755 -1476 80 16 1 PI
                                                                                                                                                                                                                         0
  op_dsbl_before
  ----- 2 drain_blk.reg_n.lat_0/BASE_REG/a R C3+R 2764 -1392
 AND 0 DELAY ----> drain_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 F C3+R 2817 -1392
  0 21 1 AND AND -54 a ----> drain_blk.reg_n.lat_0/a
                                                                                                                                                                                                FC3+R
  0 N687 ----> M#2.EXPRESSION#104EXPR0/IN1 R C3+R 2661 -1392
  AND
                                             AND 157 NET667 ---->{b} M#2.OR_VECT#3/OUT
  0 21 1 AND
  R C3+R 2661 -1392 0 21 1 AND AND 0 NET667 ---->
M#2.OR_VECT#3/IN9 F C3+R 2400 -1392 0 21 1 AND
                261 N685 ---->{c} M#2.EXPRESSION#103EXPR0/OUT F C3+R 2400 -1392
                                          AND 0 N685 ----> M#2.EXPRESSION#103EXPR0/IN2
  0 21 1 AND
 R C3+R 2295 -1392 0 37 2 AND AND 104 N1393 ----> (d) C1398/OUT R C3+R 2295 -1392 0 37 2 AND AND 0 N1393 ----> (d) C1398/OUT F C3+R 2191 -1392 0 53 3 AND AND 104 N1292 ----> C1655/OUT F C3+R 2191 -1392 0 53 3 AND AND 0 N1292 ----> C1655/IN1 R C3+R 2138 -1392 0 21 1 AND AND 52 N1650 ----> (e) C932/OUT R C3+R 2138 -1392 0 21 1 AND AND 0 N1650 ----> C932/IN1 F C3+R 2034 -1392 0 21 1 AND AND 104 NET994 ----> (f) M#2.EXPRESSION#92EXPR2/OUT F C3+R 2034 -1392 0 21 1 AND AND 0 NIET994 ----> (f) M#2.EXPRESSION#92EXPR2/IN12
   AND 0 NET994 ----> M#2.EXPRESSION#92EXPR2/IN2 R C3+R 1929 -1392
```

```
-1392
         0
             21 1 AND
                                              104 N1692 ---->
                                                               C1697/OUT
                                     AND
RC3+R
          1720 -1392
                          0
                              21 1 AND
                                                      AND
                                                               0 N1692 ---> C1697/IN1
FC3+R
          1668 -1392
                              37 2 AND
                          0
                                                      AND
                                                               52 N1479 ---->{i} C1484/OUT
FC3+R
          1668 -1392
                              37 2 AND
                                                      AND
                                                               0 N1479 ---> C1484/IN5
RC3+R
          1512 -1392
                          0
                              37 2 AND
                                                              157 N1497 ----> C1726/OUT
                                                      AND
RC3+R
          1512 -1392
                          0
                              37 2 AND
                                                      AND
                                                               0 N1497 ---> C1726/IN1
FC3+R
          1459 -1392
                          0
                              21 1 AND
                                                      AND
                                                               52 N1721 ---->{i} C1502/OUT
FC3+R
          1459 -1392
                              21 1 AND
                          0
                                                      AND
                                                               0 N1721 ---> C1502/IN10
          1250 -1392
R C3+R
                          0
                              37-2 AND
                                                              209 N1723 ---->{k} C1506/OUT
                                                      AND
RC3+R
          1250 -1392
                              37 2 AND
                                                               0 N1723 ----> C1506/IN2
                          0
                                                      AND
RC3+R
          1041 -1392
                          0
                              21 1 AND
                                                      AND
                                                              209 N1002 ---->{I} C1007/OUT
RC3+R
          1041 -1392
                          0
                              21 1 AND
                                                      AND
                                                               0 N1002 ---> C1007/IN1
                                                             157 N1001 ---->{m} C1006/OUT
FC3+R
          885 -1392
                         0
                             21 1 AND
                                                     AND
FC3+R
          885 -1392
                         0
                             21 1 AND
                                                     AND
                                                              0 N1001 ---> C1006/IN1
           780 -1392
RC3+R
                         0
                             21 1 AND
                                                     AND
                                                              104 N1673 ----> C1678/OUT
RC3+R
           780 -1392
                         0
                             21 1 AND
                                                     AND
                                                               0 N1673 ----> C1678/IN1
FC3+R
          728 -1392
                        80
                             16 1 AND
                                                      AND
                                                               52 op_dsbl_before ---->
op_dsbl_before
                                    FC3+R
                                               728 -1392
                                                                 16 1 PI
                                                            80
                                                                                              0
op_dsbl_before
                          > report_area Design: /IDCDSUC - Area: 2731.154785, Area(Weight):
                    > cputime Used 11.00 cpu seconds or 00:00:11 wall time, used 0 bytes or 0 byte.
> echo {=== Techmap process === Loading:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/tmap.tcl
                                                                       > echo {=== Technology .
mapping using wave 5 patterns 400 ===} === Technology mapping using wave 5 patterns 400 ===
> freeze_net_loads -set -limit [TIMER-6411]: Unasserted load on 369 inet(s). [TIMER-6412]: Asserted
                             > resize -trace 0 -local -mincut -inc -sequential -ana 100... Average
load on 369 inet(s).
Inverter area (used for gain scaling) = 7.5875 resize
                                                            Area: before 2731.15 after 2731.15
            Cell: before 722 after 722 (0.00 %)
                                                Time: 0.750000
                                                                          > decomp -ddi -dfi
-step2 -xor Performing Circuit Decomposition for design IDCDSUC ... Performing DDI decomposition ...
... Finished performing DDI decomposition DDI CPU time: 0.01 secs. DDI memory usage: 0 bytes
Performing DFI decomposition ... ... Finished performing DFI decomposition DFI CPU time: 0.00 secs.
DFI memory usage: 0 bytes Levelizing design ... ... Finished levelizing design Levelization CPU time:
0.03 secs. Levelization memory usage: 0 bytes Performing STEP 2 composition ... ... Finished
performing STEP 2 composition STEP 2 CPU time: 0.01 secs. STEP 2 memory usage: 0 bytes
...Finished Performing Circuit Decomposition for design IDCDSUC Decomposition CPU time: 0.05 secs.
Decomposition memory usage: 0 bytes
                                               > freeze_net_loads -reset [TIMER-6411]: Unasserted
load on 369 inet(s).
                             > resize -trace 0 -local -mincut -inc -sequential -ana 100... resize
Area: before 2731.15 after 2731.15 (0.00 %)
                                                Slack: before -1475.6755 after -1475.6755 (0.00 %)
Cell: before 722 after 722 (0.00 %)
                                    Time: 1.520000
                                                               > freeze_net_loads -set -limit
[TIMER-6412]: Asserted load on 369 inet(s).
                                                    > decomp -nand -ddi -dfi -step2 -step3 -no xor
-timer Performing Circuit Decomposition for design IDCDSUC ... Performing NAND decomposition ... ...
Finished performing NAND decomposition NAND CPU time: 0.03 secs. NAND memory usage: 0 bytes
Performing DDI decomposition ... ... Finished performing DDI decomposition DDI CPU time: 0.00 secs.
DDI memory usage: 0 bytes Performing DFI decomposition ... ... Finished performing DFI decomposition
DFI CPU time: 0.02 secs. DFI memory usage: 0 bytes Levelizing design ... ... Finished levelizing design
Levelization CPU time: 0.03 secs. Levelization memory usage: 0 bytes Performing STEP 2 composition
... ... Finished performing STEP 2 composition STEP 2 CPU time: 0.01 secs. STEP 2 memory usage: 0
bytes Performing STEP 3 decomposition ... ... Finished performing STEP 3 decomposition STEP 3 CPU
time: 0.82 secs. STEP 3 memory usage: 0 bytes ...Finished Performing Circuit Decomposition for design
IDCDSUC Decomposition CPU time: 0.91 secs. Decomposition memory usage: 0 bytes
```

104 N1098 ---->{g} C1103/OUT

C1102/IN14

FC3+R

1825 -1392

F C3+R 1825 -1392

0 21 1 AND

R C3+R

0 21

1720

0 1190 5 AND

AND

1 AND

0 N1098 ----> C1103/IN1

104 N1097 ---->{h} C1102/OUT

**AND** 

**AND** 

0 N1097 ---->

```
> techmap -tlibrary SIZELESS -wave 5 -max_net_patterns 400...
load_update -suspend
Performing Technology Mapping for design IDCDSUC ... Levelizing design ... ... Finished levelizing
design Levelization CPU time: 0.03 secs. Levelization memory usage: 0 bytes
<+<+<+<+<+-<+-<+--->-->-->-->---
  ----- Global Pattern Stats ------ Minimum:
                                                                        Inputs: 1. Outputs:
                     Inputs; 4, Outputs: 1, Bidis: 0 Average: Inputs: 1.947787, Outputs:
1. Bidis: 0 Maximum:
1.000000, Bidis: 0.000000 Total Patterns: 881 Minimum Patterns/Net: 1 Maximum Patterns/Net: 6
                  Design Utilization:
                                       cs_nor2n02c_sl - 21
cs oa21n03c_sl - 7
                                       cs_nnd4n03c_sl - 44
                                                            cs ao12n03c sl - 12
                   cs ao22n03c sl - 25
cs xbo2n01b si - 1
cs_oa22n03c_sl - 1 Combinational area: 1393.00 Sequential area: 550.00 Matchless area: 0.00 Total
area: 1943.00 ...Finished Technology Mapping for design IDCDSUC Technology Mapping CPU time:
                                                           > load_update -resume
9.23 secs. Technology Mapping memory usage: 0 bytes.
                                 > echo {Custom Synzilla Report} Custom Synzilla Report
> load_update -invalidate
                                                                   122 IN ports 73 OUT ports
> ps -cell Design /HISVHDL/IDCDSUC has:
                                            1 instances 0 upcells
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC)
                                                                   0 buses
                                                                              984 nets (0
                                 2585 pins (0 inversions) 2.63 pins per net
                                                                              1528 literals
multiply-driven; 0 undriven)
                                 19 max fanout
                                                        Cell Information
           10 max fanin
22 levels
                                                        cb_clk_32_1 (ncount
                                                                              6: area
UDO REG (ncount 83 : area
                                0)
                      cb_mode_block (ncount
                                             1 : area
480)
                                                        cs_ao22n03c_sl (ncount 17 : area
                                 20)
cs_ao12n03c_sl (ncount
                       5: area
                                                       404)
                      cs invvn01c sl (ncount 202 : area
102)
                                                        cs_nnd3n02c_sl (ncount 26 : area
cs_nnd2n02c_sl (ncount 217 : area
                                  651)
                      cs_nnd4n03c_sl (ncount
                                             8: area
104)
                                                        cs nor3n03c sl (ncount
                                                                               1: area
cs_nor2n02c_sl (ncount 12: area
                                 36)
                      cs_oa21n03c_sl (ncount
                                              2 : area
                                                        10)
                                                        cs_xbn2n01b_sl (ncount
                                                                              1 : area
cs_oa22n03c_sl (ncount
                       1 : area
                                  6)
                                                                              Total Area =
                                              1: area
                                                        8)
                      cs_xbo2n01b_sl (ncount
                                               > write_end_point_report -points 2
1943 (Comb = 1393 : Non-Comb = 550)
                                          for file /tmp/end_point_report..147522. [load_update]:
[ET-0018]:>Begin...New EndPoint Report-
Number of pin load calculations: 7350 since last stats [load_update]: Number of pin weight calculations: 0
                                                      Sun Apr 18 21:52:48 1999 Part :
since last stats [ET-0019]:<End.....New Endpoint Report.
                                              EDA EinsTimer EndPoint Report Release Level:
IDCDSUC Mode: Late Mode / Nominal
03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                                         Max. Slack:
                                          Max. Endpoints: 2 Cause of Slack
1.13427E+38 Sort Field: Slack
                                                    ------
Abbreviation Comparison/Description -----
                            Slack due to a point downstream on path Required Arrival Time
                  SlkCont
Continuation
          (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
RAT
( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
                                                                              ClkGSet
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating
                      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
            ClkGHld
Hold
                                                ( CLOCK LEADING EDGE + PULSE WIDTH <
                                     CIKTPW
+ ADJUST ) Clock Tree Pulse Width
                                                      ( DATA ARRIVAL TIME + SETUP <
                                             Setup
CLOCK TRAILING EDGE ) Setup
                                                             ( DATA ARRIVAL TIME - HOLD
CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                    ( DATA ARRIVAL TIME
> CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                         EndOfC
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
                                                                    CIkPW
                                                                               (CLOCK
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation
                                                                                 ClkSep
( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
           ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
ALTest
                                 Slack discontinuity due to failed test
Arrival Time Limiting
                       ATLimit
                                          Delay/. Failed Test/
                                                            Test PinName
LimitedAT/
                                                  P Func T.Adj NetName
           AT Slack Slew CL FO Cell
E Phase
                                                       FC3+R
                                                                1483 -604
                                                                              71 1116 7
                    1 dcd succ_last
                                                                                  879
                       0 dcd succ_last_t1 RAT
 PO
```

```
0 ----> C2744/y
                      F C3+R 1483 -604 71 1116 7 cs invvn01c sl
F C3+R 1368 -604 83 1320 5 cs nnd2n02c st
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y
                                      F C3+R 1368 -604
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
                  R C3+R 1315 -604 118 450 1 cs_nnd2n02c_si
F C3+R 1251 -604
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ----> C2725/a R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs invvn01c_sl 47 N1479 ---->{d} C2721/y
                                      R C3+R 1203 -604 118
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/v
                F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
R C3+R 1086 -604 118
R C3+R 1086 -604 118 61 1.cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1778 ----> C2334/y F C3+R 1021
                                      F C3+R 1021 -604
                                                    71
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{q}
                  R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
C2171/v
F C3+R 909 -604
                                                   71
33 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1696 ----> C1937/y
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
                  R C3+R 868 -604 80 19 1 cs_invvn01c_sl
                                   R C3+R 868
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc
-604 80 19 1 PI 0 dcd_blk_dsucc
R C3+R 1474 -545 108 1116 7
0 ----> C2744/y
              R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 59 N675 ---->{a} C2738/y
                                      FC3+R 1415 -545 83
R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
F C3+R 1304 -545 83
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1097 ---->
                 R C3+R 1255 -545 108 156 1 cs_nnd2n02c_sl
C2728/b
cs_nnd2n02c_sl 49 N1692 ----> C2725/y R
156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ----> C2725/a
                                      R C3+R 1255 -545 108
C3+R 1196 -545 83 293 2 cs_invvn01c_sl cs_invvn01c_sl 59 N1479 ---->{d} C2721/y F C3+R 1196 -545 83 293 2 cs_nnd2n02c_sl
R C3+R 1138 -545
C2550/a2
                  F C3+R 1044 -545 83 61 1 cs ao22n03c sl
cs_ao22n03c_sl 94 N1437 ---->{f} C2427/y
                                      F C3+R 1044 -545
                                                    83
R C3+R 995 -545 108 30 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 49 N1778 ---->
                  R C3+R 995 -545 108 30 1 cs_invvn01c_sl
C2334/v
```

```
FC3+R
                                                                      936
                                                                                   83
               0 N1778 ----> C2334/a
cs_invvn01c_sl
                                                                                       F
                         cs_invvn01c_sl 59 N1119 ---->{g} C2171/y
71 4 cs_invvn01c_sl
                                                  cs_nnd2n02c_sl
                                                                  0 N1119 ---->
                    83
                        71 4 cs nnd2n02c sl
        936 -545
C3+R
                                        887 -545 108 33 1 cs_nnd2n02c_sl
                               R C3+R
C2171/b
                                                              R C3+R
                                                                                    108
cs_nnd2n02c_sl 49 N1696 ----> C1937/v
                                                                        887 -545
                                         0 N1696 ----> C1937/a
                         cs_invvn01c_sl
33 1 cs invvn01c sl
                         19 1 cs_invvn01c_sl cs_invvn01c_sl 58 dcd_blk_dsucc ---->
        829 -545
                    80
C3+R
                                 FC3+R
                                                           19 1 PI
                                           829 -545
                                                     80
dcd_blk_dsucc
dcd_blk_dsucc
                           > cputime Used 18.55 cpu seconds or 00:00:18 wall time, used 458752 bytes
1255.610474
                                                                   > echo {Custom Synzilla
                        > techmap -tlibrary CC8S -seq -timer
or 448 kbytes.
                                      > ps -cell Design /HISVHDL/IDCDSUC has: 1 instances 0
Report  Custom Synzilla Report
                                            763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763
           122 IN ports 73 OUT ports
upcells
                      984 nets (0 multiply-driven; 0 undriven)
                                                                  2585 pins (0 inversions)
           0 buses
                                                                  19 max fanout
                      1528 literals 22 levels
                                            10 max fanin
2.63 pins per net
                                 FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
Cell Information
PSEUDO_REG
               (ncount 83: area
                                   0)
                                                       cb_clk_32_1 (ncount 6: area
                      cb_mode_block (ncount 1: area
                                                       cs_ao22n03c_sl (ncount 17 : area
                       5: area
                                 20)
cs_ao12n03c_sl (ncount
                      cs_invvn01c_sl (ncount 202 : area
                                                       cs_nnd3n02c_sl (ncount 26 : area
cs nnd2n02c sl (ncount 217 : area 651)
                                             8 : area
                      cs nnd4n03c sl (ncount
                                                       cs_nor3n03c_si (ncount
                                                                              1: area
cs_nor2n02c_sl (ncount 12 : area
                                 36)
                      cs_oa21n03c_sl (ncount
                                            2 : area
                                                       10)
                                                       cs xbn2n01b sl (ncount
                                                                             1 : area
cs_oa22n03c_sl (ncount
                       1 : area
                                                                             Total Area =
                      cs_xbo2n01b_sl (ncount
                                             1: area
                                                       8)
                                              > write_end_point_report -points 2
1943 (Comb = 1393 : Non-Comb = 550)
                                          for file /tmp/end_point_report..147522.
[ET-0018]:>Begin...New EndPoint Report
                                         Sun Apr 18 21:52:49 1999 Part : IDCDSUC Mode : Late
[ET-0019]:<End.....New Endpoint Report.
                         EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Mode / Nominal
                                                   Max. Slack: 1.13427E+38 Sort Field: Slack
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                        Abbreviation Comparison/Description -----
Max. Endpoints: 2 Cause of Slack
                                                          Slack due to a point downstream on
                                                SlkCont
----- Slack Continuation
                                       ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                             RAT
                              ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                             ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                  ClkGSet
Gating Setup
                                                           ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                ClkGHld
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                          CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                   Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                   Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                  ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
ClockPulseWidth
                       ClkPW
                                                   ( CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
                                         ClkSep
                                                                    ALTest
                                                                               (DATA
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
                                            Num/
           Slack discontinuity due to failed test
ATLimit
                                          Delay/ Failed Test/ Test PinName
LimitedAT/
                                              P Func T.Adj NetName
           AT Slack Slew CL FO Cell
 E Phase
                                                      F C3+R 1483 -604
                                                                             71 1116 7
                    1 dcd succ_last
                       0 dcd_succ_last_t1 RAT
                                                                                 879
 PO
                                               1483 -604 71 1116 7 cs_invvn01c_sl
                                      F C3+R
 0 ----> C2744/v
```

```
cs_invvn01c_sl 0 dcd_succ_last_t1 ---> C2744/a
                                               R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c sl 0 N675 ---->
C2738/b
                    F C3+R 1368 -604
                                    83 1320 5 cs_nnd2n02c_sl
cs nnd2n02c_sl 68 N1098 ---->{b} C2734/y
                                          F C3+R 1368 -604 83
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
                   R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
F C3+R 1251 -604
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
                    R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs~invvn01c_sl 47 N1479 ---->{d} C2721/y
                                         R C3+R 1203 -604 118
R C3+R 1086 -604 118
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c sl 0 N1437 ---->
C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1778 ----> C2334/y F C3+R 1021 -30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a
                                         FC3+R 1021 -604
                                                         71
                                                         R
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
                  R C3+R 974 -604 118 71 4 cs_nnd2n02c sl
C2171/v
cs nnd2n02c sl 0 N1119 ----> C2171/b
                                         FC3+R 909 -604
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc
                                       R C3+R 868
-604 80 19 1 PI 0 dcd_blk_dsucc
             ∠ ucu_succ_last R C3+R 1474 -545 108 1116 7 0 dcd_succ_last_t1 RAT
----- 2 dcd_succ_last
0 ----> C2744/y
                        R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                               F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---> C2738/b R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y
                                          R C3+R 1365 -545 118
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
                   F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl
C2728/y
R C3+R 1255 -545 108
R C3+R 1255 -545 108 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
                    F C3+R 1196 -545 83 293 2 cs_invvn01c_sl
C2725/a
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y
                                         FC3+R 1196 -545
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
                   R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl
.
                                          FC3+R 1044 -545
                                                         83
FC3+R 1044 -545 83 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 --->
C2427/b
           R C3+R 995 -545 108 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 49 N1778 ----> C2334/y
                                         R C3+R 995 -545 108
```

```
30 1 cs invvn01c sl
                         cs invvn01c sl 0 N1778 ----> C2334/a
        936 -545
                    83
                         71 4 cs invvn01c sl
                                                   cs invvn01c sl 59 N1119 ---->{g} C2171/y
C3+R
                          71 4 cs_nnd2n02c_sl
                                                      cs_nnd2n02c_sl
                                                                      0 N1119 --->
          936 -545
FC3+R
                      83
                                                      108
                                                            33 1 cs_nnd2n02c_sl
                                R C3+R
                                          887 -545
C2171/b
                                                                R C3+R
                                                                          887
                                                                               -545
                                                                                      108
cs nnd2n02c sl 49 N1696 ---> C1937/y
                         33 1 cs invvn01c sl
                                                 cs_invvn01c_sl 58 dcd_blk_dsucc ---->
        829 -545
                    80
                         19 1 cs_invvn01c_sl
C3+R
                                  FC3+R
                                            829 -545
                                                       80 19 1 PI
dcd_blk_dsucc
dcd blk_dsucc
                            > report area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
                       > cputime Used 0.99 cpu seconds or 00:00:01 wall time, used 131072 bytes
1255.610474
                        > freeze net loads -reset [TIMER-6411]: Unasserted load on 369 inet(s).
or 128 kbytes.
> resize -trace 0 -local -mincut -inc -sequential -ana 100... resize
                                                                    Area: before 5081.39 after
                      Slack: before -603.6691 after -603.6691 (0.00 %) Cell: before 763 after 763
5081.39 (0.00 %)
           Time: 1.750000
                                      > freeze_net_loads -set -limit [TIMER-6412]: Asserted load
(0.00\%)
                          > echo {Custom Synzilla Report} Custom Synzilla Report
on 369 inet(s).
ps -cell Design /HISVHDL/IDCDSUC has:
                                            1 instances 0 upcells
                                                                    122 IN ports 73 OUT ports
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC)
                                                                    0 buses
                                                                               984 nets (0
                                  2585 pins (0 inversions) 2.63 pins per net
                                                                               1528 literals
multiply-driven; 0 undriven)
                                                        Cell Information
                                  19 max fanout
22 levels
           10 max fanin
                                                                    PSEUDO_REG
                                                                                    (ncount
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                    0)
                                  cb_clk_32_1 (ncount
                                                                  480)
                                                        6 : area
83 : area
           0)
                                  70)
                                                        cs ao12n03c_sl (ncount 5 : area
cb mode_block (ncount 1: area
                      cs_ao22n03c_sl (ncount 17: area
                                                        102)
20)
                                                        cs_nnd2n02c_sl (ncount 217: area
cs invvn01c sl (ncount 202 : area
                                 404)
                      cs nnd3n02c_sl (ncount
                                              26 : area
                                                        104)
                                                        cs nor2n02c_sl (ncount 12 : area
                                  40)
cs nnd4n03c_sl (ncount
                       8 : area
                      cs_nor3n03c_sl (ncount
                                              1 : area
                        2: area
                                                        cs_oa22n03c_sl (ncount
                                                                                1 : area
cs_oa21n03c_sl (ncount
                                  10)
                       cs_xbn2n01b_sl (ncount
                                              1: area
                                                         8)
                                                         Total Area = 1943 (Comb = 1393:
cs xbo2n01b_sl (ncount 1 : area
                                  8)
                              > write end point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550
             for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Report
Sun Apr 18 21:52:56 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                           EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
                        Max. Slack: 1.13427E+38 Sort Field: Slack
-1.13427E+38
                                     Abbreviation Comparison/Description -----
Endpoints: 2 Cause of Slack
                                                 SlkCont
                                                            Slack due to a point downstream on
                          Slack Continuation
                                        ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
                              RAT
path Required Arrival Time
                               ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                             ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                  ClkGSet
Gating Setup
                                                             ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                 CIKGHId
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                            CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                     Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                      Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        CIkPW
ClockPulseWidth
                                                    ( CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
                                          ClkSep
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                      ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
           Slack discontinuity due to failed test
                                             Num/
ATLimit
                                                              Test PinName
                                           Delay/ Failed Test/
LimitedAT/
           AT Slack Slew CL FO Cell
                                                  P Func T.Adj NetName
E Phase
```

```
----- 1 dcd_succ_last
                                     FC3+R 1483 -604 71 1116 7
                0 dcd_succ_last_t1 RAT
                                                          879
0 ----> C2744/y
                         F C3+R 1483 -604 71 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                  R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
                    F C3+R 1368 -604 83 1320 5 cs_nnd2n02c_sl
C2738/b
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y
                                             FC3+R 1368 -604
                                                             83
C2728/y
                     R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 0 N1097 ----> C2728/b
                                            F C3+R 1251 -604
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ----> C2725/a R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs invvn01c sl 47 N1479 ---->{d} C2721/v
                                             R C3+R 1203 -604
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
                   F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
C2550/v
R C3+R 1086 -604 118
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
                      F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl
C2427/b
cs_nnd2n02c_sl 64 N1778 ----> C2334/y
                                            F C3+R 1021 -604
                                                             71
R
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
                     R C3+R 974 -604 118 71 4 cs nnd2n02c sl
cs nnd2n02c sl 0 N1119 ----> C2171/b
                                            F C3+R
                                                   909 -604
                                                            71
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a R C3+R 868 -604 80 19 1 cs_invvn01c_sl
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd_blk_dsucc
                                                   R C3+R
-604 80 19 1 PI 0 dcd_blk_dsucc
----- 2 dcd_succ_last
                                R C3+R 1474 -545 108 1116 7
            0 dcd_succ_last_t1 RAT
0 ----> C2744/y R C3+H cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                          R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
                                                  F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c sl cs_nnd2n02c sl 0 N675 ---->
C2738/b
                    R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y
                                             R C3+R 1365 -545 118
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
C2728/y
                    F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl
cs nnd2n02c sl 0 N1097 ----> C2728/b
                                            R C3+R 1255 -545 108
R C3+R 1255 -545 108 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---> C2725/a F C3+R 1196 -545 83 293 2 cs_invvn01c_sl
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y
                                .
                                            FC3+R 1196 -545
                                                             83
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
                    R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl
C2550/y
F C3+R 1044 -545
```

```
cs ao22n03c_sl 94 N1437 ---->{f} C2427/v
61 1 cs_ao22n03c_sl
                      83 61 1 cs_nnd2n02c_sl
                                                      cs_nnd2n02c_sl
                                                                       0 N1437 ---->
FC3+R
         1044 -545
                                                          30 1 cs nnd2n02c_sl
                               RC3+R
                                         995 -545
                                                     108
C2427/b
cs nnd2n02c_sl 49 N1778 ----> C2334/y
                                                               R C3+R
                                                                         995 -545
                                                                                     108
                                         0 N1778 ---> C2334/a
30 1 cs_invvn01c_sl
                         cs invvn01c_sl
                                                  cs_invvn01c_sl 59 N1119 ---->{g} C2171/y
                    83
                         71 4 cs_invvn01c_sl
C3+R
        936 -545
                                                     83
                         71 4 cs_nnd2n02c_sl
FC3+R
         936 -545
                                                     108 33 1 cs_nnd2n02c_sl
                                         887 -545
C2171/b
                               R C3+R
cs nnd2n02c_sl 49 N1696 ----> C1937/v
                                                               R C3+R
                                                                         887 -545
                                                                                     108
                                         0 N1696 ----> C1937/a
                         cs invvn01c_sl
33 1 cs_invvn01c_sl
                         19 1 cs_invvn01c_sl
                                                  cs invvn01c sl 58 dcd_blk_dsucc ---->
C3+R
        829 -545
                    80
                                                                                       0
                                 FC3+R
                                           829
                                                -545
                                                       80 19 1 PI
dcd_blk_dsucc
dcd_blk_dsucc
                             > report_area    Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
                        > cputime Used 5.71 cpu seconds or 00:00:06 wall time, used 0 bytes or 0
1255.610474
                > echo {Custom Synzilla Report} Custom Synzilla Report
                                                                             > ps -cell
byte.
                                                        122 IN ports 73 OUT ports
                                 1 instances 0 upcells
Design /HISVHDL/IDCDSUC has:
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC)
                                                                  0 buses
                                                                              984 nets (0
                                                                              1528 literals
                                 2585 pins (0 inversions) 2.63 pins per net
multiply-driven; 0 undriven)
                                                        Cell Information
                                 19 max fanout
22 levels
           10 max fanin
                                                                   PSEUDO_REG
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                                                   (ncount
                                                    0)
                                 cb_clk_32_1 (ncount
                                                       6: area
                                                                480)
83 : area
           0)
                                                        cs_ao12n03c_sl (ncount 5: area
cb mode_block (ncount 1: area
                                 70)
                      cs ao22n03c_sl (ncount 17 : area
                                                       102)
                                                        cs_nnd2n02c_si (ncount 217 : area
cs_invvn01c_sl (ncount 202 : area
                                404)
                      cs_nnd3n02c_sl (ncount
                                             26: area
                                                        104)
                                                        cs_nor2n02c_sl (ncount 12 : area
cs_nnd4n03c_sl (ncount
                       8: area 40)
                      cs nor3n03c_sl (ncount
                                             1 : area
                                                        cs_oa22n03c_sl (ncount
                       2 : area
                                 10)
cs_oa21n03c_sl (ncount
                      cs_xbn2n01b_sl (ncount
                                                        8)
                                              1: area
                                                        Total Area = 1943 (Comb = 1393:
cs_xbo2n01b_sl (ncount 1 : area
                                  8)
                            > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550
             for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Report
Sun Apr 18 21:52:57 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                          EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
                       Max. Slack: 1.13427E+38 Sort Field: Slack
                                                                             Max.
-1.13427E+38
                                    Abbreviation Comparison/Description ------
Endpoints: 2 Cause of Slack
                                                           Slack due to a point downstream on
----- Slack Continuation
                                                SlkCont
                                       ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                             RAT
                               ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                             ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                  ClkGSet
                                                            ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                 CIkGHId
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                           CIKTPW
                                                                                     . (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                    Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                    Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                  ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
ClockPulseWidth
                       ClkPW
                                                   ( CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
                                         ClkSep
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                     ALTest
                                                                                (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
                                             Num/
          Slack discontinuity due to failed test
ATLimit
                                          Delay/ Failed Test/
                                                             Test PinName
LimitedAT/
                                                  P Func T.Adj NetName
E Phase
          AT Slack Slew CL FO Cell
```

```
----- 1 dcd_succ_last
                                     FC3+R 1483 -604 71 1116 7
PO
             0 dcd_succ_last_t1 RAT
                                                        879
0 ----> C2744/v
                       F C3+R 1483 -604 71 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
                    F C3+R 1368 -604 83 1320 5 cs_nnd2n02c_sl
C2738/b
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y
                                           FC3+R 1368 -604
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N1097 ---->{c}
C2728/y
                    R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
F C3+R 1251 -604
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---->
C2725/a
                    R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y
                                          R C3+R 1203 -604
C2550/v
               F C3+R 1137 -604 105 108 1 cs_ao22n03c sl
R C3+R 1086 -604 118
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---> C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl
C2427/D CS_nnd2n02c_sl 64 N1778 ----> C2334/y
                                          F C3+R 1021 -604
                                                          71
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
                    R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
F C3+R 909 -604 71
F C3+R 909 -604 71 33 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1696 ---->
C1937/a R C3+R 868 -604 80 19 1 cs_invvn01c_sl
cs_invvn01c_sl 41 dcd_bjk_dsucc ---> dcd_blk_dsucc
                                                R C3+R 868
-604 80 19 1 PI 0 dcd_blk_dsucc
----- 2 dcd_succ_last
                                R C3+R 1474 -545 108 1116 7
           0 dcd_succ_last_t1 RAT
0 ----> C2744/y R C3+R 14 cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                     R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
                                                F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
FC3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 --->
                  R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
C2738/b
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y R C3 1320 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1098 ----> C2734/a
                                           R C3+R 1365 -545 118
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
                    F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl
R C3+R 1255 -545 108
F C3+R 1196 -545 83 293 2 cs_invvn01c_sl
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y
                              -
                                         F C3+R 1196 -545
                                                          83
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
      R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl
C2550/v
FC3+R 1044 -545 83
```

```
cs_ao22n03c_sl 94 N1437 ---->{f} C2427/v
61 1 cs ao22n03c sl
                                                                      0 N1437 ---->
                                                     cs nnd2n02c_sl
FC3+R
        1044 -545
                      83
                           61 1 cs_nnd2n02c_si
                                         995 -545
                                                     R C3+R
C2427/b
                                                                                    108
                                                              R C3+R
                                                                        995 -545
cs nnd2n02c_sl 49 N1778 ----> C2334/v
                         cs invvn01c_sl
                                         0 N1778 ----> C2334/a
30 1 cs invvn01c si
                                                 cs_invvn01c_sl 59 N1119 ---->{g} C2171/y
                        71 4 cs_invvn01c_sl
        936 -545
                    83
C3+R
                                                    FC3+R
         936 -545
                      83
                         71 4 cs_nnd2n02c_sl
                               R C3+R
                                         887 -545
                                                    108
                                                          33 1 cs_nnd2n02c_sl
C2171/b
                                                              R C3+R
                                                                        887 -545
                                                                                    108
cs_nnd2n02c_sl 49 N1696 ----> C1937/y
                                         0 N1696 ----> C1937/a
                         cs_invvn01c_sl
33 1 cs invvn01c sl
                                                 cs_invvn01c_sl 58 dcd_blk_dsucc ---->
                        19 1 cs_invvn01c_sl
        829 -545
                    80
C3+R
                                                       80 19 1 PI
                                 F C3+R
                                           829 -545
dcd blk_dsucc
dcd blk dsucc
                           > report area Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
                       > cputime Used 1.20 cpu seconds or 00:00:01 wall time, used 0 bytes or 0
1255.610474
               > echo {Custom Synzilla Report} Custom Synzilla Report
                                                                          > ps -cell Design
                                1 instances 0 upcells
                                                       122 IN ports 73 OUT ports
/HISVHDL/IDCDSUC has:
763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0 UNLINKED; 0 DC) 0 buses
                                                                             984 nets (0
                                 2585 pins (0 inversions) 2.63 pins per net
multiply-driven; 0 undriven)
                                                                             1528 literals
                                 19 max fanout
                                                       Cell Information
22 levels
           10 max fanin
                                                                  PSEUDO_REG
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                   0)
                                                                                  (ncount
                                 cb_clk_32_1 (ncount
                                                       6 : area
                                                                480)
83 : area
           0)
                                                       cs_ao12n03c_sl (ncount
                                 70)
cb mode block (ncount 1: area
                      cs ao22n03c sl (ncount 17: area
20)
                                                       cs nnd2n02c_sl (ncount 217 : area
cs_invvn01c_sl (ncount 202 : area
                                 404)
                      cs_nnd3n02c_sl (ncount 26 : area
                                                       104)
                                                       cs_nor2n02c_sl (ncount 12 : area
                       8 : area
                                 40)
cs_nnd4n03c_sl (ncount
                      cs_nor3n03c_sl (ncount
                                             1 : area
                                                       4)
                                                       cs_oa22n03c_sl (ncount
                                                                              1: area
cs_oa21n03c_sl (ncount
                       2 : area
                                 10)
                      cs_xbn2n01b_sl (ncount
                                             1: area
                                                        8)
                                                       Total Area = 1943 (Comb = 1393:
cs_xbo2n01b_sl (ncount 1 : area
                                  8)
                           > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550
             for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Report
Sun Apr 18 21:52:58 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                         EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
                       Max. Slack: 1.13427E+38 Sort Field: Slack
-1.13427E+38
                                    Abbreviation Comparison/Description -----
Endpoints: 2 Cause of Slack
                                                          Slack due to a point downstream on
                                                SIkCont
------
                         Slack Continuation
                                       ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                             RAT
                              ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                             ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
Gating Setup
                  ClkGSet
                                                           ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                ClkGHld
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                          CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                   Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                    Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                  ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                       CIkPW
ClockPulseWidth
                                                   ( CLOCK1 ARRIVAL TIME + CLOCK
                                         ClkSep
TRAILING EDGE ) ClockSeparation
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                     ALTest
                                                                               (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
          Slack discontinuity due to failed test
                                            Num/
ATLimit
                                          Delay/ Failed Test/ Test PinName
LimitedAT/
                                                 P Func T.Adj NetName
          AT Slack Slew CL FO Cell
E Phase
```

```
----- 1 dcd_succ_last
                                      FC3+R 1483 -604 71 1116 7
                0 dcd_succ_last_t1 RAT
                                                         879
0 ----> C2744/v
                        F C3+R 1483 -604 71 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                 R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
                     F C3+R 1368 -604 83 1320 5 cs_nnd2n02c_sl
C2738/b
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y
                                            F C3+R 1368 -604
                                                            83
C2728/v
            R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
FC3+R 1251 -604 71
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ----> C2725/a R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y
                                           R C3+R 1203 -604 118
F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
C2550/v
R C3+R 1086 -604 118
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---> C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 64 N1778 ----> C2334/y F
30 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1778 ----> C2334/a
                                           FC3+R 1021 -604
                                                           71
C3+R 974 -604 118 71 4 cs_invvn01c_sl cs_invvn01c_sl 47 N1119 ---->{g}
                    R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
cs nnd2n02c sl 0 N1119 ----> C2171/b
                                         F C3+R 909 -604 71
cs_invvn01c_sl 41 dcd_blk_dsucc ---> dcd_blk_dsucc
                                                 R C3+R
-604 80 19 1 PI 0 dcd_blk_dsucc
----- 2 dcd_succ_last
                                R C3+R 1474 -545 108 1116 7
            0 dcd_succ_last_t1 RAT
0 ----> C2744/y R C3+H cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                    R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
                                                 F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
                  R C3+R 1365 \ -545 118 1320 5 cs_nnd2n02c_sl
C2738/b
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y
                                            R C3+R 1365 -545 118
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
                    F C3+R 1304 -545 83 450 1 cs nnd2n02c sl
R C3+R 1255 -545 108
R C3+R 1255 -545 108 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ---> C2725/a F C3+R 1196 -545 83 293 2 cs_invvn01c_sl
cs_invvn01c_sl 59 N1479 ---->{d} C2721/y
                                .
                                           FC3+R 1196 -545
                                                           83
R C3+R 1138 -545 170 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 59 N1858 ---->{e}
                   R C3+R 1138 -545 170 108 1 cs_ao22n03c_sl
C2550/y
F C3+R 1044 -545
```

```
cs_ao22n03c_sl 94 N1437 ---->{f} C2427/v
61 1 cs ao22n03c_sl
                                                                       0 N1437 ---->
                                                      cs nnd2n02c_sl
F C3+R
        1044 -545
                      83
                           61 1 cs_nnd2n02c_sl
                                         995 -545
                                                     108 30 1 cs nnd2n02c_sl
                               R C3+R
C2427/b
                                                                          995 -545
                                                                                      108
                                                               R C3+R
cs nnd2n02c_sl 49 N1778 ---> C2334/y
                         cs_invvn01c_sl
                                         0 N1778 ----> C2334/a
30 1 cs_invvn01c_sl
                                                   cs_invvn01c_sl 59 N1119 ---->{g} C2171/y
        936 -545
                    83
                         71 4 cs invvn01c_sl
C3+R
                                                     83
                          71 4 cs nnd2n02c_sl
         936 -545
FC3+R
                                                           33 1 cs_nnd2n02c_sl
                               RC3+R
                                         887 -545
                                                     108
C2171/b
cs nnd2n02c_sl 49 N1696 ----> C1937/y
                                                                R C3+R
                                                                         887
                                                                              -545
                                                                                      108
                                          0 N1696 ----> C1937/a
33 1 cs_invvn01c_sl
                         cs_invvn01c_sl
                                                   cs_invvn01c_sl 58 dcd_blk_dsucc ---->
                         19 1 cs_invvn01c_sl
                    80
        829 -545
                                                                                        0
                                                        80 19 1 PI
                                           829
                                                -545
dcd_blk_dsucc
                                 FC3+R
dcd blk_dsucc
                           > cputime Used 0.93 cpu seconds or 00:00:01 wall time, used 0 bytes or 0
1255.610474
            > echo {=== Technology mapping process finished ===} === Technology mapping process
byte.
                                                                                   Count
                  > load update -invalidate Good names for IDCDSUC
finished ===
                                                                    447 For all nets
                   New For all nets
                                              984
                                                     537
User Transform
                                                                         0.00%
                                                                                  29.35%
                 0.00%
                         45.43% For I/O port nets
                                                         184
                                                               70.65%
      54.57%
                                                                             Count
                                100.00%
                                           0.00%
                                                     0.00%
                          166
For register output nets
                                                                    493 For all boxes
User Transform
                                               763
                                                      270
                   New For all boxes
                                                               100.00%
                                                                          0.00%
                                                                                    0.00%
                         64.61% For register boxes
                                                          83
      35.39%
                 0.00%
763
                                                                   > echo {Custom Synzilla
                                                  64.61%
For linked boxes
                        763
                               35.39%
                                         0.00%
                                     > ps -cell Design /HISVHDL/IDCDSUC has:
                                                                               1 instances 0
Report) Custom Synzilla Report
                                             763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763
           122 IN ports 73 OUT ports
                                             984 nets (0 multiply-driven; 0 undriven)
                                  0 buses
LINKED: 0 UNLINKED: 0 DC)
                                             1528 literals 22 levels
                                                                    10 max fanin
2585 pins (0 inversions) 2.63 pins per net
                                                        FUNC STRAIGHT_WIRE_DESIGN
                      Cell Information
19 max fanout
                                                            (ncount 83 : area
                                             PSEUDO_REG
(ncount 180: area
                     0)
                                                        cb_mode_block (ncount
                                                                                1: area
cb_clk_32_1 (ncount
                      6 : area
                               480)
                      cs_ao12n03c_sl (ncount
                                              5: area
70)
                                                        cs_invvn01c_sl (ncount 202 : area
                                 102)
cs_ao22n03c_sl (ncount 17 : area
                       cs nnd2n02c_sl (ncount 217 : area
                                                         651)
404)
                                                         cs nnd4n03c_sl (ncount
                                                                                8: area
cs_nnd3n02c_sl (ncount 26 : area
                                 104)
                                                         36)
                       cs_nor2n02c_sl (ncount 12 : area
40)
                                                         cs_oa21n03c_sl (ncount
                                                                                2: area
                       1 : area
                                  4)
cs_nor3n03c_sl (ncount
                                                         6)
                       cs_oa22n03c_sl (ncount 1: area
                                                         cs_xbo2n01b_sl (ncount
                                                                                1 : area
                       1 : area
cs_xbn2n01b_sl (ncount
                                  8)
                       Total Area = 1943 (Comb = 1393 : Non-Comb = 550)
write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
                                                                        for file
/tmp/end_point_report..147522. [load_update]: Number of pin load calculations: 7541 since last stats
[load_update]: Number of pin weight calculations: 0 since last stats [ET-0019]:<End.....New Endpoint
             Sun Apr 18 21:52:59 1999 Part : IDCDSUC Mode : Late Mode / Nominal
EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min.
                              Max. Slack: 1.13427E+38 Sort Field: Slack
Slack: -1.13427E+38
                                     Abbreviation Comparison/Description ------
Endpoints: 2 Cause of Slack
                                                            Slack due to a point downstream on
                                                 SIkCont
------
                         Slack Continuation
                                        ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
                              RAT
path Required Arrival Time
                               ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                              ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                   ClkGSet
Gating Setup
                                                             ( DATA ARRIVAL TIME - CLOCK
 ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                 ClkGHld
 GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                            CIKTPW
 CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                     Setup
 ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                     Hold
```

```
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
        (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST)
ClockPulseWidth
                ClkPW
                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation
                             ClkSep (CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
       Slack discontinuity due to failed test Num/
LimitedAT/
                             Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell
                                   P Func T.Adj NetName
----- 1 dcd_succ_last
                                     FC3+R 1483 -604 71 1116 7
               0 dcd_succ_last_t1 RAT
                                                          879
0 ----> C2744/y
                         F C3+R 1483 -604 71 1116 7 cs invvn01c sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                  R C3+R 1435
-604 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
R C3+R 1435 -604 118 384 4 cs_nnd2n02c_sl cs nnd2n02c_sl 0 N675 ---->
                     F C3+R 1368 -604
C2738/b
                                      83 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ---->{b} C2734/y
                                      F C3+R 1368 -604
R C3+R 1315 -604 118 450 1 cs_nnd2n02c_sl
F C3+R 1251 -604
F C3+R 1251 -604 71 156 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1692 ----> C2725/a R C3+R 1203 -604 118 293 2 cs_invvn01c_sl
cs_invvn01c_sl 47 N1479 ---->{d} C2721/y
                                            R C3+R 1203 -604 118
F C3+R 1137 -604 105 108 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 67 N1858 ---->{e}
C2550/y
                   F C3+R 1137 -604 105 108 1 cs_ao22n03c_sl
R C3+R 1086 -604
                                                           118
R C3+R 1086 -604 118 61 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1437 ---->
C2427/b F C3+R 1021 -604 71 30 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 64 N1778 ----> C2334/y F C3+R 1021 -
                                            FC3+R 1021 -604
                                                            71
R
     C3+R
                      R C3+R 974 -604 118 71 4 cs_nnd2n02c_sl
FC3+R
                                                   909 -604
                                                            71
0 N1696 ---->
cs_invvn01c_sl 41 dcd_blk_dsucc ----> dcd blk dsucc
                                                 R C3+R
-604 80 19 1 PI 0 dcd_blk_dsucc
----- 2 dcd_succ_last
                                     R C3+R 1474 -545 108 1116 7
              0 dcd_succ_last_t1 RAT
0 ----> C2744/y
                          R C3+R 1474 -545 108 1116 7 cs_invvn01c_sl
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                  F C3+R 1415
-545 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
F C3+R 1415 -545 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ----> C2738/b R C3+R 1365 -545 118 1320 5 cs_nnd2n02c_sl
cs_nnd2n02c_sl 50 N1098 ---->{b} C2734/y
                                             R C3+R 1365 -545 118
F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 61 N1097 ---->{c}
C2728/v
                     F C3+R 1304 -545 83 450 1 cs_nnd2n02c_sl
```

```
cs_nnd2n02c_sl
                            cs nnd2n02c sl
                                            49 N1692 ----> C2725/v
156 1 cs_nnd2n02c_sl
                                                       cs invvn01c_sl
                                                                        0 N1692 ---->
                            156 1 cs_invvn01c_sl
RC3+R
         1255 -545
                       108
                                                       83 293 2 cs_invvn01c_sl
                                FC3+R
                                         1196 -545
C2725/a
                                                                          1196 -545
                                                                                        83
                                                                 FC3+R
                59 N1479 ---->{d} C2721/y
cs invvn01c sl
                                             0 N1479 ---->
                                                            C2721/a
                            cs nnd2n02c sl
293 2 cs_nnd2n02c_sl
                                                        cs_nnd2n02c sl
                                                                          59 N1858 ---->{e}
                           108 1 cs_nnd2n02c_sl
         1138 -545
                       170
R C3+R
                                                       170 108 1 cs_ao22n03c_sl
                                          1138 -545
                                RC3+R
C2550/v
                                                                                        83
                                                                 FC3+R
                                                                          1044 -545
                 0 N1858 ---->
                                C2550/a2
cs ao22n03c_sl
                                            94 N1437 ---->{f} C2427/y
                           cs_ao22n03c_sl
61 1 cs ao22n03c_sl
                                                       cs nnd2n02c_sl
                                                                         0 N1437 ---->
         1044 -545
                       83
                            61 1 cs nnd2n02c_sl
FC3+R
                                                            30 1 cs nnd2n02c_sl
                                RC3+R
                                           995 -545
                                                       108
C2427/b
                                                                                       108
                                                                 RC3+R
                                                                           995 -545
                49 N1778 ----> C2334/v
cs nnd2n02c sl
                                           0 N1778 ----> C2334/a
30 1 cs invvn01c_sl
                          cs invvn01c sl
                                                    cs invvn01c sl 59 N1119 ---->{g} C2171/y
        936 -545
                     83
                          71 4 cs_invvn01c_sl
C3+R
                           71 4 cs_nnd2n02c_sl
                                                      cs_nnd2n02c_sl
                                                                        0 N1119 ---->
          936 -545
                      83
FC3+R
                                RC3+R
                                          887 -545
                                                      108
                                                             33 1 cs_nnd2n02c_sl
C2171/b
                                                                 R C3+R
                                                                           887 -545
                                                                                       108
                49 N1696 ---->
                                C1937/v
cs_nnd2n02c_sl
                          cs_invvn01c_sl
                                           0 N1696 ----> C1937/a
33 1 cs_invvn01c_sl
                                                    cs_invvn01c_sl 58 dcd_blk_dsucc ---->
                     80
                          19 1 cs_invvn01c_sl
C3+R
        829 -545
                                   FC3+R
                                                 -545
                                                         80
                                                              19 1 PI
                                             829
dcd blk dsucc
dcd blk dsucc
                        > report_area    Design: /IDCDSUC - Area: 5081.386230, Area(Weight):
                      > cputime Used 1.45 cpu seconds or 00:00:01 wall time, used 0 bytes or 0 byte.
1255.610474
[hnl attr]: Attributes registered for copy for type: PORT. MASK_ANYTHING_MASKED_ON_PORT
[hnl_attr]: Attributes registered for copy for type: CELL. MASK_ANYTHING_MASKED_ON_CELL
MASK USER CELL NOCHANGE MASK_USER_CELL_NODESTROY
MASK_USER_CELL_NOTOUCH SUGGESTED_LIBRARY_CELL SUGGESTED_PARALLEL_FANOUT
SUGGESTED_SIZE SUGGESTED_SWAP SYN_USAGE_BOX_HIDE [hnl_attr]: Attributes registered for
copy for type: PIN. MASK_ANYTHING_MASKED_ON_PIN MASK_USER_PIN_NOADD
MASK_USER_PIN_NOCHANGE MASK_USER_PIN_NONEWNET MASK_USER_PIN_NOTOUCH
SUGGESTED_SERIAL_FANOUT SYN_SAS_NAME [hnl_attr]: Attributes registered for copy for type:
NET. MASK_ANYTHING_MASKED_ON_NET MASK_USER_NET_NOTOUCH [hnl_attr]: 0 port(s) have
attribute(s) registered for copy. [hnl_attr]: 197 cell(s) have attribute(s) registered for copy. [hnl_attr]: 10
net(s) have attribute(s) registered for copy. [hnl_attr]: 1242 pin(s) have attribute(s) registered for copy.
> echo {=== CDS process ===} === CDS process === Loading:
                                                                       > time units -nano
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/tcl/cds_disc.tcl
                                                        > echo {Custom Synzilla Report} Custom
                           > reset timing area
> time_units -nano
                         > ps -cell Design /HISVHDL/IDCDSUC has:
                                                                     1 instances 0 upcells
Synzilla Report
                                   763 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 763 LINKED; 0
122 IN ports 73 OUT ports
                                   984 nets (0 multiply-driven; 0 undriven)
                                                                                 2585 pins (0
UNLINKED; 0 DC)
                       0 buses
                                   1528 literals 22 levels
                                                         10 max fanin
                                                                                 19 max fanout
inversions) 2.63 pins per net
                                   FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
Cell Information
                                                          cb clk 32_1 (ncount
                                                                                6: area
                 (ncount 83: area
                                     0)
PSEUDO_REG
                       cb mode block (ncount
                                               1 : area
480)
                                                          cs_ao22n03c_sl (ncount 17: area
                        5: area
                                  20)
cs_ao12n03c_sl (ncount
                       cs invvn01c_sl (ncount 202 : area
                                                         404)
                                                          cs nnd3n02c_sl (ncount 26 : area
cs_nnd2n02c_sl (ncount 217 : area
                                   651)
                       cs nnd4n03c_sl (ncount
                                               8 : area
104)
                                                          cs_nor3n03c_sl (ncount
                                                                                  1: area
                       12 : area
                                   36)
cs nor2n02c sl (ncount
                       cs oa21n03c_si (ncount
                                               2: area
                                                          cs_xbn2n01b_sl (ncount
                                                                                  1 : area
                        1 : area
cs_oa22n03c_sl (ncount
                                   6)
                                                                                 Total Area =
                                                1: area
                       cs xbo2n01b_sl (ncount
8)
                                                > write_end_point_report -points 2
1943 (Comb = 1393 : Non-Comb = 550)
```

0 N1097 ---->

C2728/b

108

1255 -545

RC3+R

```
[ET-0018]:>Begin...New EndPoint Report
                                         for file /tmp/end_point_report..147522.
[ET-0019]:<End....New Endpoint Report.
                                        Sun Apr 18 21:53:03 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                         EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                   Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack
                                        Abbreviation Comparison/Description -----
------
                        Slack Continuation
                                               SlkCont
                                                         Slack due to a point downstream on
path Required Arrival Time
                            RAT
                                      (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT
                              ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                 ClkGSet
                            ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                               ClkGHld
                                                          ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                         CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                 Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                  Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
EndOfC
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
ClockPulseWidth
                      ClkPW
                                 ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation
                                                  ( CLOCK1 ARRIVAL TIME + CLOCK
                                        ClkSep
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                   ALTest
                                                                             (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
ATLimit
          Slack discontinuity due to failed test
                                           Num/
LimitedAT/
                                        Delay/ Failed Test/ Test PinName
E Phase
          AT Slack Slew CL FO Cell
                                                P Func T.Adj NetName
                   1 dcd succ last
                                                     FC3+R
                                                              1483 -604
                                                                           71 1172 7
PO
                      0 dcd_succ_last_t1 RAT
                                                                                879
0 ----> C2744/y
                                     FC3+R
                                              1483 -604
                                                            71 1172 7 cs_invvn01c sl
cs_invvn01c sl
               0 dcd_succ_last_t1 ---> C2744/a
                                                                     R C3+R 1435
-604 118 416 4 cs_invvn01c_sl
                                                    47 N675 ---->{a} C2738/y
                                     cs_invvn01c_sl
R C3+R 1435 -604 118 416 4 cs_nnd2n02c_sl
                                                     cs_nnd2n02c_sl
                                                                      0 N675 ---->
C2738/b
                              FC3+R
                                       1368 -604
                                                    83 1360 5 cs nnd2n02c sl
                68 N1098 ---->{b} C2734/y
cs_nnd2n02c_sl
                                                              FC3+R
                                                                       1368 -604
                                                                                    83
1360 5 cs_nnd2n02c sl
                           cs_nnd2n02c_sl
                                            0 N1098 ----> C2734/a
                     118 458 1 cs_nnd2n02c_sl
R C3+R
        1315 -604
                                                     cs_nnd2n02c_sl
                                                                    52 N1097 ---->{c}
C2728/v
                              R C3+R
                                       1315 -604
                                                    118 458 1 cs_nnd2n02c_sl
cs nnd2n02c sl
                0 N1097 ---->
                              C2728/b
                                                             FC3+R
                                                                      1251 -604
                                                                                   71.
164 1 cs_nnd2n02c sl
                          cs_nnd2n02c_sl 64 N1692 ---->
                                                         C2725/v
        1251 -604
                          164 1 cs_invvn01c sl
F C3+R
                      71
                                                    cs_invvn01c_sl
                                                                    0 N1692 ---->
C2725/a
                              RC3+R
                                       1203 -604
                                                    118 309 2 cs_invvn01c_sl
cs_invvn01c_sl
               47 N1479 ---->{d} C2721/y
                                                             R C3+R
                                                                     1203 -604
                                                                                   118
309 2 cs_nnd2n02c_sl
                          cs nnd2n02c sl
                                           0 N1479 ---->
                                                         C2721/a
        1137 -604
FC3+R
                     105 116 1 cs_nnd2n02c_sl
                                                     cs_nnd2n02c_sl
                                                                     67 N1858 ---->{e}
C2550/y
                              FC3+R
                                      1137 -604
                                                    105 116 1 cs ao22n03c sl
cs_ao22n03c_sl
                0 N1858 ----> C2550/a2
                                                             R C3+R
                                                                      1086 -604
                                                                                   118
69 1 cs_ao22n03c sl
                         cs_ao22n03c_sl 51 N1437 ---->{f} C2427/v
R C3+R
         1086 -604
                     118 69 1 cs_nnd2n02c sl
                                                     cs_nnd2n02c_sl
                                                                     0 N1437 ---->
C2427/b
                              F C3+R
                                       1021 -604
                                                    71
                                                         38 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl 64 N1778 ----> C2334/y
                                                             FC3+R
                                                                      1021 -604
                                                                                   71
38 1 cs invvn01c sl
                        cs_invvn01c_sl
                                        0 N1778 ----> C2334/a
                                                                                    R
C3+R
        974 -604
                   118 103 4 cs_invvn01c_sl
                                                  cs_invvn01c_si 47 N1119 ---->{g}
C2171/v
                              R C3+R
                                        974 -604
                                                  118 103 4 cs_nnd2n02c sl
cs_nnd2n02c sl
                0 N1119 ---> C2171/b
                                                             FC3+R
                                                                      909 -604
                                                                                  71
41 1 cs nnd2n02c sl
                         cs_nnd2n02c_sl 64 N1696 ----> C1937/y
FC3+R
         909 -604
                        41 1 cs_invvn01c_sl
                                                  cs invvn01c sl
                                                                  0 N1696 ---->
C1937/a
                              R C3+R
                                        868 -604
                                                    80 27 1 cs invvn01c sl
cs_invvn01c_sl 41 dcd_blk_dsucc ---> dcd_blk_dsucc
                                                                     R C3+R
                                                                               868
```

```
108 1172 7
                   2 dcd succ last
                                                     R C3+R
                                                             1474 -545
                                                                                929
                      0 dcd_succ_last_t1 RAT
PO
                                                           108 1172 7 cs_invvn01c_sl
                                     RC3+R
                                              1474 -545
0 ----> C2744/v
                                                                     F C3+R 1415
cs invvn01c_sl
               0 dcd_succ_last_t1 ----> C2744/a
                                                   59 N675 ---->{a} C2738/y
-545 83 416 4 cs_invvn01c_sl
                                    cs_invvn01c_sl
                                                    cs nnd2n02c sl
                                                                     0 N675 ---->
                      83 416 4 cs_nnd2n02c_sl
FC3+R
         1415 -545
                              R C3+R
                                       1365 -545
                                                    118 1360 5 cs nnd2n02c_sl
C2738/b
                                                              R C3+R 1365 -545
               50 N1098 ---->{b} C2734/y
cs nnd2n02c_sl
1360 5 cs_nnd2n02c_sl
                                            0 N1098 ----> C2734/a
                           cs nnd2n02c sl
                          458 1 cs_nnd2n02c_sl
                                                    cs_nnd2n02c_sl 61 N1097 ---->{c}
         1304 -545
FC3+R
                      83
                                                    83 458 1 cs_nnd2n02c_sl
                              FC3+R
                                       1304 -545
C2728/v
                                                             R C3+R
                                                                      1255 -545
                                                                                  108
                0 N1097 ---->
                              C2728/b
cs nnd2n02c sl
                          cs_nnd2n02c_sl 49 N1692 ----> C2725/v
164 1 cs_nnd2n02c_sl
                                                    cs invvn01c_sl
                                                                    0 N1692 ---->
                          164 1 cs_invvn01c_sl
R C3+R
         1255 -545
                     108
                                                    83 309 2 cs_invvn01c_sl
                              FC3+R
                                       1196 -545
C2725/a
                                                                                   83
cs invvn01c_sl 59 N1479 ---->{d} C2721/y
                                                             FC3+R
                                                                     1196 -545
                                         0 N1479 ---> C2721/a
                          cs_nnd2n02c_sl
309 2 cs_nnd2n02c_sl
                                                     cs nnd2n02c_sl 59 N1858 ---->{e}
RC3+R
         1138 -545
                     170 116 1 cs_nnd2n02c_sl
                                                  170 116 1 cs_ao22n03c_sl
C2550/y
                              R C3+R
                                       1138 -545
                                                             FC3+R
                                                                     1044 -545
                                                                                   83
cs_ao22n03c_sl
                0 N1858 ---->
                              C2550/a2
                                         94 N1437 ---->{f} C2427/v
69 1 cs_ao22n03c_sl
                         cs_ao22n03c_sl
                                                    cs_nnd2n02c_sl
                                                                     0 N1437 ---->
         1044 -545
                      83
                          69 1 cs_nnd2n02c_sl
FC3+R
                                                         38 1 cs_nnd2n02c_sl
                              R C3+R 995 -545
                                                    108
C2427/b
                                                             R C3+R
                                                                                  108
                                                                       995 -545
cs_nnd2n02c_sl 49 N1778 ---> C2334/y
                        cs_invvn01c_sl
                                        0 N1778 ----> C2334/a
                                                                                    F
38 1 cs invvn01c sl
                    83
                       103 4 cs_invvn01c_sl
                                                  cs_invvn01c_sl 59 N1119 ---->{g}
        936 -545
C3+R
                                                    83 103 4 cs_nnd2n02c_sl .
                              FC3+R
                                        936 -545
C2171/v
                                                             R C3+R
                                                                      887 -545
                                                                                  108
               0 N1119 ----> C2171/b
cs nnd2n02c sl
                         cs_nnd2n02c_sl 49 N1696 ----> C1937/y
41 1 cs_nnd2n02c_sl
                                                   cs_invvn01c_sl
                                                                   0 N1696 --->
R C3+R
          887 -545
                     108 41 1 cs_invvn01c_sl
                                                    80 27 1 cs_invvn01c_sl
                              FC3+R
                                        829 -545
C1937/a
cs_invvn01c_sl 58 dcd_blk_dsucc ----> dcd_blk_dsucc
                                                                     FC3+R
                                                                               829
                                     0 dcd blk dsucc
      80 27 1 PI
```

> report\_area [load\_update]: Found 723 pin load values not up-to-date, forcing queries [load\_update]: Warning - Detected load inconsistencies, forcing global invalidation [load\_update]: Number of pin load calculations: 4599 since last stats [load\_update]: Number of pin weight calculations: 0 since last stats Design: /IDCDSUC - Area: 5301.955566, Area(Weight): 1255.610474 > cputime Used 3.86 cpu seconds or 00:00:04 wall time, used 0 bytes or 0 byte. Checking DRC for IDesign IDCDSUC INet clkl\_mode7:clkl\_mode7 has cap violation 1.046, load 147.5, 1 slack 1.134e+38 INet a clk:a\_clk has cap violation 1.046, load 147.5, limit limit 141, multiplier 1 slack 1.134e+38 INet b\_clk:b\_clk has cap violation 1.093, load 154.1, limit 141, 141, multiplier 1 slack 349 INet test\_c1:test\_c1 has cap violation 1.078, load 152.1, limit 141, multiplier 1 slack 349 INet clkg:clkg has cap violation 1.202, load 169.5, limit 141, multiplier slack 1.134e+38 INet ireg\_valid:ireg\_valid has cap violation 1.207, load 170.3, limit 141, multiplier 1 slack -498.7 INet clkg2:clkg2 has cap violation 1.202, load 169.5, limit 141, multiplier 1.134e+38 INet scan\_enable:scan\_enable has cap violation 1.261, load 177.8, limit 141, multiplier 1 slack 1.134e+38 INet du\_iu\_store\_status(2):a has transition violation 1.099, multiplier transition 500, limit 455; FALL: transition 500, limit 455 INet eu\_iu\_srlz\_op\_encode(11):a has 1 RISE: transition 500, limit 455; FALL: transition 500, limit transition violation 1.099, multiplier 455 INet op cmp tr q:12 out n has cap violation 1.009, load 249.3, limit 247, multiplier 1 slack 617 INet rcvry\_reset\_q:l2\_out\_n has cap violation 1.123, load 277.5, limit 247, multiplier 1 slack 331 INet iu\_reset\_op\_c:y has cap violation 1.227, load 1227, limit 1000, multiplier

```
INet dcd_succ_last_t1:y has cap violation 1.215, load 1216, limit 1001, multiplier
                                                                                     1 slack -603.7
INet local_milli_q:l2_out_n has cap violation 1.138, load 281.1, limit 247, multiplier
                                                                                       1 slack -207.8
INet srlz_nomatch_q:l2_out_n has cap violation 1.021, load 252.2, limit 247, multiplier
                                                                                          1 slack
392 INet dcd_succ_dly_q:l2_out_n has cap violation 1.018, load 251.5, limit 247, multiplier
                                                                                                1 slack
355.4 INet iu_reset_all:y has cap violation 1.389, load 833.6, limit 600, multiplier
                                                                                      1 slack 322.9
INet local_milli_t1_q:l2_out_n has cap violation 1.018, load 251.5, limit 247, multiplier
-42.98 INet local_milli_t2_q:l2_out_n has cap violation 1.018, load 251.5, limit 247, multiplier
slack 230.4 INet exc_cond_q:l2_out_n has cap violation 1.142, load 282.1, limit 247, multiplier
slack 322.9 INet slow_mode_t2_q:l2_out_n has cap violation 1.009, load 249.3, limit 247, multiplier
1 slack 617 INet iu_rst_fst_q:l2_out_n has cap violation 1.02, load 251.9, limit 247, multiplier
slack -42.98 INet exc_info_q(0):l2_out_n has cap violation 1.028, load 254, limit 247, multiplier
                                                                                                     1
slack 610.4 INet exc_info_q(1):l2_out_n has cap violation 1.047, load 258.7, limit 247, multiplier
slack 476.5 Net exc_info_q(2):l2_out_n has cap violation 1.061, load 262.2, limit 247, multiplier
                                                                                                     1
slack 611.1 INet exc_info_q(3):l2_out_n has cap violation 1.063, load 262.6, limit 247, multiplier
                                                                                                     1
slack 603.1 INet dcd_cyl_cnt_q(0):l2_out_n has cap violation 1.134, load 280.2, limit 247, multiplier
1 slack -351.1 INet dcd_cyl_cnt_q(1):l2_out_n has cap violation 1.145, load 282.9, limit 247,
multiplier
            1 slack -346.9 INet slow_mode_blk_q:l2_out_n has cap violation 1.03, load 254.4, limit
247, multiplier
                 1 slack -221.5 | Net br_wrongs_q:l2_out_n has cap violation 1.069, load 264.1, limit
247, multiplier
                 1 slack 133 INet rstrt_reset_q:l2_out_n has cap violation 1.065, load 263.2, limit
                 1 slack 340.9 INet N22:y has cap violation 1.212, load 1213, limit 1001, multiplier
247, multiplier
1 slack 617 INet N26:y has cap violation 1.224, load 1226, limit 1001, multiplier
INet N36:y has cap violation 1.187, load 1188, limit 1001, multiplier
                                                                       1 slack 617 INet N134:y has
cap violation 1.177, load 1178, limit 1001, multiplier
                                                        1 slack 355.4 INet N158:y has cap violation
1.116, load 1117, limit 1001, multiplier
                                           1 slack 617 INet N1098:y has cap violation 1.403, load
1403, limit 1000, multiplier
                              1 slack -603.7 IDesign IDCDSUC has 38 violations
freeze_net_loads -set -limit [TIMER-6411]: Unasserted load on 369 inet(s). [TIMER-6412]: Asserted load
on 369 inet(s).
                          > cpr_eval
                                                   > tgfs_redund -effort 50
                                                                                         > cputime {
tgfs_rewire -tech -$rwr_effort }
                                              > tgfs_rewire -tech -high tgfs rewiring
                                                                                         Area: before
5441.99 after 5359.17 (1.52 %)
                                      Slack : before -603.6691 after -543.6871 (9.94 %)
                                                                                         Cell: before
763 after 762 (0.13 %)
                         Time: 20.260000 Used 20.89 cpu seconds or 00:00:21 wall time, used 65536
bytes or 64 kbytes. Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/tf.dll tf.dll
version 1.0 (Apr 14 1999 18:12:48) Binding:
/afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/sim.dll sim.dll version 1.0 (Apr 14 1999
18:12:45) Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/synzilla/1.0/dll-rs6000/tc.dll tc.dll version 1.0
                                    > tc::trestruct -sizeless -leaf_flex 1.02 -gain 5 -load 5
(Apr 14 1999 18:12:53)
tc::critflow -depth 3 -xforms __CiType_30_30a78098 Transform: trestruct 0.1 Options: Mode=Sizeless
GainBuckets=5
                         LoadBuckets=5
                                              MinInputs=2
                                                               MaxInputs=1024
                                                                                      PartialTree=false
SingleCell=false
                      SlackThreshold=0.000
                                                   LeafFlexibility=1.020 GA_Wire: Load=18.000
Delay=0.000 Slew=0.000 [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP,
and below. [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
IET-0112]: Deleting timing for design: sub_design, analysis mode: SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW CHIP, and below.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
> echo {Custom Synzilla Report} Custom Synzilla Report
                                                                     > ps -cell Design
/HISVHDL/IDCDSUC has:
                                      1 instances 0 upcells
                                                               122 IN ports 73 OUT ports
774 cells (0 AND; 0 XOR; 0 SEQ; 0 TRI; 774 LINKED; 0 UNLINKED; 0 DC)
                                                                                         995 nets (0
multiply-driven; 0 undriven)
                                      2607 pins (0 inversions) 2.62 pins per net
                                                                                         1539 literals
```

```
19 max fanout
                                                      Cell Information
22 levels
          10 max fanin
                                                                 PSEUDO_REG
                                                                                (ncount
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                  0)
                                cb clk 32 1 (ncount
                                                      6 : area
                                                             480)
83 : area
          0)
                                                      cs_ao12n03c_sl (ncount 6: area
cb mode block (ncount 1: area
                                70)
                     cs ao22n03c_sl (ncount 16: area
                                                      96)
cs_invvn01c_sl (ncount 216 : area
                                432)
                                                      cs nnd2n02c sl (ncount 209 : area
                                                      104)
                     cs nnd3n02c_sl (ncount 26: area
                                                      cs_nor2n02c_sl (ncount 14 : area
cs_nnd4n03c_sl (ncount
                     9 : area
                                45)
                     cs_nor3n03c_sl (ncount
                                            2: area
                                                      cs_oa22n03c_sl (ncount 1: area
                      3: area
                                15)
cs_oa21n03c_sl (ncount
                     cs_xbn2n01b_sl (ncount 1: area
                                                      Total Area = 1965 (Comb = 1415:
cs_xbo2n01b_sl (ncount 1 : area
                                 8)
                           > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550)
            for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Report
Sun Apr 18 21:53:42 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                       EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
                      Max. Slack: 1.13427E+38 Sort Field: Slack
-1.13427E+38
                                   Abbreviation Comparison/Description ------
Endpoints: 2 Cause of Slack
                                                         Slack due to a point downstream on
----- Slack Continuation
                                               SlkCont
                                      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                            RAT
                            (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                            ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                 ClkGSet
Gating Setup
                                                          ( DATA ARRIVAL TIME - CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                               ClkGHld
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                 Setup
(DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold
                                                                                 Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
FndOfC
                                 ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
ClockPulseWidth
                      CIkPW
                                                 ( CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
                                        ClkSep
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                  ALTest
                                                                             (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
          Slack discontinuity due to failed test
                                           Num/
ATLimit
                                        Delay/ Failed Test/ Test PinName
LimitedAT/
                                                P Func T.Adj NetName
          AT Slack Slew CL FO Cell
E Phase
                                                     FC3+R
                                                               1392 -513
                                                                            71 1160 7
                    1 dcd succ last
                                                                                879
PO
                      0 dcd_succ_last_t1 RAT
                                               1392 -513
                                                            71 1160 7 cs_invvn01c_sl
                                     FC3+R
0 ----> C2744/v
                                                                              1345
                0 dcd_succ_last_t1 ----> C2744/a
                                                                     R C3+R
cs invvn01c sl
-513 118 412 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y
          1345 -513 118 412 4 cs_nnd2n02c_sl
                                                     R C3+R
                                                     66 1326 4 cs_nnd2n02c_sl
                              FC3+R
                                        1282 -513
C2738/b
cs nnd2n02c_sl 63 N1098 ---> C2734rwr/y
                                                              FC3+R
                                                                        1282 -513
                                                                                     66
                                          0 N1098 ----> C2734rwr/a
                           cs invvn01c_sl
1326 4 cs_invvn01c_sl
                       99 446 1 cs_invvn01c_sl
                                                                   41 N1097 ---->
                                                    cs invvn01c sl
          1241 -513
R C3+R
                                                      99 446 1 cs_invvn01c_sl
                                         1241 -513
                                R C3+R
C2728rwr/v
                                                                                    83
                                                             FC3+R
                                                                      1187 -513
cs invvn01c_sl
                0 N1097 ----> C2728rwr/a
                          cs_invvn01c_sl 54 N1692 ---->{b} C2725rwr/y
178 2 cs invvn01c_sl
                                                                      0 N1692 ---->
                                                     cs_nnd2n02c_si
                       83 178 2 cs_nnd2n02c_sl
          1187 -513
F C3+R
                                         1127 -513 188 314 2 cs_nnd2n02c_sl
                                R C3+R
C2725rwr/a
                                                               R C3+R
                                                                         1127 -513
cs nnd2n02c_sl 60 N1479 ---->{c} C2721rwr/y
                                                0 N1479 ----> C2721rwr/b
188 314 2 cs_nnd3n02c_sl
                                cs_nnd3n02c_sl
          1028 -513 77 174 2 cs_nnd3n02c_sl
                                                     cs nnd3n02c sl 98 N1497 ---->{d}
FC3+R
                              F C3+R 1028 -513
                                                     77 174 2 cs_nor2n02c_sl
C2709/y
```

```
R C3+R
                                                        977 -513
                                                                 155
82 1 cs_nor2n02c sl
                    cs_nor2n02c_sl 51 N1986 ---->{e} C2677/y
R C3+R
        977 -513
                 155 82 1 cs_nnd4n03c_sl
                                         C2677/a
                        FC3+R
                                912 -513
                                         71 45 1 cs_nnd4n03c sl
cs_nnd4n03c_si 65 N1849 ----> C2591/y
                                                 FC3+R
                                                         912 -513
                                                                  71
45 1 cs_invvn01c_sl
                  cs_invvn01c_sl
                                0 N1849 ---> C2591/a
                                                                   R
      865 -513 113 23 1 cs_invvn01c_sl cs_invvn01c_sl 47 N1976 ---->{f}
C3+R
                         R C3+R
C2579rwr 0/v
                                865 -513 113 23 1 cs_nnd2n02c_sl
cs nnd2n02c sl 0 N1976 ----> C2579rwr 0/a
                                                 F C3+R
                                                        799 -513
117 118 6 cs nnd2n02c sl
                     cs_nnd2n02c_sl 66 ireg_valid ----> ireg_valid
       799 -513 117 118 6 PI
                                           0 ireg_valid
----2 dcd_succ_last
                                          R C3+R 1386 -457 108 1160 7
PO
                 0 dcd_succ_last_t1 RAT
                                                                929
0 ----> C2744/y
                                     1386 -457 108 1160 7 cs_invvn01c_sl
                             R C3+R
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                       F C3+R
                                                             1327
    1327 -457 83 412 4 cs_nnd2n02c_sl
FC3+R
                                          cs nnd2n02c sl 0 N675 ---->
C2738/b
                        R C3+R
                                1279 -457
                                          99 1326 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 48 N1098 ----> C2734rwr/v
                                                 R C3+R
                                                         1279 -457
                       99 1326 4 cs invvn01c sl
       1229 -457 66 446 1 cs_invvn01c_sl
F C3+R
                                         cs_invvn01c_sl 50 N1097 ---->
                                1229 -457 66 446 1 cs_invvn01c_sl
C2728rwr/y
                        FC3+R
cs invvn01c sl
            0 N1097 ----> C2728rwr/a
                                                R C3+R
                                                        1186 -457
                                                                  118
R C3+R
                                                        0 N1692 ---->
C2725rwr/a
                         FC3+R
                                1113 -457
                                         135 314 2 cs nnd2n02c sl
cs_nnd2n02c_si 73 N1479 ---->{c} C2721rwr/y
                                                  FC3+R
                                                          1113 -457
R C3+R
       1030 -457 134 174 2 cs nnd3n02c sl
                                          cs nnd3n02c sl 83 N1497
---->{d} C2709/y
                             R C3+R 1030 -457 134 174 2 cs_nor2n02c sl
cs_nor2n02c sl 0 N1497 ----> C2709/a
                                                FC3+R
                                                        955 -457 107
FC3+R
        955 -457
                107 82 1 cs_nnd4n03c_sl
                                         cs_nnd4n03c_sl
                                                       0 N1986 ---->
C2677/d
                                888 -457 172 62 2 cs_nnd4n03c_sl
                        RC3+R
cs_nnd4n03c_sl 68 N1719 ---->{f} C2599rwr/y
                                                 RC3+R
                                                          888 -457
172 62 2 cs_nor3n03c_sl
                       cs_nor3n03c_sl
                                     0 N1719 ----> C2599rwr/a
FC3+R
        811 -457
                 66
                     42 1 cs_nor3n03c_sl
                                         cs_nor3n03c_sl 77 N1942 ---->
C2349rwr_0_0/y
                          FC3+R
                                 811 -457 66 42 1 cs_invvn01c_sl
cs_invvn01c_sl
            0 N1942 ---> C2349rwr_0_0/a
                                                  R C3+R
                                                          768 -457
                        cs invvn01c sl 44 N288 ---->{a} C2339/v
118 24 1 cs_invvn01c_sl
R C3+R
        768 -457 118 24 1 cs nnd2n02c sl
                                         cs_nnd2n02c sl
                                                       0 N288 ---->
C2339/a
                        FC3+R
                                706 -457
                                         83 18 1 cs nnd2n02c sl
cs_nnd2n02c_sl 61 NET690 ---->{h} C2187/y
                                                  FC3+R
                                                          706 -457
83 18 1 cs nnd2n02c sl
                       32 2 cs_nnd2n02c_sl
RC3+R
        656 -457 108
                                          cs_nnd2n02c_sl 51 N29 ---->
C2020/y
                        R C3+R
                                656 -457
                                         108 32 2 cs_invvn01c_sl
            0 N29 ---> C2020/a
cs_invvn01c_sl
                                              FC3+R
                                                      557 -457 424
19 1 cs_invvn01c_sl cs_invvn01c_sl 99 du_iu_hold_aa_req ----> du_iu_hold_aa_req
FC3+R
        557 -457 424 19 1 PI
                                          0 du_iu_hold_aa_req
```

<sup>&</sup>gt; report\_area [load\_update]: Found 620 pin load values not up-to-date, forcing queries [load\_update]: Warning - Detected load inconsistencies, forcing global invalidation [load\_update]: Number of pin load calculations: 8096 since last stats [load\_update]: Number of pin weight calculations: 0 since last stats Design: /IDCDSUC - Area: 5226.390137, Area(Weight): 1270.181396

```
> cputime Used 38.94 cpu seconds or 00:00:39 wall time, used 299008 bytes or 292 kbytes.
> report_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap violation 1.032, load 145.5,
                       1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit
limit 141, multiplier
                 1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099,
141. multiplier
            1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet
multiplier
                                                                     1 RISE: transition 500, limit
eu iu_srlz_op_encode(11):a has transition violation 1.099, multiplier
455; FALL: transition 500, limit 455 INet iu_reset_op_c:y has cap violation 1.219, load 1219, limit
                  1 slack 133 INet dcd_succ_last_t1:y has cap violation 1.115, load 1116, limit
1000, multiplier
                  1 slack -513.2 INet iu_reset_all:y has cap violation 1.328, load 796.6, limit 600,
1001, multiplier
            1 slack 322.9 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier
multiplier
slack 617 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier
INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier
                                                                      1 slack 617 INet N134:y has
cap violation 1.169, load 1170, limit 1001, multiplier
                                                       1 slack 355.4 INet N158:y has cap violation
1.108, load 1109, limit 1001, multiplier
                                          1 slack 617 INet N1098:y has cap violation 1.302, load
                             1 slack -513.2 IDesign IDCDSUC has 13 violations
1303, limit 1001, multiplier
                                                                             > echo -583.569129373
                    > echo {In restructure loop} In restructure loop
cpr_eval
                            > echo -513.216552734 -513.216552734
                                                                                  > tgfs_redund
-583.569129373
                                                                          Area: before 5133.28 after
                               > tafs rewire -tech -high tafs rewiring
ch -$rwr_effort }
                        Slack : before -513.2166 after -506.3137 (1.35 %) Cell : before 775 after 773
5092.88 (0.79 %)
            Time: 13.960000 Used 14.51 cpu seconds or 00:00:14 wall time, used 0 bytes or 0 byte.
(0.26\%)
                                                              > tc::critflow -depth 3 -xforms
> tc::trestruct -sizeless -leaf_flex 1.02 -gain 5 -load 5
  CiType_30_31c4d268 Transform: trestruct 0.1 Options: Mode=Sizeless
                                                                            GainBuckets=5
                                     MaxInputs=1024
                                                           PartialTree=false
LoadBuckets=5
                     MinInputs=2
                                                  LeafFlexibility=1.020 [ET-0112]:Deleting timing for
                     SlackThreshold=0.000
SingleCell=false
design: sub_design, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
sub_design, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design,
analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design: sub_design, analysis
                                             > echo {Custom Synzilla Report} Custom Synzilla Report
mode:SLOW CHIP, and below.
                                                                           122 IN ports 73 OUT ports
> ps -cell Design /HISVHDL/IDCDSUC has:
                                                  1 instances 0 upcells
773 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 772 LINKED; 0 UNLINKED; 0 DC)
                                                                          0 buses
                                                                                       994 nets (0
                                     2604 pins (0 inversions) 2.62 pins per net
                                                                                       1537 literals
multiply-driven; 0 undriven)
                                                              Cell Information
                                     19 max fanout
21 levels
            10 max fanin
                                                                           PSEUDO_REG
                                                                                             (ncount
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                          0)
                                     cb clk 32 1 (ncount
                                                              6: area
                                                                        480)
83 : area
                                                              cs_ao12n03c_sl (ncount 6: area
cb mode_block (ncount
                         1 : area
                                     70)
                         cs_ao22n03c_sl (ncount 16 : area
                                                              cs nnd2n02c sl (ncount 211 : area
cs_invvn01c_sl (ncount 213 : area
                                     426)
                         cs_nnd3n02c_sl (ncount 27 : area
                                                              cs_nor2n02c_sl (ncount 13 : area
cs_nnd4n03c_sl (ncount
                          8: area
                                     40)
                         cs_nor3n03c_sl (ncount
                                                   2: area
39)
                                                              cs_oa22n03c_sl (ncount
                                      15)
                          3: area
cs_oa21n03c_sl (ncount
                         cs xbn2n01b_sl (ncount
                                                   1 : area
                                                               8)
6)
                                                              Total Area = 1961 (Comb = 1411:
cs xbo2n01b sl (ncount
                          1: area
                                > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550
               for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:54:11 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                                   EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38
                          Max. Slack: 1.13427E+38 Sort Field: Slack
                                                                                      Max.
```

```
Endpoints: 2 Cause of Slack
                           Abbreviation Comparison/Description ------
------ Slack Continuation
                                     SlkCont
                                              Slack due to a point downstream on
path Required Arrival Time
                      RAT
                              (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT
                      ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
                      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
              ClkGSet
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                     ClkGHld
                                              ( DATA ARRIVAL TIME - CLOCK
  ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
Setup
        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
       ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
Hold
EndOfC
         ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
ClockPulseWidth
               CIkPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation
                               ClkSep
                                       ( CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                     ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
        Slack discontinuity due to failed test
                                  Num/
LimitedAT/
                                Delay/ Failed Test/ Test PinName
E Phase
        AT Slack Slew CL FO Cell
                                      P Func T.Adj NetName
                1 dcd_succ_last
                                           FC3+R 1385 -506 71 1116 7
PO
                  0 dcd_succ_last_t1 RAT
                                                                879
0 ----> C2744/y
                                     1385 -506 71 1116 7 cs_invvn01c_sl
                             F C3+R
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                       R C3+R 1338
-506 118 384 4 cs_invvn01c_sl cs_invvn01c_sl 47 N675 ---->{a} C2738/y.
R C3+R 1338 -506 118 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b
                        FC3+R
                               1275 -506 66 1303 4 cs_nnd2n02c sl
cs_nnd2n02c_sl 63 N1098 ----> C2734rwr/y
                                                         1275 -506
                                                 FC3+R
                                                                   .66
1234 -506 99 439 1 cs_invvn01c_sl cs_invvn01c_sl 41 N1097 ---->
C2728rwr/v
                         R C3+R 1234 -506 99 439 1 cs_invvn01c sl
F C3+R 1180 -506
                                                                   83
FC3+R
       0 N1692 ---->
C2725rwr/a
                                1120 -506 188 306 2 cs_nnd2n02c_sl
                         R C3+R
cs_nnd2n02c_sl 60 N1479 ---->{c} C2721rwr/y
                                                  R C3+R 1120 -506
1012 -506 110 162 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 108 N1497 ---->{d}
FC3+R
C2709rwr/y
                        FC3+R
                               1012 -506 110 162 2 cs_nor3n03c_sl
R C3+R
                                                         946 -506 129
54 1 cs_nor3n03c_sl
                    cs_nor3n03c_sl 66 N1986 ---->{e} C2677rwr/y
        946 -506 129 54 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1986 ---->
R C3+R
             882 -506 59 49 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 64 N1094
     FC3+R
---->{f} C2909/v
                             FC3+R
                                    882 -506 59 49 2 cs_nnd2n02c_sl
R C3+R
                                                        850 -506
R C3+R 850 -506
                 80 78 1 PI
                                        0 dcd_mcr41_blk
               2 dcd_succ_last
                                          R C3+R 1423 -494 108 1116 7
                 0 dcd_succ_last_t1 RAT
                                                               929
0 ----> C2744/v
                                     1423 -494 108 1116 7 cs_invvn01c_sl
                             R C3+R
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                       F C3+R
-494 83 384 4 cs_invvn01c_sl cs_invvn01c_sl 59 N675 ---->{a} C2738/y
       1365 -494 83 384 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
F C3+R
C2738/b
                               1317 -494
                        R C3+R
                                          99 1303 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 48 N1098 ----> C2734rwr/y
                                                 R C3+R
                                                         1317 -494
99 1303 4 cs_invvn01c_sl
```

```
50 N1097
                                                    cs invvn01c_sl
                      66 439 1 cs_invvn01c_sl
FC3+R
         1267 -494
                                                            66 439 1 cs_invvn01c_sl
                                               1267
                                                    -494
---> C2728rwr/v
                                     FC3+R
                                                             RC3+R
                                                                       1223 -494 118
cs invvn01c sl
               0 N1097 ----> C2728rwr/a
                                        44 N1692 ---->{b} C2725rwr/y
                         cs invvn01c_sl
171 2 cs invvn01c_sl
                      118 171 2 cs_nnd2n02c_sl
                                                      cs nnd2n02c sl
                                                                      0 N1692 ---->
R C3+R
         1223 -494
                                                     135 306 2 cs_nnd2n02c_sl
                               FC3+R
                                         1150 -494
C2725rwr/a
                                                               FC3+R
               73 N1479 ---->{c} C2721rwr/y
                                                                        1150 -494
cs nnd2n02c_sl
                                                0 N1479 ----> C2721rwr/b
                               cs_nnd3n02c_sl
135 306 2 cs_nnd3n02c_sl
                                                      cs nnd3n02c_sl
                                                                      95 N1497 ---->{d}
                          162 2 cs_nnd3n02c_sl
         1055 -494 247
R C3+R
                                                     247 162 2 cs_nor3n03c_sl
                                         1055 -494
                               RC3+R
C2709rwr/y
               0 N1497 ----> C2709rwr/a
                                                             FC3+R
                                                                       937 -494
                                                                                    90
cs nor3n03c sl
                        cs_nor3n03c_si 118 N1986 ---->{e} C2677rwr/y
54 1 cs nor3n03c sl
                                                                     0 N1986 ---->
                      90 54 1 cs nnd3n02c sl
                                                    cs_nnd3n02c_sl
FC3+R
         937 -494
                                         883 -494
                                                          49 2 cs nnd3n02c sl
                               RC3+R
                                                    123
C2677rwr/c
                                                               R C3+R
                                                                          883 -494
cs_nnd3n02c_sl 54 N1719 ---->{f} C2599rwr_0/y
                                               0 N1719 ----> C2599rwr 0/a
123 49 2 cs_nor2n02c_sl
                          cs nor2n02c sl
                                                    cs nor2n02c_sl 63 N1942 ---->{g}
          820 -494
                      83
                          35 1 cs_nor2n02c_sl
FC3+R
nd2n02c_sl
                cs_nnd2n02c_sl
                                0 N1942 ---->
                                               C2349rwr 0 0 0/a
                                                   cs nnd2n02c sl 52 N288 ---->{h}
        768 -494 118
                        22 1 cs_nnd2n02c_sl
C3+R
                                                   118 22 1 cs_nnd2n02c_sl
                              R C3+R
                                        768
                                             -494
C2339/y
                                                            FC3+R
                                                                      706 -494
                                                                                  83
cs nnd2n02c_sl
                0 N288 ----> C2339/a
                         cs_nnd2n02c_sl 61 NET690 ---->{i} C2187/y
17 1 cs nnd2n02c_sl
                          17 1 cs_nnd2n02c_sl
                                                    cs_nnd2n02c_sl
                                                                     0 NET690 ---->
FC3+R
          706 -494
                      83
                              RC3+R
                                                    108
                                                          32 2 cs_nnd2n02c_sl
                                         656 -494
C2187/a
cs_nnd2n02c_sl 51 N29 ----> C2020/v
                                                                     656 -494
                                                                                 108
                                                           R C3+R
                                                   C2020/a
                                                                                  · F
                        cs invvn01c_sl
                                        0 N29 ---->
32 2 cs_invvn01c_sl
                                                  cs_invvn01c_sl 99 du_iu_hold_aa_req
                        19 1 cs_invvn01c_sl
        557 -494
                   424
                                                  557 -494 424 19 1 PI
                                        FC3+R
----> du_iu_hold_aa_req .
0 du iu_hold_aa_req
```

> report area Design: /IDCDSUC - Area: 5092.879883, Area(Weight): > cputime Used 27.17 cpu seconds or 00:00:27 wall time, used 327680 bytes 1267.547363 > report\_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap or 320 kbytes. violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet du\_iu\_store\_status(2):a 1 RISE: transition 500, limit 455; FALL: transition 500, has transition violation 1.099, multiplier limit 455 INet eu\_iu\_srlz\_op\_encode(11):a has transition violation 1.099, multiplier transition 500, limit 455; FALL: transition 500, limit 455 INet iu\_reset\_op\_c:y has cap violation 1 slack 140.6 INet dcd\_succ\_last\_t1:y has cap violation 1.219, load 1219, limit 1000, multiplier 1 slack -506.3 INet iu\_reset\_all:y has cap violation 1.328, 1.115, load 1116, limit 1001, multiplier load 796.6, limit 600, multiplier 1 slack 339 INet N22:y has cap violation 1.204, load 1205, limit 1 slack 618 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier 1001, multiplier 1 slack 394.3 INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 357.2 INet N158:v INet N134:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 630.3 INet N1098:y has cap has cap violation 1.108, load 1109, limit 1001, multiplier violation 1.302, load 1303, limit 1001, multiplier 1 slack -506.3 IDesign IDCDSUC has 13 violations > echo {in restructure loop} in restructure loop > echo > cpr eval > echo -506.313720703 -506.313720703 -493.216553684 -493.216553684 freeze\_net\_loads -reset [TIMER-6411]: Unasserted load on 369 inet(s). > load\_update > gbfo\_assign\_gain -gain 5.0 [load\_update]: Number of pin load calculations: 6881 -invalidate since last stats [load\_update]: Number of pin weight calculations: 0 since last stats Assign Gain Area: before 5092.88 after 4486.86 (11.90 %) Slack : before -506.3137 after -812.2559 (-60.43 %) Cell: before 773 after 773 (0.00 %) Time: 2.590000 > check\_slack\_cont [cr]: (W): pin: c in: c (cell: C2457) has invalid rise/fall slack: 1.134e+38. [cr]: (W): pin: a (cell: C2630) has invalid rise/fall slack: 1.134e+38. [cr]: (W): pin: a (cell: C2630) has invalid rise/fall slack: 1.134e+38.

```
gbfo_fancorr -check -use_max_load -aggressive -max_buffe... [GB-103]: noninverting buffers are absent
Fanout Corr Area: before 4486.86 after 4502.64 (-0.35 %)
                                                           Slack: before -812.2559 after -812.2559
            Cell: before 773 after 787 (-1.81 %) Time: 4.870000
(0.00\%)
                                                                          > report_gain_violations
-min 1.0 -max 10.0 ------ Gain Violation Report for design IDCDSUC
----- Type
                                               Gain
                                                                       Cell Name
                                                > report drc Checking DRC for IDesign IDCDSUC
INet clkg:clkg has cap violation 1.032, load 145.5, limit 141, multiplier
                                                                   1 slack 1.134e+38 INet
clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier
                                                                  1 slack 1.134e+38 INet
du iu store status(2):a has transition violation 1.099, multiplier
                                                            1 RISE: transition 500, limit
FALL: transition 500, limit 455 INet eu_iu_srlz_op_encode(11):a has transition violation 1.099,
           1 RISE: transition 500, limit 455; FALL: transition 500, limit
                                                                        455 INet
dcd_succ_last_t1:y has cap violation 1.083, load 1084, limit 1001, multiplier
                                                                          1 slack -812.3 INet
srlz_nomatch_q:l2_out_n has cap violation 1.096, load 270.7, limit 247, multiplier
                                                                               1 slack 258.2
INet dcd_succ_dly_q:l2_out_n has cap violation 2.503, load 618.4, limit 247, multiplier
                                                                                    1 slack
68.9 INet dcd_succ_dly_q:a has transition violation 1.094, multiplier
                                                                  1 RISE: transition 497.9, limit
455; FALL: transition 400.4, limit 455 INet slow_mode_t2_q:l2_out_n has cap violation 1.018, load
251.4, limit 247, multiplier
                            1 slack 502.4 Net N22:y has cap violation 1.204, load 1205, limit
1001, multiplier
                 1 slack 502.4 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier
1 slack 258.2 INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier
                                                                                 1 slack 509.2
INet N1098:y has cap violation 1.225, load 1227, limit 1001, multiplier
                                                                     1 slack -812.3 INet
gbfonet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier
                                                                    1 slack -229 INet
gbfonet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier
                                                                     1 slack 68.9 INet
gbfonet_16:y has cap violation 1.108, load 1109, limit 1001, multiplier
                                                                     1 slack 467.6 IDesign
IDCDSUC has 16 violations
                                     > echo {Custom Synzilla Report} Custom Synzilla Report
> ps -cell Design /HISVHDL/IDCDSUC has:
                                               1 instances 0 upcells
                                                                       122 IN ports 73 OUT ports
787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC)
                                                                       0 buses 1008 nets (0
multiply-driven; 0 undriven)
                                   2632 pins (0 inversions) 2.61 pins per net
                                                                                  1551 literals
21 levels
           10 max fanin
                                   15 max fanout
                                                           Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                                       PSEUDO REG
                                                       0)
83: area
                                   cb clk 32 1
                                                 (ncount
                                                                    480)
                                                           6: area
cb_mode_block (ncount
                                                           cs_ao12n03c_sl (ncount 6: area
                        1 : area
                                   70)
                       cs_ao22n03c_sl (ncount
                                                16: area
cs_invvn01c_sl (ncount 227 : area
                                                           cs_nnd2n02c_sl (ncount 211 : area
                                   454)
                       cs_nnd3n02c_sl (ncount 27 : area
                                                           108)
cs_nnd4n03c_sl (ncount
                        8: area
                                   40)
                                                           cs_nor2n02c_sl (ncount 13: area ...
                        cs_nor3n03c_sl (ncount
                                                2: area
cs_oa21n03c_sl (ncount
                                   15)
                                                           cs_oa22n03c_sl (ncount
                        3: area
                                                                                    1: area
                        cs_xbn2n01b_sl (ncount
6)
                                                1: area
                                                           8)
cs xbo2n01b sl (ncount
                        1: area
                                                           Total Area = 1989 (Comb = 1439:
                             > write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint
Non-Comb = 550)
0019]:<End.....New Endpoint Report.
                                        Sun Apr 18 21:54:26 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                           EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                       Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack
                                           Abbreviation Comparison/Description -----
                          Slack Continuation
                                                   SlkCont
                                                              Slack due to a point downstream on
path Required Arrival Time
                               RAT
                                         (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT
                                ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                   ClkGSet
                               ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                    ClkGHld
                                                               ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                               CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                         Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                         Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
EndOfC
            ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
ClockPulseWidth
                        ClkPW
                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
```

```
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                    ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
       Slack discontinuity due to failed test
                                 Num/
                               Delay/ Failed Test/ Test PinName
LimitedAT/
                                     P Func T.Adj NetName
F Phase AT Slack Slew CL FO Cell
                                   _______
             1 eu_dsbl_aftr.reg_n.lat_0/BASE_REG/a F C3+R 2133 -812 0 05d cl_invvn05d 39 DELAY Setup eu_dsbl_aftr.reg_n.lat_0/BASE_REG/c1
27 1 cl_invvn
           050 CI_IIIVVII000 00 ___

60 221 13 CI_INVN 05d
                                       1200 c1 ---->
     160
eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/OUT
                                  F C3+R 2133 -812
                                                    0 27 1 AND
    0 DELAY ----> eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/IN1
                                                     R C3+R 2181
                         AND
                              -48 a ----> eu_dsbl_aftr.reg_n.lat_0/a
-812 132 16 1 AND
      2181 -812 132 16 1 PSEUDO_REG PSEUDO_REG 0 a ---->
R C3+R
                      R C3+R 2181 -812 132 16 1 cs_invvn01c_sl
C2874/v
F C3+R 2103 -812
F
C3+R 2103 -812 109 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl
                                                    0 N1013 ---->
                       R C3+R 2033 -812 156 17 1 cs_nnd2n02c_sl
C2856/b
cs_nnd2n02c_sl 70 N522 ---->{b} C2833/y
                                               R C3+R 2033 -812 156
F
                                 FC3+R 1945 -812 86 233 14
87 N1290 ----> C2800/y
cs_invvn01c_sl cs_invvn01c_sl 0 N1290 ----> C2800/a
                                                              RC3+R
                                cs_invvn01c_sl 63 N1648 ---->{c} C2779/y
1882 -812 156 57 1 cs_invvn01c_sl
      1882 -812 156 57 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1648 ---->
R C3+R
                       F C3+R 1795 -812 109 22 1 cs_nnd2n02c_sl
C2779/a
                                                 F C3+R 1795 -812
cs nnd2n02c sl 87 NET803 ---->{d} C2759/y
1724 -812 132 1084 7 cs_nnd2n02c_sl cs_nnd2n02c_sl 71
                                       R C3+R 1724 -812 132 1084 7
dcd_succ_last_t1 ----> C2744/v
cs_invvn01c_sl cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
       1646 -812 109 277 4 cs_invvn01c_sl cs_invvn01c_sl 78 N675 ---->{e}
FC3+R
                      F C3+R 1646 -812 109 277 4 cs_nnd2n02c_sl
C2738/v
cs nnd2n02c sl 0 N675 ----> C2738/b
                                              R C3+R
                                                      1578 -812 132
                 cs_nnd2n02c_sl 67 N1098 ----> C2734rwr/y
1227 4 cs_nnd2n02c_sl
       1578 -812 132 1227 4 cs_invvn01c_sl cs_invvn01c_sl
                                                     0 N1098 ---->
R C3+R
                               1506 -812 86 256 1 cs_invvn01c_sl
                        FC3+R
C2734rwr/a
cs invvn01c_sl 72 N1097 ----> C2728rwr/y
                                                F C3+R 1506 -812
                                                                 86
1443 -812 156 78 2 cs_invvn01c_sl cs_invvn01c_sl 63 N1692 ---->{f}
                               1443 -812 156 78 2 cs_nnd2n02c_sl
C2725rwr/v
                        R C3+R
1350 -812 132
                                                FC3+R
F C3+R
                               1253 -812 295 90 2 cs_nnd3n02c_sl
                        R C3+R
C2721rwr/b
cs_nnd3n02c_sl 97 N1497 ---->{h} C2709rwr/y
                                                 R C3+R
                                                       1253 -812
F C3+R 1102 -812 132 29 1 cs_nor3n03c_sl cs_nor3n03c_sl 151 N1986 ---->{i}
                        F C3+R 1102 -812 132 29 1 cs_nnd3n02c_sl
C2677rwr/y
                                                R C3+R
            0 N1986 ----> C2677rwr/c
                                                       1019 -812
cs nnd3n02c sl
208 33 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 83 N1719 ---->{j} C2599rwr_0/y
      1019 -812 208 33 2 cs_nor2n02c_sl cs_nor2n02c_sl 0 N1719 ---->
R C3+R
                        F C3+R 907 -812 109 17 1 cs_nor2n02c_sl
C2599rwr 0/a
cs_nor2n02c_sl 112 N1942 ---->{k} C2349rwr_0_0_0/y
                                                 F C3+R 907 -812
         R C3+R 832 -812 156 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 75
```

TRAILING EDGE ) ClockSeparation

CIKSep (CLOCK1 ARRIVAL TIME + CLOCK

```
FC3+R
                                                   744 -812 109
C2187/a
                      R C3+R
                              673 -812 132 32 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 71 N29 ---> C2020/v
                                            R C3+R 673 -812 132
F
      557 -812 424 17 1 cs_invvn01c_sl cs_invvn01c_sl 116 du_iu_hold_aa_req
----> du_iu_hold_aa_req
                        F C3+R 557 -812 424 17 1 PI
0 du_iu_hold aa req
----- 2 eu_frc_milli.reg_n.lat_0/BASE_REG/a
                                         F C3+R 2133 -812

      27 1 cl_invvn
      05d cl_invvn05d
      39 DELAY Setup
      eu_frc_milli.reg

      F C3-
      160
      60 238 14 cl_invvn
      05d
      1200 c1 ---->

      eu_frc_milli.reg_n.lat_0/DELAY_ELEMENT/OUT
      F C3+R
      2133 -812

              05d cl_invvn05d 39 DELAY Setup eu_frc_milli.reg_n.lat_0/BASE_REG/c1
                                                  0 27 1 AND
     0 DELAY ----> eu_frc_milli.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 2181 -812
                    AND -48 a ----> eu_frc_milli.reg_n.lat_0/a
132 16 1 AND
                                                           R C3+R
2181 -812 132 16 1 PSEUDO_REG PSEUDO_REG 0 a ----> C2875/y
R C3+R 2181 -812 132 16 1 cs_invvn01c_sl cs_invvn01c_sl 0 N101 ---->
C2875/a
                      F C3+R 2103 -812 109 16 1 cs_invvn01c sl
cs invvn01c_sl 78 N994 ---->{a} C2857/y...
                                            F C3+R 2103 -812 109
C3+R 2033 -812 156 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 70 N505---->{b}
                     R C3+R 2033 -812 156 17 1 cs_nnd2n02c_sl
C2834/v
FC3+R 1945 -812 86
F C3+R 1945 -812 86 233 14 cs_invvn01c_sl cs_invvn01c_sl 0 N1290 ----> C2800/a R C3+R 1882 -812 156 57 1 cs_invvn01c_sl
cs_invvn01c_sl 63 N1648 ---->{c} C2779/v
                                .
                                             R C3+R 1882 -812 156
FC3+R 1795 -812 109 22 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 87 NET803 ---->{d}
C2759/v
                      F C3+R 1795 -812 109 22 1 cs nnd2n02c sl
R C3+R 1724 -812
nnd2n02c_sl 71 dcd_succ_last_t1 ----> C2744/v
                                                 R C3+R 1724 -812
F C3+R 1646 -812 109 277 4 cs_invvn01c_sl cs_invvn01c_sl 78 N675 ---->{e}
                     F C3+R 1646 -812 109 277 4 cs_nnd2n02c_sl
R C3+R
                                                   1578 -812 132
1578 -812 132 1227 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ---->/a F C3+R 1506 -812 86 256 1 cs_invvn01c_sl
R C3+R
C2734rwr/a
cs_invvn01c_sl 72 N1097 ----> C2728rwr/y
                                             F C3+R 1506 -812
R C3+R 1443 -812 156 78 2 cs_invvn01c_sl cs_invvn01c_sl 63 N1692 ---->{f}
C2725rwr/y
                       R C3+R 1443 -812 156 78 2 cs_nnd2n02c_sl
F C3+R
                                                    1350 -812
162 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 93 N1479 ---->{g} C2721rwr/y
F C3+R 1350 -812 132 162 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
C2721rwr/b
                       R C3+R
                             1253 -812 295 90 2 cs_nnd3n02c_sl
cs_nnd3n02c_sl 97 N1497 ---->{h} C2709rwr/y
                                              R C3+R
                                                     1253 -812
295 90 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1497 ----> C2709rwr/a
F C3+R 1102 -812 132 29 1 cs_nor3n03c_sl cs_nor3n03c_sl 151 N1986 ---->{i}
C2677rwr/v
                      FC3+R 1102 -812 132 29 1 cs_nnd3n02c sl
R C3+R
                                                    1019 -812
208 33 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 83 N1719 ---->{i} C2599rwr_0/y
```

R C3+R

832 -812 156 17 1 cs\_nnd2n02c sl

N288 ---->{I} C2339/y

```
208
                               33 2 cs nor2n02c si
                                                          cs nor2n02c_sl
                                                                            0 N1719 ---->
          1019 -812
R C3+R
                                                           109 17 1 cs_nor2n02c sl
                                    FC3+R
                                               907 -812
C2599rwr_0/a
                                                                         FC3+R
                                                                                    907 -812
cs_nor2n02c_sl 112 N1942 ---->{k} C2349rwr_0_0_0/y
                                  cs_nnd2n02c_sl
                                                   0 N1942 ----> C2349rwr_0_0_0/a
     17 1 cs nnd2n02c_sl
                              17 1 cs_nnd2n02c_sl
                                                          cs_nnd2n02c_sl
                                                                           75 N288 ---->{I}
RC3+R
           832 -812
                       156
                                                               17 1 cs_nnd2n02c_sl
C2339/v
                                 R C3+R
                                            832 -812
                                                         156
                                                                  FC3+R
                                                                             744 -812
                                                                                          109
cs_nnd2n02c_sl
                  0 N288 ---->
                                C2339/a
                            cs_nnd2n02c_si 87 NET690 ---->{m} C2187/y
17 1 cs_nnd2n02c_sl
           744 -812
                        109
                              17 1 cs_nnd2n02c_sl
                                                          cs nnd2n02c sl
                                                                            0 NET690 ---->
FC3+R
                                 R C3+R
                                             673 -812
                                                         132
                                                                32 2 cs nnd2n02c sl
C2187/a
                                                                            673 -812
                                                                 RC3+R
                                                                                         132
                 71 N29 ---->
                               C2020/v
cs_nnd2n02c_sl
                                          424
                                                17 1 cs_invvn01c_sl
                                                                            cs_invvn01c_sl 116
                  FC3+R
                             557 -812
du_iu_hold_aa_req ----> du_iu_hold_aa_req
                                                              FC3+R
                                                                         557 -812
                                                                                      424
                         0 du iu hold aa_req
1 PI
                             > report area Design: /IDCDSUC - Area: 4502.641602, Area(Weight):
                        > cputime Used 14.86 cpu seconds or 00:00:15 wall time, used 0 bytes or 0
1284.131592
               > gbfo_tune_gain -target_frac 1.0 -gain_incr 0.03 -gain_de... Tune Gain
                                                                                  Area: before
bvte.
                                    Slack : before -812.2559 after -680.5689 (16.21 %) Cell : before
4502.64 after 4352.61 (3.33 %)
                                                   > qbfo_tune_gain -target_frac 0.95 -gain_incr
787 after 787 (0.00 %)
                       Time: 46.970000
0.05 -gain_d... C2734rwr new rep load 319.6 greater than max 300.2: set to max: FREEZE SIZEUP
C2738 new rep load 101.9 greater than max 96.3: set to max: FREEZE SIZEUP C2721rwr new rep load
62.36 greater than max 61.93: set to max: FREEZE SIZEUP C2709rwr new rep load 43.54 greater than
max 42.11: set to max: FREEZE SIZEUP C2550 new rep load 42.06 greater than max 39.67: set to
max: FREEZE SIZEUP C2906 new rep load 69.02 greater than max 64.9: set to max: FREEZE SIZEUP
                                                          Slack : before -680.5689 after -446.0240
Tune Gain Area: before 4352.61 after 4474.51 (-2.80 %)
            Cell: before 787 after 787 (0.00 %)
                                                Time: 20.930000
                                                                           > cpr_eval
> resize -examine 5 -trace 10 -local -mincut -inc -sequent... resize
                                                                        Area: before 4474.51 after
                        Slack : before -446.0240 after -446.0240 (0.00 %) Cell : before 787 after 787
4474.51 (0.00 %)
                                         > load update -invalidate
                                                                             > swap pins
            Time: 1.780000
(0.00\%)
-examine 5 -est -ana 10000 -exe 1000 -per 10 -... [load_update]: Number of pin load calculations: 57353
since last stats [load_update]: Number of pin weight calculations: 0 since last stats [SWAP-8603]:
Swapping pins (mode=BACK) for: IDESIGN:/IDCDSUC Note: Swapped 16 pins on 8 cells in 1 Passes.
            Area: before 4474.51 after 4475.36 (-0.02 %)
                                                           Slack: before -446.0240 after -441.6489
swap
                                                Time: 2.560000
                                                                           > reset timing_area
            Cell: before 787 after 787 (0.00%)
(0.98\%)
                                    > cputime { tgfs_rewire -tech -$rwr_effort }
> tafs redund -effort 50
                                                Area: before 4475.36 after 4531.42 (-1.25 %)
tafs rewire -tech -medium tafs rewiring
Slack: before -441.6489 after -441.6489 (0.00 %) Cell: before 787 after 787 (0.00 %)
14.330000 Used 17.42 cpu seconds or 00:00:18 wall time, used 0 bytes or 0 byte.
1 slack -419.7 Net clkg:clkg has cap violation 1.032, load
1.08, load 152.2, limit 141, multiplier
                           1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5,
145.5, limit 141, multiplier
                      1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099.
limit 141, multiplier
            1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet
eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier
                                                                  1 RISE: transition
                     500. limit 455 INet dcd succ last_t1:y has cap violation 1.078, load 1079,
455; FALL: transition
                       1 slack -441.6 INet frc_blk_1cyc_q:l2_out_n has cap violation 1.097, load
limit 1001, multiplier
                             1 slack -198.7 INet N22:y has cap violation 1.204, load 1205, limit
270.9, limit 247, multiplier
                  1 slack 614.7 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier
1001, multiplier
                         1 slack 616.3 INet N1098:y has cap violation 1.26, load 1261, limit 1001,
0. limit 1001, multiplier
            1 slack -441.6 INet gbfonet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier
1 slack 28.61 INet gbfonet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier
343.9 INet abfonet 16:y has cap violation 1.108, load 1109, limit 1001, multiplier
                                                                                 1 slack 477.9
IDesign IDCDSUC has 14 violations
                                             > write end point_report -points 3
[ET-0018]:>Begin...New EndPoint Report
                                              for file /tmp/end_point_report..147522.
```

```
[ET-0019]:<End.....New Endpoint Report.
                                 Sun Apr 18 21:56:11 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                    EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                          Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 3 Cause of Slack
                                 Abbreviation Comparison/Description -----
----- Slack Continuation
                                       SlkCont
                                                Slack due to a point downstream on
path Required Arrival Time
                      RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
              CIKGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold ClkGHld
                                               ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                             CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                    Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold
                                                                    Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
         ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
ClockPulseWidth
                   CIkPW
                           ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation
                                 ClkSep
                                        ( CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                        ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
ATLimit
        Slack discontinuity due to failed test
                                    Num/
LimitedAT/
                                  Delay/ Failed Test/ Test PinName
E Phase AT Slack Slew CL FO Cell
                                    P Func T.Adj NetName
_____
                                      F C3+R
----- 1 dcd succ last
                                                     1321 -442
                                                                81 1079 7
                 0 dcd_succ_last_t1 RAT
                                                                   879
0 ----> C2744/y
                                      1321 -442 81 1079 7 cs_invvn01c_sl
                               FC3+R
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                          R C3+R
-442 121 301 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
R C3+R 1266 -442 121 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b
                         FC3+R
                                 1198 -442
                                            79 1261 4 cs_nnd2n02c_sl
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y
                                                    FC3+R
                                                            1198 -442
        R C3+R 1151
     87 306 1 cs invvn01c sl
                           cs invvn01c sl 47 N1097 ----> C2728rwr/y
        1151 -442 87 306 1 cs invvn01c sl
R C3+R
                                            cs invvn01c sl 0 N1097 ---->
                                 1107 -442 70 165 2 cs_invvn01c_sl
                         FC3+R
C2728rwr/a
cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
                                                    F C3+R 1107 -442
                                                                       70
1060 -442 140 161 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 46 N1479 ---->{c}
R C3+R
C2721rwr/v
                          R C3+R
                                  1060 -442 140 161 2 cs nnd3n02c sl
FC3+R
                                                            980 -442
                                                                      100
65 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 81 N1858 ---->{d} C2550/y
FC3+R
        980 -442 100 65 1 cs_ao22n03c_sl cs_ao22n03c_sl 0 N1858 ---->
C2550/a2
                          R C3+R
                                  935 -442 86 48 1 cs_ao22n03c_sl
cs_ao22n03c_sl 44 N1437 ---> C2427rwr/y
                                                    R C3+R 935 -442
                                                                       86
                48 1 cs_invvn01c_sl
                 893 -442
C3+R
        893 -442 62 32 1.cs invvn01c sl
                                        cs invvn01c sl 0 N1717 ---->
FC3+R
                         R C3+R
                                  858 -442 80 87 3 cs_invvn01c_sl
C1982/a
cs_invvn01c_sl 35 op_cmp_raw ----> op_cmp_raw
                                                         RC3+R
                                                                  858 -442
80 87 3 PI
                         0 op_cmp_raw
                2 dcd_succ_last
                                             R C3+R 1353 -424
                                                               123 1079 7
                   0 dcd_succ_last_t1 RAT
                              R C3+R 1353 -424 123 1079 7 cs_invvn01c_sl
0 ----> C2744/v
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                          FC3+R
-424 85 301 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
```

```
cs nnd2n02c sl 0 N675 ---->
FC3+R
      1286 -424 85 301 4 cs_nnd2n02c_sl
                    R C3+R
                          1234 -424 120 1261 4 cs_nnd2n02c_sl
C2738/b
cs nnd2n02c_sl 52 N1098 ---> C2734rwr/y
                                           R C3+R
                                                 1234 -424
0 N1098 ----> C2734rwr/a
      1175 -424 59 306 1 cs_invvn01c_sl
                                    cs_invvn01c_sl 59 N1097 ---->
FC3+R
                           1175 -424 59 306 1 cs_invvn01c_sl
                    FC3+R
C2728rwr/v
1139 -424
                                                         101
                                          R C3+R
                    1139 -424 101 165 2 cs_nnd2n02c_sl
              R C3+R
                                                 1084 -424
                                                          98
cs nnd2n02c sl 0 N1692 ----> C2725rwr/a
                                          FC3+R
cs nnd3n02c_sl 67 N1497 ---->{d} C2709rwr/y
                                           R C3+R
                                                  1017 -424
cs_nor3n03c_sl 101 N1781
                                916 -424 97 80 2 cs_nnd4n03c_sl
                         FC3+R
---->{e} C2885/y
                                          R C3+R 850 -424 224
cs nnd4n03c sl 0 N1781 ----> C2885/c
850 -424 224 52 1 cs_oa21n03c_sl cs_oa21n03c_sl 0 N1999 ---->
R C3+R
                   F C3+R 749 -424 57 19 1 cs_oa21n03c_sl
C2889/b
cs_oa21n03c_sl 101 N2000 ----> C2890rwr/y
                                           F C3+R 749 -424
                                                          57
R
     716 -424 91 20 1 cs_invvn01c_sl cs_invvn01c_sl 33 N2005 ---->{g}
C3+R
                     R C3+R 716 -424 91 20 1 cs_nnd2n02c_sl
C2891rwr/y
FC3+R
                                                 670 -424
R C3+R 637 -424
cs invvn01c sl 33 ig empty ----> ig_empty
116 137 3 PI
                     0 iq empty
                                           F C3+R 1729 -408
----- 3 slow_mode_blk.reg_n.lat_0/BASE_REG/a
              05d cl_invvn05d 39 DELAY Setup
0 29 1 cl_invvn
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3- 160
                                           60 238 14 cl_invvn
     1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1729
     0 29 1 AND
                     AND
                           0 DELAY ---->
-408
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1777 -408 105 16 1 AND
AND -48 a ----> slow_mode_blk.reg_n.lat_0/a
                                R C3+R 1777 -408 105 16
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y
1777 -408 105 16 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N95 ----> C2841/a
                                                       RC3+R
F C3+R 1725 -408 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b}
  R C3+R 1681 -408
                   cs_nnd2n02c_sl 45 N512 ---->{c} C2798/y
107 17 1 cs_nnd2n02c_sl
R C3+R 1681 -408 107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N512 ---->
                           1624 -408 89 35 2 cs_nnd2n02c_sl
C2798/a
                     FC3+R
                                          F C3+R 1624 -408
cs nnd2n02c sl 57 N1527 ---> C2778/y
                                                          89
R
C3+R 1554 -408 192 67 4 cs_invvn01c_sl cs_invvn01c_sl 70 N931 ---->{d}
                     R C3+R 1554 -408 192 67 4 cs_nnd2n02c_sl
C2754/y
F C3+R
                                               1445 -408
                                                         101
F C3+R 1445 -408 101 86 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1555 ---->
                    R C3+R 1378 -408 117 23 1 cs_invvn01c_sl
C2588/a
cs_invvn01c_sl 67 N1730 ---->{e} C2554/y
                                          R C3+R 1378 -408 117
```

```
1313 -408
                                                    77 84 5 cs_invvn01c_sl
C2464/y
                              FC3+R
                                                            R C3+R
                                                                     1261 -408
                                                                                  120
               0 N1652 ---> C2464/a
cs invvn01c sl
                        cs invvn01c sl 52 N1749 ---->{f} C2412/v
                                                                                     R
30 1 cs_invvn01c_sl
C3+R
       1261 -408
                    120 30 1 cs_nnd3n02c_sl
                                                   C2412/a
                              FC3+R
                                        1211 -408
                                                   56 27 1 cs_nnd3n02c_sl
cs_nnd3n02c_sl 50 N1713 ---> C1954/y
                                                             FC3+R
                                                                      1211 -408
                                                                                   56
                        cs_invvn01c_sl
                                        0 N1713 ---> C1954/a
                                                                                    R
27 1 cs_invvn01c_sl
                                                  cs_invvn01c_sl 40 br_wrong_targ ---->
       1171 -408
                   175 45 2 cs_invvn01c_sl
                                          1171 -408 175 45 2 PI
                                R C3+R
br_wrong_targ
0 br wrong targ
                          > gbfo_tune_gain -target_frac 0.97 -gain_incr 0.05 -gain_d... C2734rwr
new rep load 313.2 greater than max 300.2: set to max: FREEZE SIZEUP C2738 new rep load 99.96
greater than max 96.3: set to max: FREEZE SIZEUP C2909 new rep load 98.53 greater than max
96.3: set to max: FREEZE SIZEUP C2721rwr new rep load 64.15 greater than max 61.93: set to max:
FREEZE SIZEUP C2917 new rep load 99.33 greater than max 96.3: set to max: FREEZE SIZEUP
                                                      Slack: before -441.6489 after -433.9434
Tune Gain Area: before 4531.42 after 4432.62 (2.18 %)
          Cell: before 787 after 787 (0.00 %) Time: 12.060000
                                                                    for file
write end point report -points 3 [ET-0018]:>Begin...New EndPoint Report
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report. Sun Apr 18 21:56:25
1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                    EDA EinsTimer EndPoint Report
                                                  Max. Slack: 1.13427E+38 Sort Field: Slack
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                       Abbreviation Comparison/Description ------
Max. Endpoints: 3 Cause of Slack
                                                         Slack due to a point downstream on
----- Slack Continuation
                                               SIkCont
                                     ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                            RAT
                            ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Required Arrival Time AssrtRAT
                            ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
Gating Setup
                 ClkGSet
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                               ClkGHld
                                                          ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                        CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                 Setup
                                                                                 Hold
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
(DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle
          ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
                                ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
ClockPulseWidth
                      ClkPW
                                                 ( CLOCK1 ARRIVAL TIME + CLOCK
TRAILING EDGE ) ClockSeparation
                                       ClkSep
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                   ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
          Slack discontinuity due to failed test
                                           Num/
ATLimit
                                        Delay/ Failed Test/ Test PinName
LimitedAT/
         AT Slack Slew CL FO Cell
                                                P Func T.Adj NetName
E Phase
                                                     FC3+R
                                                               1313 -434
                                                                            81 1078 7
                    1 dcd succ last
                      0 dcd_succ_last_t1 RAT
                                                                                879
PO
                                               1313 -434
                                                            81 1078 7 cs_invvn01c_sl
                                     FC3+R
0 ----> C2744/v
                                                                     R C3+R
cs invvn01c sl
                0 dcd_succ_last_t1 ---> C2744/a
-434 121 301 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
                                                    cs nnd2n02c sl
          1259 -434 121 301 4 cs_nnd2n02c_sl
                                                                      0 N675 ---->
R C3+R
C2738/b
                              FC3+R
                                        1191 -434
                                                     79 1260 4 cs_nnd2n02c_sl
                                                              FC3+R
cs nnd2n02c_sl
               68 N1098 ----> C2734rwr/y
                                                                        1191 -434
                                                                                     79
                                          0 N1098 ----> C2734rwr/a
1260 4 cs_invvn01c_sl
                       cs_invvn01c_sl
                       87 306 1 cs_invvn01c_sl
R C3+R
          1143 -434
                                                    cs_invvn01c_sl 47 N1097 ---->
                               R C3+R
                                         1143 -434 87 306 1 cs_invvn01c_sl
C2728rwr/v
                0 N1097 ----> C2728rwr/a
                                                                       1099 -434
                                                                                    70
cs invvn01c sl
                                                             FC3+R
                                        44 N1692 ---->{b} C2725rwr/y
165 2 cs_invvn01c_sl
                      cs_invvn01c_sl
```

84 5 cs nnd2n02c sl

FC3+R

1313 -408

77

cs nnd2n02c sl 66 N1652 ---->

```
1099 -434 70 165 2 cs_nnd2n02c_si
FC3+R
C2725rwr/a
                          R C3+R 1053 -434 133 157 2 cs_nnd3n02c_sl
79 ---->{c} C2721rwr/y
FC3+R
                                               979 -434
979 -434
FC3+R
                          943 -434 81 125 3 cs_nnd2n02c_sl
C2338/a
                   R C3+R
                                        R C3+R 943 -434
                                                       81
cs_nnd2n02c_sl 36 N1119 ----> C2905/y
125 3 cs invvn01c sl cs_invvn01c_sl 0 N1119 ----> C2905/a
                                                        F
     903 -434 68 92 1 cs_invvn01c_sl cs_invvn01c_sl 41 N2010 ---->{e}
C3+R
                  F C3+R 903 -434 68 92 1 cs_nor2n02c_sl
C2906/v
                                       R C3+R
74 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc ----> dcd_blk_dsucc
      868 -434 80 74 1 PI 0 dcd_blk_dsucc
R C3+R
----- 2 slow_mode_blk.reg_n.lat_0/BASE_REG/a F C3+R 1741 -421
0 29 1 cl invvn 05d cl invvn05d 39 DELAY Setup
                                 160 60 238 14 cl_invvn
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3-
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1741
    0 29 1 AND AND 0 DELAY ---->
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1789 -421 105 16 1 AND
                              R C3+R 1789 -421 105 16
    -48 a ----> slow_mode_blk.reg_n.lat_0/a
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y
                                                     R C3+R
                         1789 -421 105 16 1 cs_nnd2n02c_sl
F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b} C2821/y F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl
R C3+R 1693 -421
1693 -421 107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N512 ---->
R C3+R
                   F C3+R 1636 -421 92 35 2 cs_nnd2n02c_sl
C2798/a
                                        FC3+R 1636 -421
cs_nnd2n02c_sl 57 N1527 ----> C2778/y
                                                       92
R
C3+R 1563 -421 198 67 4 cs_invvn01c_sl cs_invvn01c_sl 72 N931 ---->{d}
                   R C3+R 1563 -421 198 67 4 cs_nnd2n02c_si
C2754/v
F C3+R 1450 -421
R C3+R
1381 -421 120 23 1 cs_invvn01c_sl cs_invvn01c_sl 69 N1730 ---->{e} C2554/y
R C3+R 1381 -421 120 23 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1730 ---->
                          1313 -421 79 84 5 cs_nnd2n02c_sl
                   FC3+R
C2554/b
                                        FC3+R 1313 -421
                                                       79
cs_nnd2n02c_sl 68 N1652 ----> C2464/y
                                                        R
C3+R 1260 -421 120 29 1 cs_invvn01c_sl cs_invvn01c_sl 53 N1749
                      R C3+R 1260 -421 120 29 1 cs_nnd3n02c_sl
---->{f} C2412/y
                                        F C3+R 1210 -421
F C3+R 1210 -421
                    R C3+R 1171 -421 175 46 2 cs_invvn01c_sl
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ
                                             R C3+R
-421 175 46 2 Pl 0 br_wrong_targ
                                   R C3+R 1349 -420 123 1078 7
----- 3 dcd succ last
PO 0 dcd_succ_last_t1 RAT 0 ----> C2744/y R C3±R
                                                     929
                        R C3+R 1349 -420 123 1078 7 cs_invvn01c_sl
                                             F C3+R 1282
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
```

```
-420
       85 301 4 cs_invvn01c_sl
                                      cs_invvn01c sl
                                                     67 N675 ---->{a} C2738/y
FC3+R
          1282 -420
                      85 301 4 cs_nnd2n02c sl
                                                      C2738/b
                               R C3+R
                                         1230 -420
                                                      120 1260 4 cs nnd2n02c sl
cs_nnd2n02c_sl
                 52 N1098 ---->
                               C2734rwr/v
                                                                RC3+R
                                                                          1230 -420
120 1260 4 cs_invvn01c sl
                                cs_invvn01c_sl
                                                0 N1098 ----> C2734rwr/a
F C3+R
          1171 -420
                       59 306 1 cs_invvn01c_sl
                                                     cs_invvn01c_sl 59 N1097 ---->
C2728rwr/y
                                FC3+R
                                          1171
                                                -420
                                                       59 306 1 cs_invvn01c sl
cs_invvn01c_sl
                0 N1097 ----> C2728rwr/a
                                                              R C3+R
                                                                        1135 -420
                                                                                     101
165 2 cs_invvn01c_sl
                          cs_invvn01c_sl
                                          36 N1692 ---->{b} C2725rwr/y
R C3+R
          1135 -420
                       101 165 2 cs nnd2n02c sl
                                                       cs_nnd2n02c_sl
                                                                        0 N1692 ---->
C2725rwr/a
                                FC3+R
                                          1081 -420
                                                       93 157 2 cs nnd2n02c sl
cs_nnd2n02c_sl 54 N1479 ---->{c} C2721rwr/v
                                                                FC3+R
                                                                          1081 -420
                          -cs_nnd3n02c_sl
93 157 2 cs_nnd3n02c sl
                                               0 N1479 ----> C2721rwr/a
->{d} C2709rwr/v
                                     R C3+R
                                               1015 -420 214 120 2 cs_nor3n03c_sl
cs_nor3n03c_sl
                0 N1497 ----> C2709rwr/a
                                                              FC3+R
                                                                         920 -420
                                                                                     59
51 1 cs_nor3n03c_sl
                         cs_nor3n03c_sl 95 N1986 ---->{e} C2677rwr_0/y
FC3+R
          920 -420
                       59 51 1 cs_nnd2n02c_sl
                                                     cs_nnd2n02c_sl
                                                                      0 N1986 ---->
C2677rwr 0/b
                                 RC3+R
                                            887 -420
                                                        90 97 2 cs_nnd2n02c_sl
cs_nnd2n02c_si 33 N1094 ---->{f} C2909/y
                                                              RC3+R
                                                                         887 -420
97 2 cs_nnd2n02c_sl
                          cs_nnd2n02c_sl
                                           0 N1094 ---> C2909/b
FC3+R
          835 -420
                      80 90 1 cs_nnd2n02c_sl
                                                 cs_nnd2n02c sl 52 dcd mcr41 blk
----> dcd_mcr41_blk
                                       FC3+R
                                                  835 -420 80 90 1 PI
0 dcd_mcr41_blk
cap violation 1.032, load 145.5, limit 141, multiplier
                                                1 slack 1.134e+38 INet clkg2:clkg2 has cap
violation 1.032, load 145.5, limit 141, multiplier
                                            1 slack 1.134e+38 INet du_iu_store_status(2):a
has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500,
limit 455 INet eu_iu_srlz_op_encode(11):a has transition violation 1.099, multiplier
                                                                           1 RISE:
transition 500, limit 455; FALL: transition 500, limit 455 INet dcd_succ_last_t1:y has cap violation
1.077, load 1078, limit 1001, multiplier
                                    1 slack -433.9 INet frc_blk_1cyc_q:l2_out_n has cap
violation 1.008, load 248.9, limit 247, multiplier 1 slack -224.9 INet N22:y has cap violation 1.204,
load 1205, limit 1001, multiplier
                               1 slack 604.5 INet N26:y has cap violation 1.216, load 1218,
limit 1001, multiplier
                     1 slack 370.7 INet N36:y has cap violation 1.179, load 1180, limit 1001,
          1 slack 606.1 INet N1098:y has cap violation 1.258, load 1260, limit 1001, multiplier
1 slack -433.9 INet gbfonet_2:y has cap violation 1.218, load 1219, limit 1001, multiplier
27.29 INet gbfonet_15:y has cap violation 1.169, load 1170, limit 1001, multiplier
INet gbfonet_16:y has cap violation 1.108, load 1109, limit 1001, multiplier
                                                                    1 slack 477.9 IDesign
IDCDSUC has 13 violations
                                  > report_gain_violations -min 1.0 -max 10.0
----- Gain Violation Report for design IDCDSUC
----- Type
                                            Gain
                                                                  Cell Name
Design ----- Max
                                            10.196948 C2194
                                                                 cs_invvn01c_sl Min
0.672053
           C2894
                     cs_nnd2n02c_sl Max
                                            13.197469
                                                      C2895
                                                                 cs_invvn01c_sl Max
12.994584 C2907
                     cs_invvn01c_sl Max
                                            12.966053 C2918
                                                                  cs_nor2n02c_sl Min
0.719591 C2677rwr_0 cs_nnd2n02c_sl
                                               > trace::set -group critflow -how many
> trace::set -group trestruct -where what
                                              > tc::trestruct -sizeless -leaf_flex 1.02 -gain 5
-load 5 GA_Tree: MinLoad=5.672 MaxLoad=300.341
                                                         > tc::critflow -depth 3 -xforms
 _CiType_30_31e1e638 Transform: trestruct 0.1 Options: Mode=Sizeless
                                                                   GainBuckets=5
LoadBuckets=5
                  MinInputs=2
                                MaxInputs=1024
                                                    PartialTree=false
SingleCell=false
                  SlackThreshold=0.000
                                           LeafFlexibility=1.020 Critical Slack = -433.943
GA_Tree: Considering net: dcd_blk_dsucc GA_Tree: Considering net: N2010 GA_Tree: Considering net:
putSlack=-433.943 Area=0.000 Delta Evaluate: A=-11.954|-12.462 S=32.916|21.555 Implementing best
tree. Delta Results: Slack=-21.268 InputSlack=-21.268 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: N892 Working on tree: 'N892' Inputs=2 A=962.086|979.016 S=93.872|65.062
```

```
Slack=-433.943 InputSlack=-433.943 Area=0.000 Delta Evaluate: A=-36.531|-30.189 S=-34.489|-18.359
Implementing best tree. Delta Results: Slack=-44.750 InputSlack=-44.750 Area=0.000 Restoring
original tree. [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below.
GA_Tree: Considering net: N1479 Working on tree: 'N1479' Inputs=6 A=1053.450|1081.162
S=133.481|92.901 Slack=-433.943 InputSlack=-433.943 Area=0.000 Delta Evaluate: A=-12.015|5.378
S=33.067|28.576 Implementing best tree. Delta Results: Slack=-12.047 InputSlack=-12.047 Area=0.000
Restoring original tree. [ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP,
and below. GA_Tree: Considering net: N1692 Working on tree: 'N1692' Inputs=2 A=1135.031|1098.978
S=100.648|70.117 Slack=-433.943 InputSlack=-433.943 Area=0.000 Delta Evaluate:
A=-55.608|-48.063 S=-72.414|-41.996 Implementing best tree. Delta Results: Slack=-63.178
InputSlack=-63.178 Area=0.000 Restoring original tree. [ET-0112]:Deleting timing for design:
sub design, analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N1097 GA_Tree:
Considering net: N1098 Working on tree: 'N1098' Inputs=1 A=1229.972|1190.680 S=119.887|78.756
Slack=-433.943 InputSlack=-433.943 Area=0.000 Restoring original tree. [ET-0112]:Deleting timing for
design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N675 Working
on tree: 'N675' Inputs=7 A=1258.629|1281.562 S=121.113|84.932 Slack=-433.943
InputSlack=-433.943 Area=0.000 Delta Evaluate: A=0.072|0.060 S=35.518|32.435 Implementing best
tree. Delta Results: Slack=0.092 InputSlack=0.091 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: dcd_succ_last_t1 Working on tree: 'dcd_succ_last_t1' Inputs=1 A=1348.840|1312.943
S=123.248|80.835 Slack=-433.943 InputSlack=-433.943 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: dcd_mcr41_blk GA_Tree: Considering net: N1094 Working on tree: 'N1094' Inputs=3
A=887.225|884.198 S=90.491|62.574 Slack=-429.858 InputSlack=-429.858 Area=0.000 Delta
Evaluate: A=0.750|0.595 S=37.597|31.491 Implementing best tree. Delta Results: Slack=0.833
InputSlack=0.833 Area=0.000 Restoring original tree. [ET-0112]:Deleting timing for design: sub_design,
analysis mode:SLOW_CHIP, and below. GA_Tree: Considering net: N1986 GA_Tree: Considering net:
N1497 Working on tree: 'N1497' Inputs=6 A=1015.222|981.022 S=213.506|99.542 Slack=-429.858
InputSlack=-429.858 Area=0.000 Delta Evaluatè: A=-23.138|-11.666 S=28.044|53.449 Implementing
best tree. Delta Results: Slack=-32.589 InputSlack=-32.588 Area=0.000 Restoring original tree.
[ET-0112]:Deleting timing for design: sub_design, analysis mode:SLOW_CHIP, and below. GA_Tree:
Considering net: op_cmp_raw Restoring original tree. [ET-0112]:Deleting timing for design: sub_design,
analysis mode:SLOW CHIP, and below. GA_Tree: Considering net: N1717 GA_Tree: Considering net:
                                                     > reset_timing_area
                                                                                     > report_drc
N1437 GA_Tree: Considering net: N1858
Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap violation 1.032, load 145.5, limit 141,
            1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141,
multiplier
            1 slack 1.134e+38 INet du_iu_store_status(2):a has transition violation 1.099, multiplier
multiplier
1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet eu_iu_srlz_op_encode(11):a
                                  1 RISE: transition 500, limit 455; FALL: transition 500, limit
nsition violation 1.099, multiplier
455 INet dcd_succ_last_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier
                                                                                       1 slack
-433.9 INet frc_blk_1cyc_q:l2_out_n has cap violation 1.008, load 248.9, limit 247, multiplier
slack -203.7 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier
INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier
                                                                     1 slack 381.3 INet N36:y has
                                                       1 slack 616.2 INet N1098:y has cap violation
cap violation 1.179, load 1180, limit 1001, multiplier
                                          1 slack -433.9 INet gbfonet_2:y has cap violation 1.218,
1.258, load 1260, limit 1001, multiplier
                                   1 slack 27.29 INet gbfonet_15:y has cap violation 1.169, load
load 1219, limit 1001, multiplier
                              1 slack 349.9 INet gbfonet_16:y has cap violation 1.108, load 1109,
1170, limit 1001, multiplier
                        1 slack 478 IDesign IDCDSUC has 13 violations
                                                                                      > echo
limit 1001, multiplier
                                                             > ps -cell Design /HISVHDL/IDCDSUC
{Custom Synzilla Report} Custom Synzilla Report
                                                                          787 cells (1 AND: 0 XOR: 0
             1 instances 0 upcells
                                     122 IN ports 73 OUT ports
                                                              1008 nets (0 multiply-driven; 0 undriven)
SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC)
                                                  0 buses
                                                                          10 max fanin
2632 pins (0 inversions) 2.61 pins per net
                                                  1551 literals 21 levels
                                                              FUNC_STRAIGHT_WIRE_DESIGN
                         Cell Information
15 max fanout
                                                                   (ncount 83: area
                                                                                         0)
                                                  PSEUDO_REG
(ncount 180 : area
                       0)
                                                              cb_mode_block (ncount
                                                                                        1 : area
                                   480)
cb clk 32 1 (ncount
                         6: area
```

```
cs_ao12n03c_sl (ncount
                                             6: area
                                                        24)
cs_ao22n03c_sl (ncount 16: area
                                  96)
                                                        cs_invvn01c_sl (ncount 228 : area
456)
                       cs_nnd2n02c_sl (ncount 208 : area
                                                        624)
cs_nnd3n02c_sl (ncount 30 : area
                                 120)
                                                        cs_nnd4n03c_sl (ncount
                                                                               7: area
                       cs_nor2n02c_sl (ncount 13 : area
35)
                                                        39)
cs_nor3n03c_sl (ncount 2 : area
                                                        cs_oa21n03c_sl (ncount
                                                                               3: area
15)
                      cs_oa22n03c_sl (ncount 1 : area
cs_xbn2n01b_sl (ncount 1 : area
                                  8)
                                                        cs xbo2n01b sl (ncount
                                                                               1: area
                       Total Area = 1989 (Comb = 1439 : Non-Comb = 550)
write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
                                                                       for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
                                                                     Sun Apr 18 21:56:39
1999 Part: IDCDSUC Mode: Late Mode / Nominal
                                                       EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack
                                                     Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description
                            Slack due to a point downstream on path Required Arrival Time
Continuation
                  SlkCont
         ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
RAT
( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
                                                                             ClkGSet
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating
           ClkGHld
                     ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
+ ADJUST ) Clock Tree Pulse Width ClkTPW
                                               ( CLOCK LEADING EDGE + PULSE WIDTH <
CLOCK TRAILING EDGE ) Setup
                                            Setup
                                                      ( DATA ARRIVAL TIME + SETUP <
CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                             ( DATA ARRIVAL TIME - HOLD
                                                    Hold
> CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                         EndOfC
                                                                    ( DATA ARRIVAL TIME
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
                                                                    ClkPW
                                                                               (CLOCK
 ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) LOOP
ALTest
          ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
Arrival Time Limiting
                                 Slack discontinuity due to failed test ... ... Num/
                       ATLimit
LimitedAT/
                                         Delay/ Failed Test/ Test PinName
          AT Slack Slew CL FO Cell
E Phase
                                                 P Func T.Adj NetName
                    1 dcd_succ_last -
                                                       FC3+R.
                                                                 1313 -434
                                                                              81 1078 7
PO
                       0 dcd_succ_last_t1 RAT
                                                                                  879
0 ----> C2744/v
                                      FC3+R
                                                1313 -434
                                                             81 1078 7 cs invvn01c sl
cs_invvn01c_sl
                0 dcd_succ_last_t1 ----> C2744/a
                                                                       R C3+R
                                                                                 1259
-434 121 301 4 cs_invvn01c_sl
                                                     54 N675 ---->{a} C2738/y
                                   cs invvn01c sl
R C3+R
                     121 301 4 cs_nnd2n02c_sl
         1259
               -434
                                                       cs_nnd2n02c_sl
                                                                        0 N675 ---->
C2738/b
                               FC3+R
                                         1191 -434
                                                      79 1260 4 cs nnd2n02c sl
                68 N1098 ----> C2734rwr/y
cs_nnd2n02c_sl
                                                               FC3+R
                                                                          1191 -434
                                                                                       79
                           cs invvn01c_sl
1260 4 cs invvn01c sl
                                           0 N1098 ----> C2734rwr/a
RC3+R
          1143 -434
                       87 306 1 cs invvn01c sl
                                                      cs_invvn01c sl 47 N1097 ---->
C2728rwr/v
                                R C3+R
                                          1143 -434
                                                       87 306 1 cs_invvn01c_sl
                0 N1097 ----> C2728rwr/a
cs_invvn01c_sl
                                                              FC3+R
                                                                        1099 -434
                                                                                      70
165 2 cs_invvn01c_sl
                          cs_invvn01c_sl
                                         44 N1692 ---->{b} C2725rwr/v
FC3+R
         1099 -434
                       70 165 2 cs_nnd2n02c_sl
                                                      cs_nnd2n02c_sl
                                                                       0 N1692 ---->
C2725rwr/a
                                R C3+R
                                          1053 -434
                                                      133 157 2 cs_nnd2n02c sl
cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y
                                                                R C3+R
                                                                          1053 -434
133 157 2 cs_nnd3n02c sl
                                                 0 N1479 ----> C2721rwr/c
                                cs nnd3n02c sl
FC3+R
          979 -434
                      65
                          118 2 cs_nnd3n02c si
                                                      cs_nnd3n02c_sl
                                                                      74 N892 ---->{d}
C2338/v
                               FC3+R
                                         979 -434
                                                     65 118 2 cs nnd2n02c sl
cs nnd2n02c sl
                 0 N892 ---> C2338/a
                                                             RC3+R
                                                                        943 -434
                                                                                    81
125 3 cs nnd2n02c sl
                                           36 N1119 ----> C2905/y
                           cs_nnd2n02c_si
RC3+R
          943 -434
                       81
                          125 3 cs_invvn01c sl
                                                     cs_invvn01c sl
                                                                     0 N1119 ---->
C2905/a
                               FC3+R
                                         903 -434
                                                     68 92 1 cs_invvn01c_sl
cs_invvn01c_sl 41 N2010 ---->{e} C2906/y
                                                              FC3+R
                                                                         903 -434
                                                                                     68
```

70)

```
R
92 1 cs nor2n02c_sl
                                             cs_nor2n02c_si
                                                                  35 dcd_blk_dsucc ---->
        868 -434
                    80 74 1 cs nor2n02c_sl
C3+R
                    0 dcd_blk_dsucc
                    2 slow_mode_blk.reg_n.lat_0/BASE_REG/a
                                                                 FC3+R
                                                                           1741 -421
                        05d cl invvn05d 39 DELAY Setup
0 29 1 cl invvn
slow_mode_blk.reg_n.lat_0/BASE_REG/c1
                                                               60 238 14 cl_invvn
                                            F C3-
                                                     160
        1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                                      FC3+R
05d
                                         0 DELAY ---->
-421
       0 29 1 AND
                                AND
                                                         1789 -421 105 16 1 AND
slow mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1
                                               R C3+R
                                                                  1789 -421
       -48 a ----> slow_mode_blk.reg_n.lat_0/a
                                                        R C3+R
                                                                                 RC3+R
                        PSEUDO_REG
                                        0 a ---->{a} C2841/y
1 PSEUDO_REG
1789 -421 105 16 1 cs_nnd2n02c_sl
                                            cs_nnd2n02c_sl
                                                             0 N95 ----> C2841/a
                                                     cs_nnd2n02c_sl 52 N935 ---->{b}
                      75 17 1 cs_nnd2n02c_sl
         1738 -421
FC3+R
                              FC3+R
                                        1738 -421
                                                     75 17 1 cs_nnd2n02c_sl
C2821/v
                                                            RC3+R
                                                                      1693 -421
                                                                                   107
                0 N935 ---> C2821/b
cs nnd2n02c_sl
                         cs_nnd2n02c_sl 45 N512 ---->{c} C2798/y
17 1 cs nnd2n02c sl
                                                   cs_nnd2n02c_sl
                                                                       0 N512 ---->
                           17 1 cs nnd2n02c_sl
R C3+R
         1693 -421
                      107
                                                     92 35 2 cs_nnd2n02c_sl
                              FC3+R
                                        1636 -421
C2798/a
                                                                                     92
                                                              FC3+R
                                                                       1636 -421
cs nnd2n02c_sl 57 N1527 ----> C2778/y
                                        0 N1527 ----> C2778/a
                                                                                     R
                        cs invvn01c sl
35 2 cs_invvn01c_sl
                     198 67 4 cs_invvn01c_sl cs_invvn01c_sl 72 N931 ---->{d}
        1563 -421
C3+R
                                        1563 -421 198 67 4 cs_nnd2n02c_sl
                              R C3+R
C2754/v
                                                            FC3+R
                                                                      1450 -421
                                                                                   104
                0 N931 ---> C2754/b
cs_nnd2n02c_sl
                         cs_nnd2n02c_sl 113 N1555 ----> C2588/y
86 5 cs_nnd2n02c_sl
                      104 86 5 cs_invvn01c_sl
                                                     cs_invvn01c_sl
                                                                     0 N1555 ---->
FC3+R
         1450 -421
                                                     120 23 1 cs_invvn01c_sl
                                         1381 -421
C2588/a
                               RC3+R
                                                              R C3+R
                                                                                    120
                                                                        1381 -421
              69 N1730 ---->{e} C2554/y
cs invvn01c sl
                                         0 N1730 ----> C2554/b
                         cs nnd2n02c_sl
23 1 cs nnd2n02c sl
                                                                     68 N1652 ---->
                                                     cs_nnd2n02c_sl
                       79 84 5 cs_nnd2n02c_sl
FC3+R
         1313 -421
                                                     79 84 5 cs_invvn01c_st
                              FC3+R
                                        1313 -421
C2464/v
                                                             RC3+R
                                                                       1260 -421
                                                                                   120
cs invvn01c sl 0 N1652 ----> C2464/a
                        cs_invvn01c_sl
                                       53 N1749
29 1 cs invvn01c_sl
                                              1260 -421
                                                           120 29 1 cs nnd3n02c_sl
                                     R C3+R
---->{f} C2412/y
                                                             FC3+R
                                                                       1210 -421
                 0 N1749 ----> C2412/a
cs nnd3n02c sl
                       cs_nnd3n02c_sl 50 N1713 ----> C1954/v
27 1 cs_nnd3n02c_sl
                       55 27 1 cs_invvn01c_sl
                                                                    0 N1713 --->
                                                    cs_invvn01c_sl
FC3+R
          1210 -421
                                         1171 -421 175 46 2 cs_invvn01c_sl
                               RC3+R
C1954/a
                                                                     R C3+R
                                                                                1171
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ
                                    0 br_wrong_targ
-421 175 46 2 PI
                           > report_area    Design: /IDCDSUC - Area: 4432.619141,
                              > cputime Used 129.23 cpu seconds or 00:02:13 wall time,
Area(Weight): 1283.903442
                                                           > echo {In gain tuning loop} In
used 262144 bytes or 256 kbytes.
                                      > cpr_eval
               > echo -425.923987771 -425.923987771
                                                                      > echo
gain tuning loop
                                     > report_drc Checking DRC for IDesign IDCDSUC INet
-433.943389893 -433.943389893
clkg:clkg has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet
clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet
du_iu_store_status(2):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455;
FALL: transition 500, limit 455 lNet eu_iu_srlz_op_encode(11):a has transition violation 1.099.
           1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet
dcd_succ_last_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier
                                                                     1 slack -433.9 INet
frc_blk_1cyc_q:l2_out_n has cap violation 1.008, load 248.9, limit 247, multiplier
                                                                         1 slack -203.7
INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 614.9 INet N26:y has
```

cap violation 1.216, load 1218, limit 1001, multiplier 1 slack 381.3 INet N36:y has cap violation

```
1.179, load 1180, limit 1001, multiplier 1 slack 616.2 INet N1098:y has cap violation 1.258, load
                          1 slack -433.9 INet gbfonet_2:y has cap violation 1.218, load 1219,
1260, limit 1001, multiplier
limit 1001, multiplier
                     1 slack 27.29 INet gbfonet_15:y has cap violation 1.169, load 1170, limit
                1 slack 349.9 INet gbfonet_16:y has cap violation 1.108, load 1109, limit 1001,
1001, multiplier
multiplier
           1 slack 478 IDesign IDCDSUC has 13 violations
                                                                > write_end_point_report
-points 3 [ET-0018]:>Begin...New EndPoint Report
                                                  for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report.
                                         Sun Apr 18 21:56:42 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                          EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                    Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 3 Cause of Slack
                                         Abbreviation Comparison/Description -----
----- Slack Continuation
                                                SlkCont
                                                           Slack due to a point downstream on
path Required Arrival Time
                             RAT
                                       ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT
                              ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                  ClkGSet
                             ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                 ClkGHld
                                                            ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                           CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                   Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                    Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
DGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation
                                                                      ClkSep
                                                                                (CLOCK1
ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
          ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
ALTest
Arrival Time Limiting
                      ATLimit
                                 Slack discontinuity due to failed test
LimitedAT/
                                          Delay/ Failed Test/
                                                             Test PinName
E Phase
                                                  P Func T.Adj NetName
           AT Slack Slew CL FO Cell
                    1 dcd_succ_last
                                                       FC3+R
                                                                 1313 -434
                                                                              81 1078 7
PO
                       0 dcd_succ_last_t1 RAT
                                                                                  879
0 ----> C2744/y
                                      FC3+R
                                                1313 -434
                                                              81 1078 7 cs_invvn01c_sl
cs_invvn01c_sl
                0 dcd_succ_last_t1 ---> C2744/a
                                                                       RC3+R
                                                                                 1259
-434 121 301 4 cs_invvn01c_sl
                                                      54 N675 ---->{a} C2738/v
                                    cs_invvn01c_sl
R C3+R
          1259
               -434
                      121 301 4 cs_nnd2n02c_sl
                                                       cs_nnd2n02c sl
                                                                        0 N675 --->
C2738/b
                               FC3+R
                                         1191 -434
                                                      79 1260 4 cs nnd2n02c sl
cs_nnd2n02c_sl
                68 N1098 ---->
                               C2734rwr/v
                                                                FC3+R
                                                                          1191 -434
                                                                                       79
1260 4 cs invvn01c sl
                           cs invvn01c sl
                                           0 N1098 ----> C2734rwr/a
R C3+R
          1143 -434
                       87
                           306 1 cs_invvn01c sl
                                                      cs invvn01c sl
                                                                     47 N1097 ---->
C2728rwr/y
                                R C3+R
                                          1143
                                                -434
                                                       87 306 1 cs invvn01c sl
cs_invvn01c_sl
                0 N1097 ---->
                              C2728rwr/a
                                                              FC3+R
                                                                        1099 -434
                                                                                      70
165 2 cs invvn01c sl
                          cs_invvn01c_sl
                                          44 N1692 ---->{b} C2725rwr/v
         1099 -434
FC3+R
                       70 165 2 cs_nnd2n02c_sl
                                                      cs_nnd2n02c_sl
                                                                       0 N1692 ---->
C2725rwr/a
                                RC3+R
                                          1053 -434
                                                       133 157 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl
                46 N1479 ---->{c} C2721rwr/y
                                                                R C3+R
                                                                           1053
133 157 2 cs_nnd3n02c_sl
                                cs_nnd3n02c_sl
                                                 0 N1479 ---->
                                                               C2721rwr/c
FC3+R
          979 -434
                      65
                          118 2 cs_nnd3n02c_sl
                                                      cs_nnd3n02c_sl 74 N892 ---->{d}
C2338/y
                               FC3+R
                                         979 -434
                                                         118 2 cs nnd2n02c sl
                                                     65
cs_nnd2n02c_sl
                0 N892 ---->
                              C2338/a
                                                             RC3+R
                                                                        943 -434
                                                                                    81
125 3 cs_nnd2n02c sl
                           C2905/y
R C3+R
          943 -434
                           125 3 cs invvn01c sl
                                                     cs_invvn01c_sl
C2905/a
                                                          92 1 cs_invvn01c_sl
                               FC3+R
                                         903 -434
                                                      68
cs_invvn01c_sl 41 N2010 ---->{e} C2906/y
                                                              FC3+R
                                                                         903
                                                                              -434
                                                                                     68
92 1 cs_nor2n02c sl
                         cs nor2n02c sl
                                          0 N2010 ----> C2906/a
                                                                                        R
C3+R
        868 -434
                     80
                         74 1 cs_nor2n02c_sl
                                                   cs_nor2n02c_sl
                                                                   35 dcd_blk_dsucc ---->
succ
                        R C3+R
                                   868 -434
                                               80
                                                   74 1 PI
                                                                               0
dcd_blk_dsucc
```

```
-----2 slow_mode_blk.reg_n.lat_0/BASE_REG/a
                                              F C3+R 1741 -421
               05d cl invvn05d 39 DELAY Setup
0 29 1 cl invvn
                                          60 238 14 cl_invvn
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3-
                                      160
     1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                   F C3+R
05d
                             0 DELAY ---->
                AND
     0 29 1 AND
-421
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R
                                         1789 -421 105 16 1 AND
                                         R C3+R 1789 -421 105 16
     -48 a ----> slow_mode_blk.reg_n.lat_0/a
                                                           RC3+R
                 PSEUDO_REG 0 a ---->{a} C2841/y
1 PSEUDO REG
                                           0 N95 ----> C2841/a
                               cs nnd2n02c_sl
1789 -421 105 16 1 cs_nnd2n02c_sl
     1738 -421 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b}
F C3+R
                            1738 -421
                                      75 17 1 cs_nnd2n02c_sl
                      FC3+R
C2821/v
                                                   1693 -421 107
                                            R C3+R
cs nnd2n02c sl 0 N935 ----> C2821/b
107 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl
                                                   0 N512 ---->
R C3+R 1693 -421
                            1636 -421 92 35 2 cs_nnd2n02c_sl
                      FC3+R
C2798/a
cs_nnd2n02c_sl 57 N1527 ---> C2778/v
                                            FC3+R
                                                   1636 -421
                                                              92
1563 -421 198 67 4 cs_invvn01c_sl cs_invvn01c_sl 72 N931 ---->{d}
                            1563 -421 198 67 4 cs_nnd2n02c_sl
                      R C3+R
C2754/v
                                            FC3+R
                                                   1450 -421
                                                            104
1450 -421 104 86 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1555 ---->
R C3+R 1381 -421 120 23 1 cs_invvn01c_sl
F C3+R
C2588/a
                                             R C3+R 1381 -421
                                                              120
cs invvn01c sl 69 N1730 ---->{e} C2554/y
               23 1 cs_nnd2n02c_sl
                79 84 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 68 N1652 ----> F C3+R 1313 -421 79 84 5 cs_invvn01c_sl
      1313 -421
F C3+R
C2464/v
                                            R C3+R
                                                   1260 -421 120
R C3+R 1260 -421 120 29 1 cs_nnd3n02c_sl
---->{f} C2412/v
                                             F C3+R 1210 -421
           0 N1749 ----> C2412/a
cs nnd3n02c sl
0 N1713 ---->
F C3+R 1210 -421
C1954/a
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ
                                                 R C3+R
-421 175 46 2 Pl 0 br_wrong_targ
                                      R C3+R 1349 -420 123 1078 7
              3 dcd_succ_last
               0 dcd_succ_last_t1 RAT
PO
                          R C3+R 1349 -420 123 1078 7 cs_invvn01c_sl
0 ---> C2744/y
cs_invvn01c_sl 0 dcd_succ_last_t1 ---> C2744/a
                                                   F C3+R
                                                         1282
    85 301 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
      1282 -420 85 301 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
FC3+R
                             1230 -420 120 1260 4 cs_nnd2n02c_sl
                      R C3+R
                                              R C3+R
                                                     1230 -420
cs_nnd2n02c_sl 52 N1098 ----> C2734rwr/y
                                   0 N1098 ----> C2734rwr/a
                   cs_invvn01c_sl
120 1260 4 cs_invvn01c_sl
       1171 -420 59 306 1 cs_invvn01c_sl
                                       cs_invvn01c_sl 59 N1097 ---->
                              1171 -420 59 306 1 cs_invvn01c_sl
C2728rwr/y
                       FC3+R
                                             R C3+R 1135 -420
1135 -420 101 165 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N1692 ---->
R C3+R
                              1081 -420 93 157 2 cs_nnd2n02c_sl
                       FC3+R
C2725rwr/a
                                              FC3+R
                                                     1081 -420
cs_nnd2n02c_sl 54 N1479 ---->{c} C2721rwr/y
                     93 157 2 cs_nnd3n02c_sl
```

```
C2709rwr/y
                               R C3+R
                                         1015 -420
                                                     214 120 2 cs nor3n03c sl
cs_nor3n03c_sl
                0 N1497 ---> C2709rwr/a
                                                             FC3+R
                                                                       920 -420
                                                                                   59
51 1 cs_nor3n03c_sl
                         cs_nor3n03c_sl 95 N1986 ---->{e} C2677rwr_0/y
FC3+R
          920 -420
                      59 51 1 cs_nnd2n02c sl
                                                    cs_nnd2n02c_st 0 N1986 ---->
C2677rwr 0/b
                                R C3+R
                                           887 -420
                                                       90 97 2 cs_nnd2n02c_sl
cs_nnd2n02c_sl 33 N1094 ---->{f} C2909/y
                                                             R C3+R
                                                                       887 -420
                                                                                   90
97 2 cs_nnd2n02c_sl
                         cs_nnd2n02c sl
                                          0 N1094 ---> C2909/b
FC3+R
          835 -420
                      80 90 1 cs_nnd2n02c_sl
                                                   cs_nnd2n02c_sl 52 dcd mcr41 blk
----> dcd_mcr41_blk
                                       FC3+R
                                                 835 -420
                                                            80 90 1 PI
0 dcd mcr41 blk
  > tafs redund -effort 50
                                 > cputime { tgfs_rewire -tech -$rwr_effort }
tafs_rewire -tech -high tafs rewiring
                               Area: before 4432.62 after 4434.25 (-0.04 %)
-433.9434 after -433.9434 (0.00 %)
                                Cell: before 787 after 787 (0.00 %) Time: 10.200000 Used
11.55 cpu seconds or 00:00:11 wall time, used 0 bytes or 0 byte.
                                                               > write_end_point_report
-points 3 [ET-0018]:>Begin...New EndPoint Report
                                                 for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report.
                                        Sun Apr 18 21:56:57 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                         EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                  Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 3 Cause of Slack
                                      Abbreviation Comparison/Description ------
----- Slack Continuation
                                               SlkCont
                                                         Slack due to a point downstream on
path Required Arrival Time
                                      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
                            RAT
Required Arrival Time AssrtRAT
                             ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                 ClkGSet
                            ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                               ClkGHld
                                                          ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                        ClkTPW (
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                 Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                 Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
EndOfC
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
ClockPulseWidth
                      ClkPW
                                 ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation
                                       ClkSep
                                                ( CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                  ALTest
                                                                             (DATA
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
ATLimit
          Slack discontinuity due to failed test
                                           Num/
LimitedAT/
                                        Delay/ Failed Test/ Test PinName
E Phase
          AT Slack Slew CL FO Cell
                                                P Func T.Adj NetName
                   1 dcd_succ_last
                                                     FC3+R
                                                               1313 -434
                                                                           81 1078 7
PO
                      0 dcd_succ_last_t1 RAT
                                                                               879
0 ----> C2744/v
                                     FC3+R
                                              1313 -434
                                                           81 1078 7 cs_invvn01c sl
cs_invvn01c_sl
               0 dcd_succ_last_t1 ---> C2744/a
                                                                    R C3+R 1259____
-434 121 305 4 cs_invvn01c sl
                                                    54 N675 ---->{a} C2738/y
                                 cs_invvn01c_sl
RC3+R
          1259 -434 121 305 4 cs_nnd2n02c_sl
                                                     cs_nnd2n02c sl 0 N675 ---->
C2738/b
                              FC3+R
                                       1191 -434
                                                    79 1261 4 cs_nnd2n02c_si
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y
                                                              FC3+R
                                                                      1191 -434
                                                                                    79
R C3+R
          1143 -434
                      87 306 1 cs_invvn01c_sl
                                                     cs_invvn01c_sl
                                                                  47 N1097 ---->
C2728rwr/v
                               R C3+R
                                        1143 -434
                                                     87 306 1 cs invvn01c sl
cs invvn01c sl
               0 N1097 ----> C2728rwr/a
                                                             FC3+R
                                                                      1099 -434
                                                                                   70
165 2 cs invvn01c sl
                         cs_invvn01c_sl 44 N1692 ---->{b} C2725rwr/y
FC3+R
         1099 -434
                      70 165 2 cs_nnd2n02c_sl
                                                     cs_nnd2n02c_sl
                                                                     0 N1692 ---->
C2725rwr/a
                               R C3+R
                                        1053 -434 133 157 2 cs_nnd2n02c_sl
cs nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y
                                                              R C3+R
                                                                        1053 -434
133 157 2 cs_nnd3n02c_sl
```

cs\_nnd3n02c\_sl 66 N1497 ---->{d}

1015 -420 214 120 2 cs\_nnd3n02c\_sl

R C3+R

```
F C3+R 979 -434 65 118 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 74 N892 ---->{d} C2338/y F C3+R 979 -434 65 118 2 cs_nnd2n02c_sl
                                          R C3+R 943 -434
R C3+R
                  F C3+R 903 -434 68 92 1 cs_invvn01c_sl
C2905/a
F C3+R 903 -434
      868 -434 80 74 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc ---->
C3+R
                     R C3+R 868 -434 80 74 1 PI
dcd_blk_dsucc
dcd blk dsucc
______ 2 slow_mode_blk.reg_n.lat_0/BASE_REG/a F C3+R 1741 -421
0 29 1 cl invvn 05d cl_invvn05d 39 DELAY Setup
slow_mode_blk.reg_n.lat_0/BASE_REG/c1 F C3- 160 60 238 14 cl_invvn
05d 1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT F C3+R 1741
     0 29 1 AND AND 0 DELAY ---->
-421
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1789 -421 105 16 1 AND
     -48 a ----> slow_mode_blk.reg_n.lat_0/a R C3+R 1789 -421 105 16
1 PSEUDO_REG PSEUDO_REG 0 a ---->{a} C2841/y
                                                        RC3+R
                          1789 -421 105 16 1 cs_nnd2n02c_sl
F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 52 N935 ---->{b} C2821/y F C3+R 1738 -421 75 17 1 cs_nnd2n02c_sl
                                          R C3+R 1693 -421 107
17 1 cs_nnd2n02c_sl cs_nnd2n02c_sl 45 N512 ---->{c} C2798/y
R C3+R 1563 -421 198
C3+R 1563 -421 198 67 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N931 ---->
C2754/b F C3+R 1450 -421 104 86 5 cs_nnd2n02c_sl cs_nnd2n02c_sl 113 N1555 ----> C2588/y F C3+R 1450
                                           F C3+R 1450 -421
                                                           104
C3+R 1381 -421 120 23 1 cs_invvn01c_sl cs_invvn01c_sl 69 N1730 ---->{e}
                     R C3+R 1381 -421 120 23 1 cs_nnd2n02c_sl
F C3+R 1313 -421 79
F C3+R 1313 -421 79 88 5 cs_invvn01c_sl cs_invvn01c_sl 0 N1652 ---->
                    R C3+R 1260 -421 120 30 1 cs_invvn01c_sl
C2464/a
cs invvn01c_sl 53 N1749
                          R C3+R 1260 -421 120 30 1 cs_nnd3n02c_sl
---->{f} C2412/y
                                          F C3+R 1210 -421 55
cs nnd3n02c sl 0 N1749 ---> C2412/a
F C3+R 1210 -421 55 27 1 cs_invvn01c_sl cs_invvn01c_sl 0 N1713 ----> C1954/a R C3+R 1171 -421 175 47 2 cs_invvn01c_sl
cs_invvn01c_sl 39 br_wrong_targ ----> br_wrong_targ
-421 175 47 2 Pl 0 br_wrong_targ
                                 R C3+R 1349 -420 123 1078 7
----- 3 dcd succ last
              0 dcd_succ_last_t1 RAT
                       R C3+R 1349 -420 123 1078 7 cs_invvn01c_sl
0 ----> C2744/y
cs_invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                F C3+R 1282
-420 85 305 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
F C3+R 1282 -420 85 305 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
```

```
C2738/b
                               R C3+R
                                         1230
                                              -420
                                                      120 1261 4 cs nnd2n02c sl
cs nnd2n02c sl
                52 N1098 ---->
                                                               R C3+R
                               C2734rwr/y
                                                                         1230 -420
120 1261 4 cs_invvn01c_sl
                                                0 N1098 ----> C2734rwr/a
                                cs invvn01c sl
                                                     cs_invvn01c_sl 59 N1097 ---->
FC3+R
         1171
               -420
                           306 1 cs_invvn01c sl
C2728rwr/y
                                FC3+R
                                         1171
                                                -420
                                                       59 306 1 cs_invvn01c_sl
    1135 -420
                 101
                      165 2 cs_invvn01c sl
                                                cs_invvn01c_sl 36 N1692 ---->{b}
C2725rwr/v
                               R C3+R
                                         1135
                                               -420
                                                     101 165 2 cs_nnd2n02c_sl
                0 N1692 ---->
cs_nnd2n02c_sl
                              C2725rwr/a
                                                               FC3+R
                                                                         1081 -420
                                                                                      93
157 2 cs nnd2n02c sl
                           cs nnd2n02c sl
                                           54 N1479 ---->{c} C2721rwr/y
FC3+R
         1081
               -420
                          157 2 cs_nnd3n02c_sl
                       93
                                                      cs nnd3n02c sl
                                                                       0 N1479 ---->
C2721rwr/a
                                R C3+R
                                          1015 -420 214 120 2 cs_nnd3n02c_sl
cs nnd3n02c_sl
                66 N1497 ---->{d} C2709rwr/y
                                                                RC3+R
                                                                          1015 -420
214 120 2 cs_nor3n03c_sl
                               cs_nor3n03c_sl
                                                0 N1497 ---> C2709rwr/a
          920 -420
FC3+R
                      59
                           51 1 cs nor3n03c sl
                                                    cs_nor3n03c_sl 95 N1986 ---->{e}
C2677rwr 0/v
                                FC3+R
                                           920
                                                -420
                                                      59 51 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl
                0 N1986 ---->
                              C2677rwr 0/b
                                                                RC3+R
                                                                          887 -420
90 97 2 cs_nnd2n02c sl
                              cs_nnd2n02c_sl 33 N1094 ---->{f} C2909/y
        . 887
R<sub>C3+R</sub>
              -420
                      90
                          97 2 cs_nnd2n02c_sl
                                                     cs_nnd2n02c_sl
                                                                      0 N1094 ---->
C2909/b
                              FC3+R
                                         835 -420
                                                     80 90 1 cs_nnd2n02c sl
cs_nnd2n02c_sl
                52 dcd_mcr41_blk ---->
                                      dcd mcr41 blk
                                                                        FC3+R
                                                                                   835
      80 90 1 PI
                                      0 dcd_mcr41_blk
```

violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet du ju store status(2):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit\_455 | Net eu\_iu\_srlz\_op\_encode(11):a has transition violation\_1.099, multiplier\_1 RISE:\_\_\_\_1 transition 500, limit 455; FALL: transition 500, limit 455 INet dcd\_succ\_last\_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -433.9 INet frc\_blk\_1cyc\_q:l2\_out\_n has cap violation 1.008, load 248.9, limit 247, multiplier 1 slack -203.8 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 614.9 INet N26:y has cap violation 1.216, load 1218, 1 slack 381.3 INet N36:y has cap violation 1.179, load 1180, limit 1001. limit 1001, multiplier 1 slack 616.2 INet N1098:y has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -433.9 INet gbfonet\_2:y has cap violation 1.218, load 1219, limit 1001, multiplier 1 slack 27.29 INet gbfonet 15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 349.9 INet gbfonet\_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 478 IDesign IDCDSUC has 13 violations > reset\_timing\_area > report\_drc Checking DRC for IDesign IDCDSUC INet clkg:clkg has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1.134e+38 INet du\_iu\_store\_status(2):a has transition violation 1.099, multiplier 1 RISE: transition 1):a has transition violation 1.099, multiplier 1 RISE: transition 500, limit 455; FALL: transition 500, limit 455 INet dcd\_succ\_last\_t1:y has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -433.9 INet frc\_blk\_1cyc\_q:l2\_out\_n has cap violation\_1.008, load\_248.9, limit\_\_247, multiplier 1 slack -203.8 INet N22:y has cap violation 1.204, load 1205, limit 1001, multiplier INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier 1 slack 381.3 INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 616.2 INet N1098:y has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -433.9 INet gbfonet\_2:y has cap violation 1.218, load 1219, limit 1001, multiplier 1 slack 27.29 INet gbfonet\_15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 349.9 INet gbfonet\_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 478 IDesign IDCDSUC has 13 violations > gbfo fancorr -check -use\_max\_load -aggressive -enforce\_p... [GB-103]: noninverting buffers are absent Fanout Corr Area: before 4434.25 after 4434.25 (0.00 %) Slack: before -433.9434 after -433.9434 (0.00 %) Cell: before 787 after 787 (0.00 %) Time: 4.680000 > gbfo\_tune\_gain -target\_frac 0.98 -gain\_incr 0.05 -gain\_d... C2906 new rep load 66.5 greater than max 64.9: set to max: FREEZE SIZEUP C2721rwr new rep load 62.36 greater than max 61.93: set to max: FREEZE SIZEUP C2734rwr

```
new rep load 307.3 greater than max 300.2: set to max: FREEZE SIZEUP C2738 new rep load 99.28
greater than max 96.3: set to max: FREEZE SIZEUP C2709rwr new rep load 43.14 greater than max
42.11: set to max: FREEZE SIZEUP Tune Gain
                                            Area: before 4434.25 after 4385.96 (1.09 %)
Slack: before -433.9434 after -433.0000 (0.22 %)
                                            Cell: before 787 after 787 (0.00 %)
                                             > report_gain_violations -min 1.0 -max 10.0
                   > attribute_gain -to
------ Gain Violation Report for design IDCDSUC
                                                                   Cell Name
----- Type
                                            Gain
                                            10.230905
                                                       C2194
                                                                   cs invvn01c_sl Min
                                                                   cs_invvn01c_sl Max
                                                       C2895
                                            10.629883
0.777985
           C2894
                      cs nnd2n02c_sl Max
                                                                   cs nnd2n02c_sl Max
                                            0.963504
                                                        C2911
           C2907
                      cs invvn01c sl Min
13.073235
                                            0.681414
                                                        C2677rwr_0 cs_nnd2n02c_sl
                      cs_nor2n02c_sl Min
12.189666 C2918
Slack: before -1475.6755
                                 Cell: before 722 after 722 (0.00 %)
                                                                   Time: 0.750000 resize
after -1475.6755 (0.00 %)
                                            Slack : before -1475.6755 after -1475.6755 (0.00 %)
Area: before 2731.15 after 2731.15 (0.00 %)
                                 Time: 1.520000 resize Area: before 5081.39 after 5081.39
Cell: before 722 after 722 (0.00 %)
           (0.00\%)
                                 Area: before 5441.99 after 5359.17 (1.52 %)
                                                                              Slack: before
Time: 1.750000 tgfs rewiring
                                 Cell: before 763 after 762 (0.13 %)
                                                                   Time: 20.260000 tgfs
-603.6691 after -543.6871 (9.94 %)
                                                        Slack: before -513.2166 after -506.3137
           Area: before 5133.28 after 5092.88 (0.79%)
                                            Time: 13.960000 Assign Gain
                                                                              Area: before
           Cell: before 775 after 773 (0.26 %)
(1.35\%)
                                 Slack: before -506.3137 after -812.2559 (-60.43 %)
5092.88 after 4486.86 (11.90 %)
                                                                   Area: before 4486.86 after
                                 Time: 2.590000 Fanout Corr
Cell: before 773 after 773 (0.00 %)
                      4502.64 (-0.35 %)
                                            Area: before 4502.64 after 4352.61 (3.33 %)
           Time: 4.870000 Tune Gain
(-1.81 %)
Slack : before -812.2559 after -680.5689 (16.21 %) Cell : before 787 after 787 (0.00 %)
                                                                   Slack: before -680.5689
                      Area: before 4352.61 after 4474.51 (-2.80%)
46.970000 Tune Gain
                                                        Area: before 4474.51 after 4474.51
                      Time: 20.930000 resize
787 (0.00 %)
           (0.00\%)
                                                                   Slack: before -446.0240
                      Area: before 4474.51 after 4475.36 (-0.02 %)
Time: 1.780000 swap
                                                       Time: 2.560000 tgfs rewiring
after -441.6489 (0.98 %) Cell: before 787 after 787 (0.00 %)
                                            Slack: before -441.6489 after -441.6489 (0.00 %)
Area: before 4475.36 after 4531.42 (-1.25 %)
                                 Time: 14.330000 Tune Gain
                                                                   Area: before 4531.42 after
Cell: before 787 after 787 (0.00 %)
                       Slack : before -441.6489 after -433.9434 (1.74 %) Cell : before 787 after 787
4432.62 (2.18 %)
                                             Area : before 4432.62 after 4434.25 (-0.04 %)
           Time: 12.060000 tafs rewiring
Slack : before -433.9434 after -433.9434 (0.00 %) Cell : before 787 after 787 (0.00 %)
10.200000 Fanout Corr Area: before 4434.25 after 4434.25 (0.00 %)
                                                                   Slack: before -433.9434
after -433.9434 (0.00 %) Cell: before 787 after 787 (0.00 %)
                                                        Time: 4.680000 Tune Gain
                                             Slack: before -433.9434 after -433.0000 (0.22 %)
Area: before 4434.25 after 4385.96 (1.09%)
                                  Time: 11.630000 CDS Effectiveness Report:
                                                                               Trafo
Cell: before 787 after 787 (0.00 %)
                                                                               #time:
                                                                   #calls
                                             SIDeg
                       Tot SI
SI/call
                                                                   tafs rewiring 16.721207
                                                        91.59
                      374,880829 0.000000
                                             4
Tune Gain
           93.720207
                                                                               0.000000
                                                        4.375061
                                                                   4.375061
                                  58.75
                                             swap
           0.000000
                       4
66.884827
                                                                               Stretch Area
                                  0.000000
                                             0.000000
           Legalization 0.000000
2.56
                                                        Apportion FO-
                                                                               0:000000
                       0.000000
           0.000000
                                  0
                                             0
0.000000
                                                                   0.000000
                                                                               -305.942200 1
                                             Assign Gain 0.000000
                                  0
           0.000000
                       0
0.000000
                                                                               Beta Assign
                                             0.000000
                                                        2
                                                                   9.55
           Fanout Corr 0.000000
                                  0.000000
2.59
                                                                               0.000000
                       0.000000
                                  0
                                                        Stretch Delay
           0.000000
0.000000
                                                                   0.000000
                                                                               0.000000
                                  0
                                             Strect Mincut
0.000000
           0.000000
                       0
                                                                   0.000000
                                                                                          0
                                             0.000000
                                                        0.000000
                                                                               0
0.000000
           0
                       0
                                  fantom
                                                                   fantomless
                                                                               0.000000
           0.000000
                       0.000000
                                  0.000000
                                             0
                                                        0
Buffering
                                                        0.000000
                                                                   0.000000
                                                                               0.000000
                                                                                          0
                                             spitless
0.000000
           0.000000
                                                                   0
                                                                               pmove
                                  0.000000
                                             0.000000
                                                        0
                       0.000000
            bmove
                                                                   0.000000
                                                                               0.000000
                                                        resize
                                             O
            0.000000
                       0.000000
                                  0
0.000000
                                                                   0.000000
                                                                                          0
                                             0.000000
                                                        0.000000
                                                                               0
0.000000
                       5.8
                                  bftm
                                                                               0.000000
                                                                    phase
                                  0.000000
                                             0
                                                        0
 spltp
            0.000000
                       0.000000
```

```
0.000000
            0.000000
                       0
                                                > cds_acc -runtime -no_full CDS Effectiveness
Report:
            Trafo
                                   SI/call
                                                           Tot SI
                                                                                  SIDea
#calls
            #time:
                       Tune Gain
                                   93.720207
                                               374.880829 0.000000
                                                                      4
                                                                                  91.59
tafs rewiring 16.721207
                       66.884827
                                   0.000000
                                               4
                                                           58.75
                                                                      Fanout Corr 0.000000
0.000000
            0.000000
                       2
                                   9.55
                                               resize
                                                           0.000000
                                                                      0.000000
                                                                                  0.000000
                                                                                              4
5.8
            Assign Gain 0.000000
                                   0.000000
                                               -305.942200 1
                                                                      2.59
                                                                                  swap
4.375061
            4.375061
                       0.000000
                                               2.56
                                                           Legalization 0.000000
                                   1
                                                                                  0.000000
0.000000
            0
                                               0.000000
                                                          0.000000
                                   Buffering
                                                                      0.000000
                       O
                                                                                  0
                                                                                              0
Beta Assign 0.000000
                       0.000000
                                   0.000000
                                               0
                                                                      Stretch Delay
0.000000
            0.000000
                       0.000000
                                               0
                                   0
                                                           Strect Mincut
                                                                                  0.000000
0.000000
            0.000000
                                   0
                                               fantom
                                                           0.000000
                                                                      0.000000
                                                                                  0.000000
                                                                                              0
            Stretch Area 0.000000
                                   0.000000
                                               0.000000
                                                                      0
                                                                                  fantomiess
                       0.000000
0.000000
            0.000000
                                                           spltless
                                   0
                                               0
                                                                      0.000000
                                                                                  0.000000
0.000000
                                   bmove
                                               0.000000
            0
                       0
                                                          0.000000
                                                                      0.000000
                                                                                              0
pmove
            0.000000
                       0.000000
                                   0.000000
                                               0
                                                          0
                                                                      Apportion FO
0.000000
            0.000000
                       0.000000
                                   0
                                               0
                                                          bftm
                                                                      0.000000
                                                                                  0.000000
0.000000
                                   spltp
                                               0.000000
                                                          0.000000
                                                                      0.000000
                                                                                  O
                                                                                              0
            0.000000
                       0.000000
phase
                                   0.000000
                                               0
                                                          O
                                                                       > echo {Custom Synzilla
Report  Custom Synzilla Report
                                        > ps -cell Design /HISVHDL/IDCDSUC has:
                                                                                  1 instances 0
upcells
            122 IN ports 73 OUT ports
                                               787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786
LINKED; 0 UNLINKED; 0 DC)
                                               1008 nets (0 multiply-driven; 0 undriven)
                                   0 buses
2632 pins (0 inversions) 2.61 pins per net
                                               1551 literals 21 levels
                                                                      10 max fanin
15 max fanout
                       Cell Information
                                                          FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area
                     0)
                                               PSEUDO_REG
                                                               (ncount 83 : area
cb clk 32 1 (ncount
                       6: area
                                 480)
                                                          cb_mode_block (ncount
                                                                                   1: area
70)
                       cs_ao12n03c_sl (ncount
                                                6: area
cs_ao22n03c_sl (ncount
                       16: area 96)
                                                          cs_invvn01c_sl (ncount 229 : area
458)
                       cs_nnd2n02c_sl (ncount 206 : area
                                                           618)
ount 31: area
                                   cs_nnd4n03c_sl (ncount
                                                           7: area
                                                                      35)
cs_nor2n02c_sl (ncount
                       13 : area
                                   39)
                                                          cs_nor3n03c_sl (ncount
                                                                                  2: area
                       cs_oa21n03c_sl (ncount
8)
                                                3: area
                                                          15)
                                                          cs_xbn2n01b_sl (ncount
cs_oa22n03c_sl (ncount
                        1: area
                                   6)
                                                                                   1: area
                       cs_xbo2n01b_sl (ncount
                                                1 : area
                                                           8)
                                                                                  Total Area =
1989 (Comb = 1439 : Non-Comb = 550)
                                                > write_end_point_report -points 2
[ET-0018]:>Begin...New EndPoint Report
                                            for file /tmp/end_point_report..147522.
[ET-0019]:<End.....New Endpoint Report.
                                           Sun Apr 18 21:57:21 1999 Part : IDCDSUC Mode : Late
Mode / Nominal
                           EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Fri
Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                      Max. Slack: 1.13427E+38 Sort Field: Slack
Max. Endpoints: 2 Cause of Slack
                                           Abbreviation Comparison/Description -----
                          Slack Continuation
                                                  SlkCont
                                                             Slack due to a point downstream on
path Required Arrival Time
                               RAT
                                         ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
Required Arrival Time AssrtRAT
                                ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                   ClkGSet
                              ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                                   ClkGHld
                                                              ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                              CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                                        Setup
( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                                                        Hold
( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
           ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST )
EndOfC
ClockPulseWidth
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        CIkPW
TRAILING EDGE ) ClockSeparation
                                           ClkSep
                                                      ( CLOCK1 ARRIVAL TIME + CLOCK
SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
                                                                        ALTest
ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting
ATLimit
           Slack discontinuity due to failed test
                                              Num/
LimitedAT/
                                            Delay/ Failed Test/
                                                               Test PinName
```

```
FC3+R 1312 -433 81 1078 7
----- 1 dcd_succ_last
                                                             879
               0 dcd_succ_last_t1 RAT
                           F C3+R 1312 -433 81 1078 7 cs_invvn01c_sl
0 ----> C2744/y
cs invvn01c_sl 0 dcd_succ_last_t1 ----> C2744/a
                                                    R C3+R 1258
-433 121 304 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a} C2738/y
R C3+R 1258 -433 121 304 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
                     F C3+R 1190 -433 79 1260 4 cs_nnd2n02c_sl
C2738/b
    d2n02c_sl 68 N1098 ----> C2734rwr/y F C3+R 1190 -433
R C3+R 1143 -433 86 306 1 cs_invvn01c_sl cs_invvn01c_sl 47
----> C2728rwr/y R C3+R 1143 -433 86 306 1
cs_nnd2n02c_sl 68 N1098 ----> C2734rwr/y
N1097 ----> C2728rwr/y
cs_invvn01c_sl cs_invvn01c_sl 0 N1097 ----> C2728rwr/a
     C2725rwr/y
R C3+R 1053 -433
134 157 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y
R C3+R 1053 -433 134 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
                 F C3+R 978 -433 64 109 2 cs_nnd3n02c_sl
C2721rwr/c
cs nnd3n02c sl 74 N892 ---->{d} C2338/y
                                              FC3+R 978 -433 64
R C3+R 943 -433 81 126 3 cs_invvn01c_sl
C2905/v
F C3+R 903 -433
C3+R 903 -433 80 73 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcd_blk_dsucc
R C3+R 868 -433 80 73 1 cs_nor2n02c_sl cs_nor2n02c_sl 35 dcc ----> dcd_blk_dsucc R C3+R 868 -433 80 73 1 PI
0 dcd blk dsucc
0 dcd_succ_last_t1 RAT
R C3+R 12F
                                        R C3+R 1353 -424 123 1078 7
----- 2 dcd_succ_last
                                                            929
                           R C3+R 1353 -424 123 1078 7 cs_invvn01c_sl
0 ----> C2744/v
-424 85 304 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
F C3+R 1286 -424 85 304 4 cs_nnd2n02c_sl cs_nnd2n02c_sl 0 N675 ---->
C2738/b R C3+R 1234 -424 120 1260 4 cs_nnd2n02c_sl
cs nnd2n02c sl 52 N1098 ---> C2734rwr/y
                                               R C3+R 1234 -424
F C3+R 1175 -424 58 306 1 cs_invvn01c_sl cs_invvn01c_sl 59 N1097 ---->
                 F C3+R 1175 -424 58 306 1 cs_invvn01c_sl
C2728rwr/v
R C3+R 1140 -424 101
C3+R 1086 -424 93 157 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 54 N1479 ---->{c}
                        F C3+R 1086 -424 93 157 2 cs_nnd3n02c_sl
C2721rwr/y
R C3+R
                                                       1020 -424
204 111 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 65 N1497 ---->{d} C2709rwr/y
R C3+R 1020 -424 204 111 2 cs_nor3n03c_sl cs_nor3n03c_sl 0 N1497 ---->
                       F C3+R 905 -424 115 50 1 cs_nor3n03c_sl
C2709rwr/c
cs_nor3n03c_sl 115 N1976 ---->{e} C2579rwr_0_0/y F C3+R 905 -424
115 50 1 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1976 ----> C2579rwr_0_0/c
R C3+R 834 -424 162 39 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 71 N1719 ---->{f}
               R C3+R 834 -424 162 39 2 cs_nor2n02c_sl
C2599rwr_0_0_0/y
cs_nor2n02c_sl 0 N1719 ----> C2599rwr_0_0_0/a F C3+R 754 -424
```

```
72 22 1 cs_nor2n02c_sl
                              cs_nor2n02c_sl 80 N1942 ---->{g} C2349rwr_0_0 0 0 0/v
FC3+R
          754 -424
                           22 1 cs_nnd2n02c_sl
                                                    72
C2349rwr_0_0_0_0_0/a
                                     R C3+R
                                               712 -424
                                                           99 20 1 cs_nnd2n02c sl
cs_nnd2n02c_sl 42 N288 ---->{h} C2339/y
                                                             R C3+R
                                                                       712 -424
20 1 cs nnd2n02c sl
                          cs_nnd2n02c_sl 0 N288 ---> C2339/a
C3+R
         665 -424
                         20 1 cs_nnd2n02c sl
                                                   cs_nnd2n02c_sl 46 NET690 ---->{i}
C2187/v
                              FC3+R
                                        665 -424
                                                    65 20 1 cs_nnd2n02c_sl
cs_nnd2n02c_sl
                0 NET690 ----> C2187/a
                                                              R C3+R
                                                                                    78
39 2 cs_nnd2n02c_sl
                         cs_nnd2n02c_sl 35 N29 ----> C2020/v
                                                                                    R
C3+R
        630 -424
                     78
                         39 2 cs_invvn01c sl
                                                  FC3+R
          557 -424
                     424 40 1 cs_invvn01c_sl
                                                    cs_invvn01c_sl 73 du_iu_hold_aa_req
57 -424 424 40 1 Pl
----> du_iu_hold_aa_reg
                                        FC3+R
                                                  557 -424
0 du_iu_hold_aa_req
                          > cputime Used 40.74 cpu seconds or 00:00:41 wall time, used 0 bytes or 0
1283.882935
            > echo {=== CDS process finished === Good names for
byte.
IDCDSUC
                          Count
                                   User Transform
                                                      New For all nets
                                                                               1008
556
             452 For all nets
        0
                                      1008
                                             55.16%
                                                       0.00%
                                                               44.84% For I/O port nets
179
      71.51%
                0.00%
                        28.49% For register output nets
                                                        166
                                                              100.00%
                                                                         0.00%
0.00%
                                User Transform
                       Count
                                                   New For all boxes
290
        22
              475 For all boxes
                                        787 36.85%
                                                        2.80%
                                                                60.36% For register boxes
     0.00% For linked boxes
                                   786
                                         36.90%
                                                   2.80%
                                                           60.31%
                                                                           > echo
{Custom Synzilla Report} Custom Synzilla Report
                                                  > ps -cell Design /HISVHDL/IDCDSUC has:
1 instances 0 upcells
                     122 IN ports 73 OUT ports
                                                      787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI;
786 LINKED; 0 UNLINKED; 0 DC)
                                           1008 nets (0 multiply-driven; 0 undriven)
                                0 buses
2632 pins (0 inversions) 2.61 pins per net
                                           1551 literals 21 levels
                                                                10 max fanin
15 max fanout
                     Cell Information
                                                      FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area
                   0)
                                           PSEUDO_REG (ncount 83: area
cb_clk_32_1 (ncount
                     6: area 480)
                                                      cb_mode_block (ncount
                                                                             1: area
                     cs_ao12n03c_sl (ncount
                                            6: area
cs_ao22n03c_sl (ncount 16 : area
                                 96)
                                                      cs_invvn01c_sl (ncount 229 : area
             cs_nnd2n02c_sl (ncount 206 : area
                                                      618)
cs_nnd3n02c_sl (ncount 31: area 124)
                                                      cs_nnd4n03c sl (ncount
                                                                             7: area
                     cs_nor2n02c_sl (ncount
                                           13 : area
cs_nor3n03c_sl (ncount
                     2 : area
                                                      cs_oa21n03c_sl (ncount
                                                                            3: area
                     cs_oa22n03c_sl (ncount
                                           1: area
cs_xbn2n01b_sl (ncount 1: area
                                8)
                                                      cs_xbo2n01b_sl (ncount
                                                                            1: area
                     Total Area = 1989 (Comb = 1439 : Non-Comb = 550)
write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
                                                                    for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
                                                                  Sun Apr 18 21:57:23
1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                      EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38 Sort Field: Slack
                                                  Max. Endpoints: 2 Cause of Slack
Abbreviation Comparison/Description ------
                                                   ----- Slack
Continuation
                 SIkCont
                           Slack due to a point downstream on path Required Arrival Time
         ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating
          ClkGHld
                     ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
+ ADJUST ) Clock Tree Pulse Width
                                   CIKTPW
                                              ( CLOCK LEADING EDGE + PULSE WIDTH <
CLOCK TRAILING EDGE ) Setup
                                          Setup
                                                    ( DATA ARRIVAL TIME + SETUP <
CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                  Hold
                                                           ( DATA ARRIVAL TIME - HOLD
> CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                       EndOfC
                                                                  ( DATA ARRIVAL TIME
+ CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
                                                                 ClkPW
                                                                            (CLOCK
```

```
( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) LOOP
      ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
Arrival Time Limiting ATLimit Slack discontinuity due to failed test
                         Delay/ Failed Test/ Test PinName
LimitedAT/
E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName
F C3+R 1312 -433 81 1078 7
----- 1 dcd_succ_last
                    0 ----> C2744/y
                                            F C3+R
                                                  1312
                      cs_invvn01c_sl 0 dcd_succ_last_t1 ---> C2744/a
-433 81 1078 7 cs_invvn01c_sl
R C3+R 1258 -433 121 304 4 cs_invvn01c_sl cs_invvn01c_sl 54 N675 ---->{a}
                  R C3+R 1258 -433 121 304 4 cs_nnd2n02c_sl
C2738/v
F C3+R
                                           1190 -433
1190 -433 79 1260 4 cs_invvn01c_sl cs_invvn01c_sl 0 N1098 ---->
                         1143 -433 86 306 1 cs_invvn01c_sl
                   R C3+R
C2734rwr/a
cs invvn01c_sl 47 N1097 ----> C2728rwr/y
                                      R C3+R 1143 -433
                                                     86
1099 -433 71 171 2 cs_invvn01c_sl cs_invvn01c_sl 44 N1692 ---->{b}
                   F C3+R 1099 -433 71 171 2 cs_nnd2n02c_sl
C2725rwr/y
R C3+R
                                            1053 -433
134 157 2 cs_nnd2n02c_sl cs_nnd2n02c_sl 46 N1479 ---->{c} C2721rwr/y
R C3+R 1053 -433 134 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl
                                           0 N1479 ---->
                   F C3+R 978 -433 64 109 2 cs_nnd3n02c_sl
C2721rwr/c
                                      F C3+R 978 -433 64
cs nnd3n02c_sl 74 N892 ---->{d} C2338/y
R C3+R
                  R C3+R 943 -433 81 126 3 cs_invvn01c_sl
C2905/y
F C3+R 903 -433 68
----> dcd_blk_dsucc R C3+R 868 -433 80 73 1 Pl 0 dcd_blk_dsucc
______
                           R C3+R 1353 -424 123 1078 7
            2 dcd succ last
             0 dcd_succ_last_t1 RAT
                                                  929
PO
                      R C3+R 1353 -424 123 1078 7 cs_invvn01c_sl
0 ----> C2744/v
                                           F C3+R 1286
cs invvn01c sl 0 dcd_succ_last_t1 ---> C2744/a
-424 85 304 4 cs_invvn01c_sl cs_invvn01c_sl 67 N675 ---->{a} C2738/y
                       R C3+R 1234 -424 120 1260 4
 0 N675 ----> C2738/b
R
    C3+R
C2734rwr/a
cs_invvn01c_sl 59 N1097 ----> C2728rwr/y
                                      F C3+R 1175 -424
                                                     58
R C3+R
C2725rwr/v
cs nnd2n02c sl 0 N1692 ----> C2725rwr/a
                                       FC3+R 1086 -424
                                                     93
157 2 cs nnd2n02c sl cs nnd2n02c_sl 54 N1479 ---->{c} C2721rwr/y
     1086 -424 93 157 2 cs_nnd3n02c_sl cs_nnd3n02c_sl 0 N1479 ---->
F C3+R
                   R C3+R 1020 -424 204 111 2 cs_nnd3n02c_sl
C2721rwr/a
cs_nnd3n02c_sl 65 N1497 ---->{d} C2709rwr/y
                                       R C3+R
                                              1020 -424
F C3+R 905 -424 115 50 1 cs_nor3n03c_sl cs_nor3n03c_sl 115 N1976 ---->{e}
```

LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation

```
C2579rwr_0_0/y
                                   FC3+R
                                              905 -424
                                                          115
                                                                50 1 cs_nnd3n02c sl
 cs_nnd3n02c_sl
                  0 N1976 ----> C2579rwr_0_0/c
                                                                   R C3+R
                                                                              834 -424
      39 2 cs_nnd3n02c_sl
                                 cs_nnd3n02c_si 71 N1719 ---->{f} C2599rwr_0_0 0/y
 R C3+R
           834 -424 162
                             39 2 cs nor2n02c sl
                                                       cs_nor2n02c_sl
                                                                        0 N1719 ---->
C2599rwr 0 0 0/a
                                     FC3+R
                                               754 -424
                                                           72 22 1 cs_nor2n02c_sl
                80 N1942 ---->{g} C2349rwr_0_0_0_0_0/y
cs_nor2n02c_st
                                                                       FC3+R
                                                                                  754
                                                                                       -424
72 22 1 cs_nnd2n02c_sl
                                cs_nnd2n02c_sl 0 N1942 ---> C2349rwr_0_0_0_0 0/a
R C3+R
           712 -424
                        99
                            20 1 cs_nnd2n02c_sl
                                                       cs_nnd2n02c_sl 42 N288 ---->{h}
C2339/y
                                R C3+R
                                           712 -424
                                                            20 1 cs nnd2n02c sl
                                                       99
cs_nnd2n02c_sl
                  0 N288 ----> C2339/a
                                                               FC3+R
                                                                         665 -424
                                                                                      65
20 1 cs_nnd2n02c_si
                           cs_nnd2n02c_sl 46 NET690 ---->{i} C2187/y
FC3+R
                            20 1 cs_nnd2n02c sl
           665 -424
                       65
                                                       cs_nnd2n02c_sl
                                                                        0 NET690 ---->
C2187/a
                                R C3+R
                                           630 -424
                                                            39 2 cs_nnd2n02c_sl
                                                       78
cs_nnd2n02c_sl 35 N29 ---->
                              C2020/v
                                                              R C3+R
                                                                         630 -424
                                                                                     78
39 2 cs_invvn01c sl
                          cs_invvn01c_sl
                                          0 N29 ---->
                                                       C2020/a
                     424 40 1 cs_invvn01c_sl
C3+R
         557 -424
                                                     cs_invvn01c_sl 73 du_iu_hold_aa_req
----> du_iu_hold_aa_req
                                          FC3+R
                                                    557 -424 424 40 1 PI
0 du_iu_hold_aa_req
IDCDSUC - Area: 4385.956543, Area(Weight): 1283.882935
                                                               > cputime Used 2.05 cpu
seconds or 00:00:02 wall time, used 0 bytes or 0 byte.
                                                       > echo {=== Discretization process ===}
=== Discretization process ===
                                    > time_units -nano
                                                             > time_units -nano
cds_discrete -no_slew_violation
                                      > echo {Custom Synzilla Report} Custom Synzilla Report
> ps -cell Design /HISVHDL/IDCDSUC has:
                                             1 instances 0 upcells
                                                                  122 IN ports 73 OUT ports
787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC)
                                                                    0 buses
                                                                               1008 nets (0
multiply-driven; 0 undriven)
                                  2632 pins (0 inversions) 2.61 pins per net
                                                                               1551 literals
21 levels
                                  15 max fanout
           10 max fanin
                                                        Cell Information
FUNC_STRAIGHT_WIRE_DESIGN (ncount 180 : area 0)
                                                                    PSEUDO_REG
                                                                                    (ncount
83 : area
           0)
                                  cb_clk_32_1 (ncount
                                                        6: area 480)
cb_mode_block (ncount 1: area
                                  70)
                                                        cs_ao12n03c (ncount
                                                                               6: area
24)
                       cs_ao22n03c (ncount 15: area
                                                        90)
                                                                               cs ao22n10c
(ncount 1: area
                                             cs_invvn01c (ncount 130 : area
                   18)
                                                                             260)
cs_invvn02c (ncount
                      7: area
                                14)
                                                        cs_invvn04c (ncount 5: area
                                                                                         10)
           cs_invvn05c (ncount
                                13 : area
                                            26)
                                                                    cs_invvn06c (ncount
: area
        18)
                                  cs_invvn07c (ncount
                                                        9: area
                                                                  18)
cs_invvn08c (ncount 3: area
                                12)
                                                        cs_invvn09c (ncount 7: area
                                                                                         28)
           cs_invvn10c (ncount
                                 6: area
                                           24)
                                                                    cs_invvn11c (ncount
                                                                                         5
: area
        30)
                                  cs_invvn12c (ncount 21: area
                                                                  126)
cs_invvn13c
            (ncount 4: area
                                32)
                                                        cs_invvn14c (ncount 1: area
           cs_invvn15c (ncount
                                 4: area
                                           40)
                                                                    cs_invvn16c (ncount
: area
        42)
                                  cs_invvn18c (ncount
                                                        1: area
                                                                  20)
cs_invvn19c (ncount
                      1 : area
                                25)
                                                        cs_nnd2n02c (ncount 185: area
555)
                      cs_nnd2n03c (ncount 3: area
                                                        9) .....
                                                                               cs_nnd2n04c
(ncount 3: area
                   9)
                                 cs_nnd2n05c (ncount
                                                        3: area
                                                                  12)
cs_nnd2n06c (ncount
                       2: area
                                 8)
                                                        cs_nnd2n07c (ncount
                                                                               2: area
8)
                      cs_nnd2n11c (ncount
                                             1 : area
                                                                               cs nnd2n12c
(ncount 1: area
                   12)
                                             cs_nnd2n13c (ncount 4: area
                                                                              60)
cs_nnd2n14c (ncount
                       2 : area
                                 38)
                                                        cs_nnd3n02c (ncount 27: area
108)
                      cs_nnd3n05c (ncount
                                             1 : area
                                                        6)
                                                                               cs_nnd3n06c
(ncount 1: area
                   6)
                                 cs_nnd3n09c (ncount
                                                        1 : area
                                                                  12)
cs_nnd3n12c (ncount
                       1: area
                                 22)
                                                        cs_nnd4n03c (ncount
                                                                               6: area
30)
                      cs_nnd4n09c (ncount
                                             1: area
                                                       16)
                                                                               cs_nor2n02c
(ncount 10 : area
                   30)
                                             cs_nor2n04c (ncount 2: area
                                                                              6)
cs_nor2n12c (ncount
                      1: area
                                12)
                                                        cs_nor3n03c (ncount
                                                                               1: area
           cs_nor3n10c (ncount 1: area
                                           12)
                                                                   cs oa21n03c (ncount
```

```
cs_oa21n04c (ncount
                                                    1 : area
                                                              5)
1: area
                                                    cs oa22n03c (ncount 1: area
cs_oa21n05c (ncount 1: area
                               8)
                    cs_xbn2n01b (ncount 1: area
                                                                         cs_xbo2n01d
                                                    8)
                               Total Area = 2441 (Comb = 1891 : Non-Comb = 550)
                  8)
(ncount
       1 : area
> write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
                                                                 Sun Apr 18 21:57:29
1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                    EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                        Max. Endpoints: 2 Cause of Slack
Max. Slack: 1.13427E+38 Sort Field: Slack
Abbreviation Comparison/Description -----
                                                 ----- Slack
                          Slack due to a point downstream on path Required Arrival Time
                SlkCont
Continuation
EQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME <
                                                         ClkGSet
ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
                                                                    ( DATA ARRIVAL
TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating Hold
          ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST )
ClkGHld
                                  ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
Clock Tree Pulse Width
                       CIKTPW
                                   Setup
                                          ( DATA ARRIVAL TIME + SETUP < CLOCK
TRAILING EDGE ) Setup
                                                   ( DATA ARRIVAL TIME - HOLD >
ARRIVAL TIME + ADJUST ) Hold
                                          Hold
                                                    EndOfC
                                                              ( DATA ARRIVAL TIME +
CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                               ClkPW
                                                                         (CLOCK
CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation
                                                                            ClkSep
( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
          ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
ALTest
                               Slack discontinuity due to failed test
                     ATLimit
                                                               Num/
Arrival Time Limiting
                                       Delay/ Failed Test/ Test PinName
LimitedAT/
          AT Slack Slew CL FO Cell
                                               P Func T.Adj NetName
E Phase
                         .....
                   1 slow_mode_blk.reg_n.lat_0/BASE_REG/a
                                                               FC3+R
                                                                        1745 -424
                       05d cl_invvn05d 39 DELAY Setup
0 29 1 cl invvn
slow_mode_blk.reg_n.lat_0/BASE_REG/c1
                                          F C3-
                                                             60 238 14 cl_invvn
                                                   160
       1200 c1 ----> slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/OUT
                                                                    FC3+R
05d
                                        0 DELAY ---->
                               AND
-424
       0 29 1 AND
slow_mode_blk.reg_n.lat_0/DELAY_ELEMENT/IN1
                                                        1793 -424
                                                                    106 16 1 AND
                                              RC3+R
       -48 a ----> slow mode blk.reg_n.lat_0/a
                                                      R C3+R
                                                                1793 -424
                                                                            106 16
                                       0 a ---->{a} C2841/y
                       PSEUDO REG
                                                                              RC3+R
1 PSEUDO_REG
                                       02c cs_nnd2n02c 0 N95 ----> C2841/a
1793 -424 106 16 1 cs_nnd2n
                                                02c cs_nnd2n02c 53 N935 ---->{b}
         1740 -424 77 17 1 cs_nnd2n
FC3+R
                                                       17 1 cs_nnd2n
                                                                              02c
                             FC3+R
                                      1740 -424 77
C2821/v
                                                                              109
              0 N935 ---> C2821/b
                                                        R C3+R
                                                                 1694
                                                                       -424
cs nnd2n02c
                     02c cs_nnd2n02c 46 N512 ---->{c} C2798/y
17 1 cs_nnd2n
                                                                0 N512 ----> C2798/a
                                               02c cs_nnd2n02c
                    109 17 1 cs_nnd2n
       1694 -424
         1634 -424
                     103
                           35 2 cs_nnd2n
                                                 02c cs nnd2n02c 61 N1527 ---->
FC3+R
                             FC3+R
                                       1634 -424 103 35 2 cs_invvn
                                                                             01c
C2778/v
                                                        R C3+R
                                                                 1552 -424
                                                                              215
cs invvn01c
             0 N1527 ----> C2778/a
                    01c cs_invvn01c 82 N931 ---->{d} C2754/y
66 4 cs invvn
                                               03c cs_nnd2n03c
                                                                0 N931 ---> C2754/b
                    215 66 4 cs nnd2n
        1552 -424
C3+R
                                                03c cs_nnd2n03c 121 N1555 ---->
FC3+R
               -424
                      99 85 5 cs nnd2n
         1431
                    FC3+R
                              1431 -424
                                           99 85 5 cs invvn
                                                                    05c cs invvn05c
0 N1555 ----> C2588/a
                                           RC3+R
                                                     1366 -424
                                                                115
                                                                     24 1 cs invvn
                                                             R C3+R
                                                                      1366 -424
05c cs invvn05c 66 N1730 ---->{e} C2554/y
                                            0 N1730 ----> C2554/b
115 24 1 cs_nnd2n
                           03c cs_nnd2n03c
                                                03c cs_nnd2n03c 66 N1652 ---->
         1300 -424
                         87 5 cs_nnd2n
FC3+R
                      78
                             FC3+R
                                       1300 -424
                                                   78
                                                       87 5 cs_invvn
C2464/y
                                                        R C3+R 1248 -424 117
             0 N1652 ----> C2464/a
cs invvn07c
                                                                                 R
                    07c cs_invvn07c 52 N1749 ---->{f} C2412/y
31 1 cs invvn
```

```
FC3+R
        1202 -424
                   45 27 1 cs_nnd3n
                                        06c cs nnd3n06c
                                                     46 N1713 ---->
                         FC3+R
                                1202 -424
                                          45 27 1 cs_invvn
                                                               07c
 R C3+R
                                                      1171 -424 175
 49 2 cs_invvn 07c cs_invvn07c 31 br_wrong_targ ---> br_wrong_targ
       1171 -424 175 49 2 PI
                                            0 br_wrong_targ
                2 dcd succ last
                                           RC3+R
                                                   1351 -422
                                                             123 1078 7
 PO
                  0 dcd_succ_last_t1 RAT
                                                                929
 0 ----> C2744/v
                                      1351 -422 123 1078 7 cs invvn
                              R C3+R
 FC3+R
                                                                1285
      83 302 4 cs_invvn 18c cs_invvn18c 66 N675 ---->{a} C2738/y
 FC3+R
       1285 -422
                  83 302 4 cs nnd2n
                                        14c cs nnd2n14c
                                                      0 N675 ---->
 C2738/b
                         R C3+R
                                 1235 -422 118 1261 4 cs_nnd2n
                                                                  14c
 cs_nnd2n14c 50 N1098 ---> C2734rwr/y
                                                R C3+R
                                                        1235 -422
                                                                  118
                                 0 N1098 ----> C2734rwr/a
 1261 4 cs invvn
                 19c cs_invvn19c
 C3+R
       1178 -422
                 54 310 1 cs invvn
                                      19c cs_invvn19c 56 N1097 ---->
 C2728rwr/y
                          F C3+R 1178 -422 54 310 1 cs_invvn
                                                                 16c
           0 N1097 ----> C2728rwr/a
 cs_invvn16c
                                               R C3+R
                                                      1145 -422
                                                                 104
 181 2 cs_invvn 16c cs_invvn16c 33 N1692 ---->{b} C2725rwr/y
       1145 -422 104 181 2 cs nnd2n
                                      C2725rwr/a
                          FC3+R
                                 1090 -422 91 161 2 cs_nnd2n
                                                                 13c
 cs_nnd2n13c 56 N1479 ---->{c} C2721rwr/y
                                                FC3+R
                                                        1090
 161 2 cs_nnd3n 12c cs_nnd3n12c
                                 0 N1479
----> C2721rwr/a
                              R C3+R
                                      1025 -422
                                               199 115 2 cs_nnd3n
 12c cs_nnd3n12c 65 N1497 ---->{d} C2709rwr/y
                                                    R C3+R 1025 -422
 199 115 2 cs_nor3n 10c cs_nor3n10c 0 N1497 ---> C2709rwr/c
 F C3+R 912 -422 115 52 1 cs_nor3n
                                       10c cs_nor3n10c 113 N1976 ---->{e}
 C2579rwr_0_0/y
                           FC3+R
                                   912 -422 115 52 1 cs_nnd3n
                                                                  05c
 R C3+R
                                                          840 -422
                                                                   171
                 05c cs_nnd3n05c 72 N1719 ---->{f} C2599rwr_0_0_0/y
 40 2 cs_nnd3n
 RC3+R
         840 -422 171 40 2 cs_nor2n 04c cs_nor2n04c 0 N1719 ---->
                 F C3+R
 C2599rwr 0 0 0/b
                                    747 -422 109 21 1 cs_nor2n
                                                                   04c
 cs nor2n04c 93 N1956 ---->{g} C2440rwr/y
                                                FC3+R
                                                       747 -422
                                                                 109
 C3+R 679 -422 144 18 1 cs_nnd4n 03c cs_nnd4n03c 68 N283 ---->{h} C2318/y
 R C3+R
        679 -422 144 18 1 cs oa21n
                                        FC3+R
                                 598 -422 81 37 2 cs_oa21n
                                                                .04c
 cs_oa21n04c 81 three_branches ----> three_branches
                                                      F C3+R
                                                               598
 -422 81 37 2 PI 0 three_branches
```

06c cs\_nnd3n06c

0 N1749 ---> C2412/a

C3+R

1248 -424 117 31 1 cs\_nnd3n

1 RISE: transition 390, limit 290; FALL: transition 390, limit 290 INet violation 1.345, multiplier 1 RISE: transition 500, limit 290: du ju store\_status(2):a has transition violation 1.724, multiplier FALL: transition 500, limit 290 INet eu\_iu\_srlz\_op\_actn(0):a has transition violation 1.29, multiplier 1 RISE: transition 366, limit 290; FALL: transition 374, limit 290 INet eu\_iu\_srlz\_op\_actn(1):a has tion 341, limit 290 INet eu\_iu\_srlz\_op\_encode(0):a has transition violation 1.383, multiplier RISE: transition 401, limit 290; FALL: transition 401, limit 290 INet eu\_iu\_srlz\_op\_encode(1):a has transition violation 1.379, multiplier 1 RISE: transition 400, limit 290; FALL: transition 399, limit 290 INet eu\_iu\_srlz\_op\_encode(2):a has transition violation 1.448, multiplier transition 420, limit 290; FALL: transition 420, limit 290 INet eu\_iu\_srlz\_op\_encode(3):a has 1 RISE: transition 302, limit 290; FALL: transition 295, limit transition violation 1.041, multiplier 1 RISE: transition 406, 290 INet eu\_iu\_srlz\_op\_encode(4):a has transition violation 1.4, multiplier limit 290; FALL: transition 405, limit 290 INet eu\_iu\_srlz\_op\_encode(5):a has transition violation 1 RISE: transition 373, limit 290; FALL: transition 373, limit 290 INet 1.286, multiplier 1 RISE: transition eu ju srlz op encode(6):a has transition violation 1.221, multiplier 290; FALL: transition 336, limit 290 INet eu\_iu\_srlz\_op\_encode(7):a has transition violation 1.372, 1 RISE: transition 398, limit 290; FALL: transition 395, limit 290 INet 1 RISE: transition eu iu srlz\_op\_encode(8):a has transition violation 1.266, multiplier 290; FALL: transition 367, limit 290 INet eu\_iu\_srlz\_op\_encode(9):a has transition violation 1.114, 1 RISE: transition 323, limit 290; FALL: transition 319, limit 290 INet eu\_iu\_srlz\_op\_encode(11):a has transition violation 1.724, multiplier 1 RISE: transition 500, limit 290; FALL: transition 500, limit 290 INet dcd\_succ\_last\_t1:y has cap violation 1.077, load 1078, 1 slack -421.9 INet N22:y has cap violation 1.204, load 1205, limit 1001, limit 1001, multiplier 1 slack 611.4 INet N26:y has cap violation 1.216, load 1218, limit 1001, multiplier slack 377.5 INet N36:y has cap violation 1.179, load 1180, limit 1001, multiplier 1 slack 613.3 INet N1098:y has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -421.9 INet N2016:b 1 RISE: transition 296.8, limit 290; FALL: transition 142.2, has transition violation 1.023, multiplier limit 290 INet gbfonet\_2:y has cap violation 1.218, load 1219, limit 1001, multiplier 20.51 INet gbfonet\_15:y has cap violation 1.169, load 1170, limit 1001, multiplier 1 slack 354.5 INet gbfonet\_16:y has cap violation 1.108, load 1109, limit 1001, multiplier 1 slack 480 IDesign > resize -trace 0 -examine 10 -local IDCDSUC has 33 violations > cpr\_eval -mincut -inc -rank 1 ... INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1 slack -421.9 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.075, load 1 slack -421.8 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1076, limit 1001, multiplier 1 slack -422 INet N1555:b has transition violation 1.117. 1.079, load 1080, limit 1001, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:c has multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit transition violation 1.117, multiplier 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has ion 198.9. limit 290 INet N1555:c has transition violation 1.117, multiplier 1 RISE: transition 324. limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: Net N1555:b has transition violation 1.117, multiplier transition 198.9, limit 290 INet N1652:b has transition violation 1.138, multiplier 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit 290 INet N1652:b has transition violation 1.138, 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit 290 INet N1652:b has multiplier 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit transition violation 1.138, multiplier 1 RISE: transition 330, limit 290; FALL: 290 INet N1652:b has transition violation 1.138, multiplier transition 202.6, limit 290 INet N1652:b has transition violation 1.138, multiplier 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit 290 INet N1652:b has transition violation 1.138, 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit 290 INet N1652:b has multiplier 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit transition violation 1.138, multiplier 1 RISE: transition 330, limit 290; FALL: 290 INet N1652:b has transition violation 1.138, multiplier

transition 202.6, limit 290 INet N1652:b has transition violation 1.138, multiplier 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit 290 INet N1652:b has transition violation 1.138, 1 RISE: transition 330, limit 290; FALL: transition 202.6, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:c has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:c has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1555:b has transition violation 1.117, multiplier 1 RISE: transition 324, limit 290; FALL: transition 198.9, limit 290 INet N1692:b has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:a has transition violation 1.904. 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:b has multiplier transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:a has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290: ISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:a has transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:b has transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:a has transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:b has transition violation 1.189, 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:a has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:b has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:a has transition violation 1.189, multiplier 1 RISE:transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier 1\_RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 Net N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.97, 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has multiplier transition violation 1.51, multiplier 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51, multiplier 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51, multiplier 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51, 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.006, multiplier 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition violation 1.006, multiplier 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition violation 1.006, multiplier transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition violation 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet 1.006, multiplier

1 RISE: transition 664.4, limit 290; FALL: transition N1497:b has transition violation 2.291, multiplier 1 RISE: transition 664.4, limit 290; FALL: transition 240, as transition violation 2.291, multiplier 1 RISE: transition 664.4, limit limit 290 INet N1497:b has transition violation 2.291, multiplier 290; FALL: transition 240, limit 290 INet N1497:a has transition violation 2.291, multiplier transition 664.4, limit 290; FALL: transition 240, limit 290 INet N1497:b has transition violation 1 RISE: transition 514, limit 290; FALL: transition 189.8, limit 290 INet 1.773, multiplier 1 RISE: transition 514, limit 290; FALL: transition N1497:a has transition violation 1.773, multiplier 1 RISE: transition 514, limit 189.8, limit 290 INet N1497:b has transition violation 1.773, multiplier 290; FALL: transition 189.8, limit 290 INet N1497:a has transition violation 1.773, multiplier RISE: transition 514, limit 290; FALL: transition 189.8, limit 290 INet N1497:b has transition 1 RISE: transition 434.7, limit 290; FALL: transition 163.7, limit 290 violation 1.499, multiplier 1 RISE: transition 434.7, limit 290; FALL: INet N1497:a has transition violation 1.499, multiplier 1 RISE: transition transition 163.7, limit 290 INet N1497:b has transition violation 1.499, multiplier 434.7, limit 290; FALL: transition 163.7, limit 290 INet N1497:a has transition violation 1.499, 1 RISE: transition 434.7, limit 290; FALL: transition 163.7, limit 290 INet N1497:b has 1 RISE: transition 364.4, limit 290; FALL: transition 144, limit transition violation 1.256, multiplier 290 INet N1497:a has transition violation 1.256, multiplier 1 RISE: transition 364.4, limit 290; FALL: transition 144, limit 290 INet N1497:b has transition violation 1.256, multiplier transition 364.4, limit 290; FALL: transition 144, limit 290 INet N1497:a has transition violation 1 RISE: transition 364.4, limit 290; FALL: transition 144, limit 290 INet 1 RISE: transition 306.8, limit 290; FALL: transition N1497:b has transition violation 1.058, multiplier 128.2, limit 290 INet N1497:a has transition violation 1.058, multiplier 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit 290 INet N1497:b has transition violation 1.058, multiplier 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit 290 INet N1497:a has transition 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit 290 violation 1.058, multiplier INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 RISE: transition 742.7, limit 290; FALL: INet N675:a has transition violation 2.561, multiplier transition 510, limit 290 INet N675:a has transition violation 2.561, multiplier 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:b has transition violation 2.561, 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:a has 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit transition violation 2.561, multiplier 1 RISE: transition 742.7, limit 290; FALL: 290 INet N675:a has transition violation 2.561, multiplier transition 510, limit 290 INet N675:a has transition violation 2.561, multiplier 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:b has transition violation 2.561, 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:a has 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit transition violation 2.561, multiplier 290 INet N1098:dcd\_success has cap violation 1.175, load 1176, limit 1001, multiplier 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:a 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, has transition violation 1.978, multiplier 1 RISE: transition 573.7, limit 290; limit 290 INet N675:b has transition violation 1.978, multiplier FALL: transition 401.6, limit 290 INet N675:a has transition violation 1.978, multiplier transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:a has transition violation 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:a 1.978, multiplier 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, has transition violation 1.978, multiplier 1 RISE: transition 573.7, limit 290; limit 290 INet N675:b has transition violation 1.978, multiplier FALL: transition 401.6, limit 290 INet N675:a has transition violation 1.978, multiplier transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N1098:dcd\_success has cap 1 slack -216.3 INet N675:a has transition violation violation 1.178, load 1179, limit 1001, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a 1.608, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, has transition violation 1.608, multiplier 1 RISE: transition 466.3, limit 290; limit 290 INet N675:b has transition violation 1.608, multiplier FALL: transition 323.6, limit 290 INet N675:a has transition violation 1.608, multiplier transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a has transition violation 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, has transition violation 1.608, multiplier

limit 290 INet N675:b has transition violation 1.608, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a has transition violation 1.608, multiplier transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N1098:dcd\_success has cap violation 1.181, load 1182, limit 1001, multiplier 1 slack -216.4 INet N675:a has transition violation 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a 1.299, multiplier has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:b has transition violation 1.299, multiplier 1 RISE: transition 376.7. limit 290: FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, multiplier transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:b has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290: FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, multiplier transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N1098:dcd\_success has cap violation 1.185, load 1186, limit 1001, multiplier 1 slack -216.5 INet N675:a has transition violation 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a 1.03, multiplier has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:b has transition violation 1.03, multiplier 1 RISE: transition 298.7. limit on 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:b has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N1098:dcd\_success has cap violation 1.19, 1 slack -216.7 INet N1098:dcd\_success has cap violation 1.196, load 1191, limit 1001, multiplier load 1197, limit 1001, multiplier 1 slack -216.8 INet N1098:dcd\_success has cap violation 1.204, load: 1205, limit 1001, multiplier 1 slack -217.1 INet N1098:dcd\_success has cap violation 1.214, load: 1215, limit 1001, multiplier 1 slack -217.4 INet N1098:dcd\_success has cap violation 1.225, load: 1227, limit 1001, multiplier 1 slack -217.7 INet N1098:dcd\_success has cap violation 1.241, load 1242, limit 1001, multiplier 1 slack -218.1 INet N1098:dcd\_success has cap violation 1.26. load 1261, limit 1001, multiplier 1 slack -218.7 INet N1098:dcd\_success has cap violation 1.26. load: 1261, limit 1001, multiplier 1.slack -218.7 ...INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -518.9 INet N1098:dcd\_success has transition violation 1.774, multiplier 1 RISE: transition 807.2, limit 455; FALL: transition 494.8, limit 455 INet N1098:b has transition violation 2.784, multiplier 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:a has transition violation 2.784, multiplier 1 RISE: transition 807.2. limit 290; FALL: transition 494.8, limit 290 INet N1098:b has transition violation 2.784, multiplier 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -518.9 INet N1098:dcd\_success has transition violation 1.774, multiplier 1 RISE: transition 807.2, limit 455; FALL: transition 494.8, limit 455 INet N1098:b has transition violation 2.784, multiplier 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:a has transition violation 2.784, multiplier transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:b has transition violation 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet 2.784, multiplier N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -448.6 INet N1098:dcd\_success has transition violation 1.44, multiplier 1 RISE: transition 655, limit 455: FALL: transition 395.9, limit 455 INet N1098:b has transition violation 2.259, multiplier transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:a has transition violation 2.259, multiplier 1 RISE: transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:b has transition violation 2.259, multiplier 1 RISE: transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -448.6 INet N1098:dcd\_success has transition violation 1.44, multiplier 1 RISE: transition 655, limit 455; FALL: transition 395.9, limit 455 INet N1098:b has transition violation 2.259, :a has transition violation 2.259, multiplier 1 RISE: transition 655, limit 290; FALL: transition

1 RISE: transition 655, limit 395.9, limit 290 INet N1098:b has transition violation 2.259, multiplier 290; FALL: transition 395.9, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, 1 slack -408.9 INet N1098:dcd\_success has transition violation 1.139, limit 1001, multiplier 1 RISE: transition 518.2, limit 455; FALL: transition 321.8, limit 455 INet N1098:b has 1 RISE: transition 518.2, limit 290; FALL: transition 321.8, limit transition violation 1.787, multiplier 1 RISE: transition 518.2, limit 290; 290 INet N1098:a has transition violation 1.787, multiplier FALL: transition 321.8, limit 290 INet N1098:b has transition violation 1.787, multiplier transition 518.2, limit 290; FALL: transition 321.8, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -408.9 INet N1098:dcd\_success has 1 RISE: transition 518.2, limit 455; FALL: transition 321.8, limit transition violation 1.139, multiplier 1 RISE: transition 518.2, limit 290; 455 INet N1098:b has transition violation 1.787, multiplier FALL: transition 321.8, limit 290 INet N1098:a has transition violation 1.787, multiplier transition 518.2, limit 290; FALL: transition 321.8, limit 290 INet N1098:b has transition violation 1 RISE: transition 518.2, limit 290; FALL: transition 321.8, limit 290 INet 1.787, multiplier N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -341.5 INet 1 RISE: transition 417.9, limit 290; FALL: transition N1098:b has transition violation 1.441, multiplier 253.3, limit 290 INet N1098:a has transition violation 1.441, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 INet N1098:b has transition violation 1.441, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 INet N1098:dcd\_success has 1 slack -341.5 INet N1098:b has transition cap violation 1.26, load 1261, limit 1001, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 violation 1.441, multiplier 1 RISE: transition 417.9, limit 290; FALL: INet N1098:a has transition violation 1.441, multiplier transition 253.3, limit 290 INet N1098:b has transition violation 1.441, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 INet N1098:dcd\_success has cap violation 1.26, 1 slack -304.1 INet N1098:b has transition violation 1.153, load 1261, limit 1001, multiplier multiplier 1 RISE: transition 334.3, limit 290; FALL: transition 203.3, limit 290 INet N1098:a has 1 RISE: transition 334.3, limit 290; FALL: transition 203.3, limit transition violation 1.153, multiplier 1 RISE: transition 334.3, limit 290; 290 INet N1098:b has transition violation 1.153, multiplier FALL: transition 203.3, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1 slack -304.1 INet N1098:b has transition violation 1.153, multiplier 1001, multiplier transition 334.3, limit 290; FALL: transition 203.3, limit 290 INet N1098:a has transition violation 1 RISE: transition 334.3, limit 290; FALL: transition 203.3, limit 290 INet 1.153, multiplier 1 RISE: transition 334.3, limit 290; FALL: transition N1098:b has transition violation 1.153, multiplier 203.3, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -276.1 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1001, multiplier 1 slack -256.6 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1 slack -256.6 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -241.8 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -241.8 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -231.3 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -231.3 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -223.6 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -223.6 INet N1097:a has transition violation 1.339, multiplier 1 RISE: 1001, multiplier transition 388.3, limit 290; FALL: transition 237.4, limit 290 INet-N1097:a has transition violation 1 RISE: transition 388.3, limit 290; FALL: transition 237.4, limit 290 INet 1.339, multiplier 1 RISE: transition 313.9, limit 290; FALL: transition N1097:a has transition violation 1.082, multiplier 190.2, limit 290 INet N1097:a has transition violation 1.082, multiplier 1 RISE: transition 313.9, limit 290; FALL: transition 190.2, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1 slack -421.9 INet dcd\_succ\_last\_t1:dcd\_succ\_last has 1.077, load 1078, limit 1001, multiplier 1 slack -421.9 INet cap violation 1.077, load 1078, limit 1001, multiplier dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -747 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.881, multiplier 855.9, limit 455; FALL: transition 523.3, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290;

FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -747 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.881, multiplier 855.9, limit 455; FALL: transition 523.3, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet ion 1.077, load 1078, limit 1001, multiplier 1 slack -669.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.516, multiplier 1 RISE: transition 690, limit 455; FALL: transition 422.9, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -669.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.516, multiplier 1 RISE: transition 690, limit 455; FALL: transition 422.9, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 Net dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -608 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.231, multiplier transition 559.9, limit 455; FALL: transition 338.4, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9. limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -608 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.231, multiplier 1 RISE: transition 559.9, limit 455; FALL: transition 338.4, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, has transition violation 1.931, multiplier

290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, limit 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet multiplier dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1 slack -564 INet dcd\_succ\_last\_t1:a1 has transition violation 1.527, 1078, limit 1001, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet 1 RISE: transition 442.9, limit dcd\_succ\_last\_t1:b has transition violation 1.527, multiplier FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:b has 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit transition violation 1.527, multiplier 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack 1 RISE: transition 442.9, limit -564 INet dcd\_succ\_last\_t1:a1 has transition violation 1.527, multiplier 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.527, multiplier 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit transition violation 1.527, multiplier 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -514.6 INet dcd\_succ\_last\_t1:a1 has transition violation 1.232, multiplier 1 RISE: transition 357.2. limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier - 1 RISE: transition 357.2, limit 290;--FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.232, multiplier RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit transition violation 1.232, multiplier 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, 1 slack -514.6 INet dcd\_succ\_last\_t1:a1 has transition violation load 1078, limit 1001, multiplier tion 216.5. limit 290 INet dcd succ last\_t1:b has transition violation 1.232, multiplier transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has transition 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 violation 1.232, multiplier INet dcd succ last t1:b has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit transition violation 1.232, multiplier 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -482.5 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, 1 slack -482.5 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, multiplier 1 slack -461.5 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, limit 1001, multiplier 1 slack -461.5 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap load 1078, limit 1001, multiplier 1 slack -445.7 INet violation 1.077, load 1078, limit 1001, multiplier dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -445.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -433.9 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, 1 slack -433.9 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, 1 slack -426.3 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, limit 1001, multiplier load 1078, limit 1001, multiplier 1 slack -426.3 INet N1781:a has transition violation 1.002, 1 RISE: transition 290.7, limit 290; FALL: transition 217, limit 290 INet N1781:b has 1 RISE: transition 290.7, limit 290; FALL: transition 217, limit transition violation 1.002, multiplier

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290 INet N1781:a has transition violation 1.002, multiplier 1 RISE: transition 290.7, limit 290;
FALL: transition 217, limit 290 INet N1781:b has transition violation 1.002, multiplier
transition 290.7, limit 290; FALL: transition 217, limit 290 resize
                                                            Area: before 4516.00 after
4516.00 (0.00 %)
                    (0.00\%)
          Time: 5.610000
                                 > write_end_point_report -points 3 [ET-0018]:>Begin...New
EndPoint Report
                   for file /tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
Sun Apr 18 21:57:39 1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                                  EDA EinsTimer
EndPoint Report Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack:
-1.13427E+38
                     Max. Slack: 1.13427E+38 Sort Field: Slack
                                                                    Max.
Endpoints: 3 Cause of Slack
                                Abbreviation Comparison/Description ------
----- Slack Continuation
                                           SlkCont
                                                     Slack due to a point downstream on
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted
path Required Arrival Time
                          RAT
Required Arrival Time AssrtRAT
                          ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock
Gating Setup
                ClkGSet
                          ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST ) Clock Gating Hold
                                           ClkGHld
                                                     ( DATA ARRIVAL TIME - CLOCK
GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width
                                                                  CIKTPW
CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup
                                                                           Setup
+ SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold
                                                         Hold
                                                                 ( DATA ARRIVAL
TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                               EndOfC
                                                                         (DATA
ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
                                                                         ClkPW
( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation
         ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST
                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME
                   ALTest
FROM CLOCK + ADJUST ) Arrival Time Limiting
                                           ATLimit
                                                     Slack discontinuity due to failed test
                                LimitedAT/
                                                                      Delay/
Failed Test/ Test PinName
                                                     AT Slack Slew CL FO Cell
                                            E Phase
P Func T.Adj NetName
_____
PO
                    0 dcd_succ_last_t1 RAT
                                                                         929
0 ----> C2744/v
                       R C3+R 1345 -416 123 1078 7 cs invvn
18c cs invvn18c
               0 dcd_succ_last_t1 ---> C2744/a
                                                                FC3+R
                                                                         1279
-416 83 302 4 cs_invvn _____18c cs_invvn18c 66 N675 ---->{a} C2738/y
FC3+R
        1279 -416
                    83 302 4 cs_nnd2n
                                             C2738/b
                            R C3+R
                                    1228 -416 118 1261 4 cs_nnd2n
                                                                           14c
cs_nnd2n14c 50 N1098 ----> C2734rwr/y
                                                                1228 -416
                                                       R C3+R
                                                                           118
1261 4 cs_invvn
                   C3+R
       1172 --416 54 310 1 cs_invvn
                                           19c cs_invvn19c 56 N1097 ---->
C2728rwr/y
                                                 54 310 1 cs_invvn
                            FC3+R
                                     1172 -416
                                                                          16c
cs invvn16c
            0 N1097 ----> C2728rwr/a
                                                      RC3+R
                                                              1139 -416
                                                                          104
181 2 cs invvn
                    16c cs_invvn16c 33 N1692 ---->{b} C2725rwr/y
                                                                              R
       1139 -416
C3+R
                  104 181 2 cs nnd2n
                                            13c cs nnd2n13c
                                                             0 N1692 ---->
C2725rwr/a
                                     1083 -416 91 161 2 cs_nnd2n
                             FC3+R
                                                                           13c
cs_nnd2n13c 56 N1479 ---->{c} C2721rwr/y
                                                       FC3+R
                                                                1083 -416
                                                                            91
161 2 cs_nnd3n
                     12c cs_nnd3n12c
                                     0 N1479 ---> C2721rwr/a
        1019 -416
R C3+R
                    199 115 2 cs_nnd3n
                                              12c cs_nnd3n12c 65 N1497 ---->{d}
C2709rwr/v
                            R C3+R
                                     1019 -416 199 115 2 cs nor3n
                                                                           10c
cs nor3n10c
            0 N1497 ----> C2709rwr/c
                                                      FC3+R
                                                               907
                                                                          92
                    10c cs_nor3n10c 111 N1976 ---->{e} C2579rwr_0_0/y
52 1 cs_nor3n
FC3+R
         907
             -416
                    92 52 1 cs nnd3n
                                            07c cs_nnd3n07c
                                                             0 N1976 ---->
C2579rwr_0_0/c
                                                  189 47 2 cs_nnd3n
                              R C3+R
                                        849 -416
                                                                            07c
            RC3+R
                      849 -416 189 47 2 cs_nor2n
                                                          04c cs_nor2n04c
                                                                          0
N1719 ----> C2599rwr_0_0_0/b
                                          FC3+R
                                                   747 -416 109
                                                                   21 1 cs nor2n
FC3+R
                                                                    747 -416
109 21 1 cs_nnd4n
                         03c cs_nnd4n03c
                                         0 N1956 ----> C2440rwr/b
```

```
R C3+R 679 -416 144 18 1 cs_nnd4n 03c cs_nnd4n03c 68 N283 ---->{h}
                         R C3+R 679 -416 144 18 1 cs_oa21n 04c
C2318/v
                                                  FC3+R 598 -416 81 37
F C3+R 598 -416 81 37 2 Pl 0 three_branches
------ 2 dcd_succ_last F C3+R 1294 -415 79 1078 7
            0 dcd_succ_last_t1 RAT
F C3+R
                                                                     879
                             F C3+R 1294 -415 79 1078 7 cs_invvn
0 ----> C2744/v
R C3+R
                                                                     1241
-415 119 302 4 cs_invvn 18c cs_invvn18c 53 N675 ---->{a} C2738/y
R C3+R 1241 -415 119 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ----> C2738/b F C3+R 1175 -415 76 1261 4 cs_nnd2n 14c
                                                    F C3+R 1175 -415
cs nnd2n14c 66 N1098 ----> C2734rwr/y
1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a
C3+R 1130 -415 80 310 1 cs_invvn 19c cs_invvn19c 45 N1097 --->
                 R C3+R 1130 -415 80 310 1 cs_invvn
C2728rwr/v
F C3+R 1089 -415
R C3+R 1041 -415 132 161 2 cs_nnd2n
C2725rwr/a

      cs_nnd2n13c
      48 N1479 ---->{c} C2721rwr/y
      R C3+R
      1041 -415 132

      161 2 cs_nnd3n
      12c cs_nnd3n12c
      0 N1479 ----> C2721rwr/c
      F

      C3+R
      969 -415 60 113 2 cs_nnd3n
      12c cs_nnd3n12c
      72 N892 ---->{d} C2338/y

      F C3+R
      969 -415 60 113 2 cs_nnd2n
      13c cs_nnd2n13c
      0 N892 ----> C2338/a

      R C3+R
      937 -415 72 124 3 cs_nnd2n
      13c cs_nnd2n13c
      32 N1119 ---->

                          R C3+R 937 -415 72 124 3 cs_invvn 13c
13c cs_invvn13c 36 N2010 ---->{e} C2906/y F C3+R 901 -415 63 - 90 53 90 1 cs nor2n 102 ---->
C2905/v
cs invvn13c 0 N1119 ----> C2905/a
63 90 1 cs_nor2n 12c cs_nor2n12c 0 N2010 ---> C2906/a
R C3+R 868 -415 80 76 1 cs_nor2n 12c cs_nor2n12c 33 dcd_blk_dsucc ---> dcd_blk_dsucc R C3+R 868 -415 80 76 1 Pl
dcd blk dsucc
AND 0 DELAY ----> eu_dsbl_aftr.reg_n.lat_0/DELAY_ELEMENT/IN1 R C3+R 1769
-401 98 16 1 AND AND -48 a ----> eu_dsbl_aftr.reg_n.lat_0/a
R C3+R 1769 -401 98 16 1 PSEUDO_REG PSEUDO_REG 0 a ----> C2874/y
R C3+R 1769 -401 98 16 1 cs_invvn 01c cs_invvn01c 0 N145 ----> C2874/a
F C3+R 1718 -401 74 16 1 cs_invvn 01c cs_invvn01c 51 N1013 ---->{a}
                         F C3+R 1718 -401 74 16 1 cs_nnd2n 02c
R C3+R 1674 -401 109
C3+R 1674 -401 109 17 1 cs_nnd2n 02c cs_nnd2n02c 0 N522 ----> C2833/b F C3+R 1601 -401 124 234 14 cs_nnd2n 02c cs_nnd2n02c 73 N1290 ---->
                          F C3+R 1601 -401 124 234 14 cs_invvn 08c
C2800/v
cs invvn08c 0 N1290 ----> C2800/a
                                                  R C3+R 1510 -401 166
37 1 cs_invvn 08c cs_invvn08c 92 N1648 ---->{c} C2779/y
F C3+R 1403 -401 134 107 6 cs_invvn
                                              R C3+R 1315 -401 122
cs invvn04c 0 N1645 ----> C2646/a
```

```
04c cs_invvn04c 89 N1746 ---->{d} C2620/y
21 1 cs_invvn
C3+R
        1315
                           21 1 cs_nnd2n
              -401
                     122
                                                  02c cs_nnd2n02c
                                                                     0 N1746 ---->
                                                                                    C2620/b
FC3+R
          1232 -401
                       134
                             67 4 cs nnd2n
                                                    02c cs_nnd2n02c
                                                                      83 N1740 ---->
C2602/v
                               FC3+R
                                          1232 -401
                                                       134 67 4 cs_invvn
                                                                                   02c
cs invvn02c
                            C2602/a
              0 N1740 ---->
                                                            RC3+R
                                                                      1132
                                                                            -401
                                                                                    168
37 2 cs. invvn
                      02c cs_invvn02c 100 N905 ---->{e} C2546/y
                                                                                      R
        168
              37 2 cs_nnd2n
                                     02c cs_nnd2n02c
                                                        0 N905 ---->
                                                                     C2546/b
FC3+R
         1044 -401
                       68
                            17 1 cs_nnd2n
                                                   02c cs nnd2n02c
                                                                      88 N1647 ---->
C1928/v
                               FC3+R
                                         1044
                                                -401
                                                       68
                                                            17 1 cs_invvn
cs_invvn01c
             0 N1647 ---->
                            C1928/a
                                                            RC3+R
                                                                       988 -401
16 1 cs invvn
                      01c cs_invvn01c
                                       56 eu_iu_fxu_exc_cond ----> eu_iu_fxu_exc_cond
R C3+R
          988
                -401
                      390
                            16 1 PI
                                                        0 eu_iu_fxu_exc_cond
```

> resize -trace 0 -examine 10 -local -critical -inc -rank ... INet N1692:b has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:a has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:b has transition violation 1.904, multiplier RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:a has transition violation 1.904, multiplier 1 RISE: transition 552.3, limit 290; FALL: transition 381.9, limit 290 INet N1692:b has transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:a has transition violation 1.539, multiplier 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:b has transition violation 1.539, 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:a has multiplier transition violation 1.539, multiplier 1 RISE: transition 446.2, limit 290; FALL: transition 306.4, limit 290 INet N1692:b has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:a has transition violation 1.189, multiplier 1.RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:b has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1692:a has transition violation 1.189, multiplier 1 RISE: transition 344.7, limit 290; FALL: transition 241.3, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 2.428, multiplier 1 RISE: transition 704.1, limit 290; FALL: transition 513.2, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.97, multiplier 1 RISE: transition 571.4, limit 290; FALL: transition 414.1, limit 290 INet N1479:a has transition violation 1.51, multiplier 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51. ALL: transition 321.2, limit 290 INet N1479:a has transition violation 1.51, multiplier transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a has transition violation 1 RISE: transition 437.8, limit 290; FALL: transition 321.2, limit 290 INet N1479:a 1.51, multiplier has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, multiplier transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.23, multiplier 1 RISE: transition 356.6, limit 290; FALL: transition 259, limit 290 INet N1479:a has transition violation 1.006, multiplier 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition violation 1.006, multiplier 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition violation 1.006, multiplier RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 INet N1479:a has transition 1 RISE: transition 291.7, limit 290; FALL: transition 210.4, limit 290 violation 1.006, multiplier Net N1497:b has transition violation 2.291, multiplier 1 RISE: transition 664.4, limit 290; FALL:

transition 240, limit 290 INet N1497:a has transition violation 2.291, multiplier 664.4, limit 290; FALL: transition 240, limit 290 INet N1497:b has transition violation 2.291, 1 RISE: transition 664.4, limit 290; FALL: transition 240, limit 290 INet N1497:a has transition violation 2.291, multiplier 1 RISE: transition 664.4, limit 290; FALL: transition 240, limit 1 RISE: transition 514, limit 290; FALL: 290 INet N1497:b has transition violation 1.773, multiplier 1 RISE: transition transition 189.8, limit 290 INet N1497:a has transition violation 1.773, multiplier 514, limit 290; FALL: transition 189.8, limit 290 INet N1497:b has transition violation 1.773, 1 RISE: transition 514, limit 290; FALL: transition 189.8, limit 290 INet N1497:a has multiplier 1 RISE: transition 514, limit 290; FALL: transition 189.8, limit transition violation 1.773, multiplier 1 RISE: transition 434.7, limit 290; 290 INet N1497:b has transition violation 1.499, multiplier FALL: transition 163.7, limit 290 INet N1497:a has transition violation 1.499, multiplier transition 434.7, limit 290; FALL: transition 163.7, limit 290 INet N1497:b has transition violation 1 RISE: transition 434.7, limit 290; FALL: transition 163.7, limit 290 INet 1.499, multiplier 1 RISE: transition 434.7, limit 290; FALL: transition N1497:a has transition violation 1.499, multiplier 1 RISE: transition 364.4, 163.7, limit 290 INet N1497:b has transition violation 1.256, multiplier limit 290; FALL: transition 144, limit 290 INet N1497:a has transition violation 1.256, multiplier RISE: transition 364.4, limit 290; FALL: transition 144, limit 290 INet N1497:b has transition 1 RISE: transition 364.4, limit 290; FALL: transition 144, limit 290 violation 1.256, multiplier 1 RISE: transition 364.4, limit 290; FALL: INet N1497:a has transition violation 1.256, multiplier transition 144, limit 290 INet N1497:b has transition violation 1.058, multiplier 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit 290 INet N1497:a has transition violation 1.058, 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit 290 INet N1497:b has multiplier 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit 290 INet N1497:a has 1 RISE: transition 306.8, limit 290; FALL: transition 128.2, limit transition violation 1.058, multiplier 290 INet N1098:dcd success has cap violation 1.26, load 1261, limit 1001, multiplier 1 RISE: transition 742.7, limit 290; -212.4 Net N675:a has transition violation 2.561, multiplier FALL: transition 510, limit 290 INet N675:a has transition violation 2.561, multiplier transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:b has transition violation 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:a 2.561, multiplier 1 RISE: transition 742.7, limit 290; FALL: transition 510, has transition violation 2.561, multiplier 1 RISE: transition 742.7, limit 290; limit 290 INet N675:a has transition violation 2.561, multiplier FALL: transition 510, limit 290 INet N675:a has transition violation 2.561, multiplier transition 742.7, limit 290; FALL: transition 510, limit 290 INet N675:b has transition violation 1 RISE: transition 742.7, limit 290; FALL: transition 510, limit 290 Net N675:a 2.561, multiplier 1 RISE: transition 742.7, limit 290; FALL: transition 510, has transition violation 2.561, multiplier limit 290 INet N1098:dcd\_success has cap violation 1.175, load 1176, limit 1001, multiplier slack -209.9 INet N675:a has transition violation 1.978, multiplier 1 RISE: transition 573.7, limit 290: FALL: transition 401.6, limit 290 INet N675:a has transition violation 1.978, multiplier 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:b has transition violation 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:a 1.978, multiplier has transition violation 1.978, multiplier 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, 1 RISE: transition 573.7, limit 290; limit 290 INet N675:a has transition violation 1.978, multiplier FALL: transition 401.6, limit 290 INet N675:a has transition violation 1.978, multiplier transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:b has transition violation 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, limit 290 INet N675:a 1.978, multiplier 1 RISE: transition 573.7, limit 290; FALL: transition 401.6, has transition violation 1.978, multiplier limit 290 INet N1098:dcd\_success has cap violation 1.178, load 1179, limit 1001, multiplier slack -210 INet N675:a has transition violation 1.608, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a has transition violation 1.608, multiplier transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:b has transition violation 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a 1.608, multiplier has transition violation 1.608, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a has transition violation 1.608, multiplier 1 RISE: transition 466.3, limit FALL: transition 323.6, limit 290 INet N675:a has transition violation 1.608, multiplier transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:b has transition violation

1.608, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N675:a has transition violation 1.608, multiplier 1 RISE: transition 466.3, limit 290; FALL: transition 323.6, limit 290 INet N1098:dcd\_success has cap violation 1.181, load 1182, limit 1001, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit nsition violation 1.299, multiplier 290 INet N675:a has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:b has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:b has transition violation 1.299, multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N675:a has transition violation 1.299. multiplier 1 RISE: transition 376.7, limit 290; FALL: transition 259.3, limit 290 INet N1098:dcd\_success has cap violation 1.185, load 1186, limit 1001, multiplier 1 slack -210.2 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:b has transition violation 1.03, multiplier transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1.03, multiplier 1 RISE: transition 298.7, limit FALL: transition 206.7, limit 290 INet N675:b has transition violation 1.03, multiplier transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet N675:a has transition violation 1 RISE: transition 298.7, limit 290; FALL: transition 206.7, limit 290 INet 1.03, multiplier N1098:dcd\_success has cap violation 1.19, load 1191, limit 1001, multiplier 1 slack -210.4 INet N1098:dcd\_success has cap violation 1.196, load 1197, limit 1001, multiplier 1 slack -210.6 INet N1098:dcd\_success has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack -210.8 INet N1098:dcd\_success has cap violation 1.214, load 1215, limit 1001, multiplier 1 slack -211.1 TNet N1098:dcd\_success has cap violation 1.225, load 1227, limit 1001, multiplier 1 slack -211.4 INet N1098:dcd\_success has cap violation 1.241, load 1242, limit 1001, multiplier 1 slack -211.9 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -212.4 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -212.4 INet 1 slack -512.7 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier N1098:dcd\_success has transition violation 1.774, multiplier 1 RISE: transition 807.2, limit 455; FALL: transition 494.8, limit 455 INet N1098:b has transition violation 2.784, multiplier transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:a has transition violation 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet 2.784, multiplier N1098:b has transition violation 2.784, multiplier 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 RISE: transition 807.2, limit 455; FALL: transition 494.8, limit 455 INet N1098:b has 1 RISE: transition 807.2, limit 290; FALL: transition 494.8, limit transition violation 2.784, multiplier 290 INet N1098:a has transition violation 2.784, multiplier 1 RISE: transition 807.2, limit 290: FALL: transition 494.8, limit 290 INet N1098:b has transition violation 2.784, multiplier transition 807.2, limit 290; FALL: transition 494.8, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -442.3 INet N1098:dcd\_success has transition violation 1.44, multiplier 1 RISE: transition 655, limit 455; FALL: transition 395.9, limit 455 INet N1098:b has transition violation 2.259, multiplier 1 RISE: transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:a has transition violation 2.259, multiplier 1 RISE: transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:b has transition violation 2.259, multiplier 1 RISE: transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -442.3 INet N1098:dcd\_success has transition violation 1.44, multiplier 1 RISE: transition 655, limit 455; FALL: transition 395.9, limit 455 INet N1098:b has transition violation 2.259, multiplier transition 655, limit 290; FALL: transition 395.9, limit 290 INet N1098:a has transition violation 1 RISE: transition 655, limit 290; FALL: transition 395.9, limit 290 INet 2.259. multiplier

1 RISE: transition 655, limit 290; FALL: transition N1098:b has transition violation 2.259, multiplier 395.9, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -402.7 INet N1098:dcd\_success has transition violation 1.139, multiplier 1 RISE: transition 518.2, limit 455; FALL: transition 321.8, limit 455 INet N1098:b has transition violation 1.787, 1 RISE: transition 518.2, limit 290; FALL: transition 321.8, limit 290 INet N1098:a has 1 RISE: transition 518.2, limit 290; FALL: transition 321.8, limit transition violation 1.787, multiplier 290 INet N1098:b has transition violation 1.787, multiplier 1 RISE: transition 518.2, limit 290; FALL: transition 321.8, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1 slack -402.7 INet N1098:dcd\_success has transition violation 1.139, multiplier 1001, multiplier RISE: transition 518.2, limit 455; FALL: transition 321.8, limit 455 INet N1098:b has transition 1 RISE: transition 518.2, limit 290; FALL: transition 321.8, limit 290 violation 1.787, multiplier 1 RISE: transition 518.2, limit 290; FALL: INet N1098:a has transition violation 1.787, multiplier 1 RISE: transition transition 321.8, limit 290 INet N1098:b has transition violation 1.787, multiplier 518.2, limit 290; FALL: transition 321.8, limit 290 INet N1098:dcd\_success has cap violation 1.26, 1 slack -335.2 INet N1098:b has transition violation 1.441, load 1261, limit 1001, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 INet N1098:a has multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit transition violation 1.441, multiplier 290 INet N1098:b has transition violation 1.441, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1 slack -335.2 INet N1098:b has transition violation 1.441, multiplier 1001, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 ition violation 1.441, multiplier INet N1098:b has transition violation 1.441, multiplier 1 RISE: transition 417.9, limit 290; FALL: transition 253.3, limit 290 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, 1 slack -297.8 INet N1098:b has transition violation 1.153, multiplier 1 RISE: transition multiplier 334.3, limit 290, FALL: transition 203.3, limit 290 INet N1098:a has transition violation 1.153, 1 RISE: transition 334.3, limit 290; FALL: transition 203.3, limit 290 INet N1098:b has 1 RISE: transition 334.3, limit 290; FALL: transition 203.3, limit transition violation 1.153, multiplier 290 INet N1098.dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -297.8 INet N1098:b has transition violation 1.153, multiplier 1 RISE: transition 334.3, limit FALL: transition 203.3, limit 290 INet N1098:a has transition violation 1.153, multiplier transition 334.3, limit 290; FALL: transition 203.3, limit 290 INet N1098:b has transition violation 1 RISE: transition 334.3, limit 290; FALL: transition 203.3, limit 290 INet 1.153, multiplier N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -269.8 **INet** 1 slack -269.8 INet N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -250.3 **INet** 1261, limit 1001, multiplier 1 slack -250.3 **INet** N1098:dcd\_success has cap violation 1.26, load 1 slack -235.5 **INet** N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -235.5 **INet** N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -225.1 **INet** N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -225.1 **INet** N1098:dcd\_success has cap violation 1.26, load 1261, limit 1001, multiplier 1 slack -217.3 INet N1098:dcd success has cap violation 1.26, load 1 slack -217.3 INet 1261, limit 1001, multiplier N1097:a has transition violation 1.339, multiplier 1 RISE: transition 388.3, limit 290; FALL: transition 237.4, limit 290 INet N1097:a has transition violation 1.339, multiplier 1 RISE: transition 388:3, limit 290; FALL: transition 237.4, limit 290 INet N1097:a has transition violation 1.082, multiplier 1 RISE: transition 313.9, limit 290; FALL: transition 190.2, limit 290 INet N1097:a has transition 1 RISE: transition 313.9, limit 290; FALL: transition 190.2, limit 290 violation 1.082, multiplier INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier slack -415.6 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, 1 slack -415.6 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, 1 slack -740.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation limit 1001, multiplier 1 RISE: transition 855.9, limit 455; FALL: transition 523.3, limit 455 INet 1.881, multiplier dcd\_succ\_last\_t1:a1 has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has

transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9. limit 290: FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -740.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.881, multiplier 1 RISE: transition 855.9, limit 455; FALL: transition 523.3, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd succ last t1:a has transition violation 2.951, multiplier 1 RISE: transition 855.9, limit 290; FALL: transition 523.3, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -663.4 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.516, multiplier transition 690, limit 455; FALL: transition 422.9, limit 455 INet dcd\_succ\_last\_t1:a1 has transition 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 violation 2.379, multiplier INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -663.4 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.516, multiplier 1 RISE: transition 690, limit 455; FALL: transition 422.9, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 2.379, multiplier 1 RISE: transition 690, limit 290; FALL: transition 422.9, limit 290 INet 1 slack -601.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.231, multiplier 1 RISE: transition 559.9, limit 455; FALL: transition 338.4, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -601.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has transition violation 1.231, multiplier transition 559.9, limit 455; FALL: transition 338.4, limit 455 INet dcd\_succ\_last\_t1:a1 has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290: FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit

290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.931, multiplier 1 RISE: transition 559.9, limit 290; FALL: transition 338.4, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -557.7 INet dcd\_succ\_last\_t1:a1 has transition violation 1.527, multiplier 1 RISE: transition 442.9. limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.527, 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.527, multiplier RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit transition violation 1.527, multiplier 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, 1 slack -557.7 INet dcd\_succ\_last\_t1:a1 has transition violation load 1078, limit 1001, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet 1.527, multiplier dcd\_succ\_last\_t1:b has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:b has 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.527, multiplier 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1 RISE: transition 442.9, limit 290; FALL: transition 275, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -508.3 INet dcd\_succ\_last\_t1:a1 has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.232, 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:b has transition violation 1.232, multiplier RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit transition violation 1.232, multiplier 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, 1 slack -508.3 INet dcd\_succ\_last\_t1:a1 has transition violation load 1078, limit 1001, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet 1.232, multiplier dcd\_succ\_last\_t1:b has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:b has 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:a has transition violation 1.232, multiplier 1 RISE: transition 357.2, limit 290; FALL: transition 216.5, limit 290 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -476.2 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -476.2 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, 1 slack -455.3 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load --1078, multiplier 1 slack -455.3 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, limit 1001, multiplier 1 slack -439.5 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap load 1078, limit 1001, multiplier violation 1.077, load 1078, limit 1001, multiplier 1 slack -439.5 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier -427.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, multiplier 1 slack -427.7 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, limit 1001, 1 slack -420.1 INet dcd\_succ\_last\_t1:dcd\_succ\_last has cap violation 1.077, load 1078, Area: before 4516.00 after 4516.00 (0.00 %) 1 slack -420.1 resize limit 1001, multiplier Time: > echo {In resize loop} In resize loop > echo > cpr\_eval 2.950000 > echo -415.62286377 -415.62286377 -404.222419168 -404.222419168

```
md:a has transition violation 1.214, multiplier
                                               1 RISE: transition 352, limit 290; FALL: transition
346, limit 290 INet eu_iu_mmode:a has transition violation 1.124, multiplier
                                                                               1 RISE: transition
326, limit 290; FALL: transition 326, limit 290 INet du_iu_hold_aa_req:a has transition violation
                   1 RISE: transition 424, limit 290; FALL: transition 424, limit 290 INet
1.462, multiplier
eu_iu_fpu_end_op:a has transition violation 1.169, multiplier
                                                              1 RISE: transition 339, limit 290;
FALL: transition 338, limit 290 INet eu_iu_misc_hold:c has transition violation 1.145, multiplier
                 332, limit 290; FALL: transition 310, limit 290 INet clkg:clkg has cap violation
RISE: transition
1.032, load 145.5, limit 141, multiplier
                                          1 slack 1.134e+38 INet du_iu_quiesced:a has transition
violation 1.166, multiplier
                            1 RISE: transition 338, limit 290; FALL: transition 338, limit 290 INet
iq_empty:iq_empty has cap violation 1.019, load 143.6, limit 141, multiplier
                                                                             1 slack -383.8 INet
clkg2:clkg2 has cap violation 1.032, load 145.5, limit 141, multiplier 1 slack 1.134e+38 INet
eu_iu_fxu_exc_cond:a has transition violation 1.345, multiplier
                                                               1 RISE: transition 390, limit 290;
FALL: transition 390, limit 290 INet du_iu_store_status(2):a has transition violation 1.724, multiplier
1 RISE: transition 500, limit 290; FALL: transition 500, limit 290 INet eu_iu_srlz_op_actn(0):a has
transition violation 1.29, multiplier
                                    1 RISE: transition 366, limit 290; FALL: transition 374, limit
290 lNet eu_iu_srlz_op_actn(1):a has transition violation 1.176, multiplier
                                                                           1 RISE: transition 341.
limit 290; FALL: transition 341, limit 290 INet eu_iu_srlz_op_encode(0):a has transition violation
1.383, multiplier
                   1 RISE: transition 401, limit 290; FALL: transition 401, limit 290 INet
eu_iu_srlz_op_encode(1):a has transition violation 1.379, multiplier
                                                                    1 RISE: transition 400. limit
290; FALL: transition 399, limit 290 INet eu_iu_srlz_op_encode(2):a has transition violation 1.448,
            1 RISE: transition 420, limit 290; FALL: transition 420, limit 290 INet
eu_iu_srlz_op_encode(3):a has transition violation 1.041, multiplier
                                                                  1 RISE: transition
290; FALL: transition 295, limit 290 INet eu_iu_srlz_op_encode(4):a has transition violation 1.4,
            1 RISE: transition 406, limit 290; FALL: transition 405, limit 290 INet
eu_iu_srlz_op_encode(5):a has transition violation 1.286, multiplier
                                                                    1 RISE: transition 373, limit
290; FALL: transition 373, limit 290 INet eu_iu_srlz_op_encode(6):a has transition violation 1.221,
multiplier 1 RISE: transition 354, limit 290; FALL: transition 336, limit 290 INet
eu_iu_srlz_op_encode(7):a has transition violation 1.372, multiplier
                                                                    1 RISE: transition
290; FALL: transition 395, limit 290 INet eu_iu_srlz_op_encode(8):a has transition violation 1.266,
multiplier
            1 RISE: transition 367, limit 290; FALL: transition 367, limit 290 INet
eu_iu_srlz_op_encode(9):a has transition violation 1.114, multiplier
                                                                   1 RISE: transition 323, limit
290; FALL: transition 319, limit 290 INet eu_iu_srlz_op_encode(11):a has transition violation 1.724.
multiplier 1 RISE: transition 500, limit 290; FALL: transition 500, limit 290 INet
dcd succ last_t1:v has cap violation 1.077, load 1078, limit 1001, multiplier
                                                                              1 slack -415.6 INet
N22:y has cap violation 1.204, load 1205, limit 1001, multiplier 1 slack 611.4 INet N26:y has cap
violation 1.216, load 1218, limit 1001, multiplier
                                                  1 slack 377.5 INet N36:y has cap violation 1.179,
load 1180, limit 1001, multiplier
                                   1 slack 613.3 INet N1098:y has cap violation 1.26, load 1261,
      1 slack -415.6 INet N2016:b has transition violation 1.023, multiplier
                                                                            1 RISE: transition 296.8.
limit 290; FALL: transition 142.2, limit 290 INet obfonet_2:y has cap violation 1.218, load 1219.
limit 1001, multiplier
                        1 slack 20.51 INet gbfonet_15:y has cap violation 1.169, load 1170, limit
                  1 slack 354.5 INet gbfonet_16:y has cap violation 1.108, load 1109, limit 1001,
1001, multiplier
multiplier
            1 slack 480 IDesign IDCDSUC has 33 violations
                                                                       > echo {Custom Synzilla
Report  Custom Synzilla Report
                                         > ps -cell Design /HISVHDL/IDCDSUC has:
                                                                                       1 instances 0
            122 IN ports 73 OUT ports
upcells
                                                  787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786
LINKED; 0 UNLINKED; 0 DC)
                                     0 buses
                                                  1008 nets (0 multiply-driven; 0 undriven)
2632 pins (0 inversions) 2.61 pins per net
                                                  1551 literals 21 levels
                                                                          10 max fanin
15 max fanout
                         Cell Information
                                                              FUNC_STRAIGHT_WIRE_DESIGN
(ncount 180 : area
                      0)
                                                                  (ncount 83 : area
                                                  PSEUDO_REG
                                                                                          0)
cb_clk_32_1 (ncount
                        6: area
                                   480)
                                                              cb_mode_block (ncount
                                                                                         1: area
                         cs_ao12n03c (ncount
                                                  6: area
                                                             24)
                                                                                       cs ao22n03c
(ncount 15 : area
                     90)
                                                  cs_ao22n10c (ncount
                                                                           1: area
                                                                                      18)
cs_invvn01c (ncount 129; area
                                   258)
                                                              cs_invvn02c (ncount
                                                                                      7: area
                                                                                                  14)
            cs_invvn04c (ncount
                                               10)
                                    5 : area
                                                                           cs_invvn05c (ncount 13
         26)
                                     cs_invvn06c (ncount
                                                             9: area
                                                                         18)
cs_invvn07c (ncount 10: area
                                   20)
                                                              cs_invvn08c (ncount
                                                                                      3: area
                                                                                                  12)
```

```
cs invvn10c (ncount
           cs_invvn09c (ncount
                                7 : area
                                         28)
                                cs_invvn11c (ncount
                                                               30)
                                                      5 : area
       24)
: area
                                                      cs_invvn13c (ncount 4: area
cs_invvn12c (ncount 21: area
                               126)
                                                                 cs invvn15c (ncount
           cs invvn14c (ncount
                                1 : area
                                          8)
                                 cs_invvn16c (ncount
                                                      3 : area
                                                                42)
cs_invvn18c (ncount 1: area
                                                      cs invvn19c (ncount
                                                                            1 : area
                                                                                      25)
                               20)
          cs_nnd2n02c (ncount 185: area 555)
                                                                 cs_nnd2n03c (ncount
                                cs nnd2n04c (ncount
                                                       3: area
3: area
                                                      cs_nnd2n06c (ncount
                                                                             1: area
                     3 : area
                                12)
cs_nnd2n05c (ncount
                                                                            cs_nnd2n11c
                     cs_nnd2n07c (ncount
                                            3: area
                                           cs_nnd2n12c (ncount 1: area
                                                                           12)
(ncount 1: area
                  11)
                                                                            2: area
                                                      cs nnd2n14c (ncount
                                60)
cs nnd2n13c (ncount
                      4: area
                                                                            cs_nnd3n07c
                                                      108)
                                           27 : area
38)
                     cs_nnd3n02c (ncount
                                           cs_nnd3n09c (ncount 1: area
                                                                            12)
(ncount 2: area
                  12)
                                                      cs_nnd4n03c (ncount
                                                                             6: area
cs_nnd3n12c (ncount
                                22)
                     1 : area
                                                                            cs_nor2n02c
                     cs_nnd4n09c (ncount
                                            1 : area
30)
                                           cs_nor2n04c
                  30)
                                                        (ncount 2: area
                                                                            6)
(ncount 10 : area
                               12)
                                                       cs nor3n03c (ncount
                                                                            1 : area
cs nor2n12c (ncount
                     1: area
                                                                  cs_oa21n03c (ncount
                                1 : area
                                         12)
          cs_nor3n10c (ncount
                                 cs_oa21n04c (ncount
                                                       1: area
                                                                 5)
1 : area
          5)
                                                       cs_oa22n03c (ncount
                                                                            1 : area
cs_oa21n05c (ncount
                                8)
                      1: area
                     cs_xbn2n01b (ncount 1: area
                                                                             cs_xbo2n01d
                                                      8)
6)
                                 Total Area = 2441 (Comb = 1891 : Non-Comb = 550)
                   8)
(ncount 1 : area
> write end point report -points 2 [ET-0018]:>Begin...New EndPoint Report
                                                                       for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
                                                                    Sun Apr 18 21:57:44
1999 Part : IDCDSUC Mode : Late Mode / Nominal
                                                       EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                    Max. Endpoints: 2 Cause of Slack
Max. Slack: 1.13427E+38 Sort Field: Slack
                                                    ------ Slack
Abbreviation Comparison/Description ------
 Slack due to a point downstream on path Required Arrival Time
                                                             RAT
                                                                      ( ARRIVAL TIME <
REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME <
ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
                                                           ClkGSet (DATA ARRIVAL
TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating Hold
          ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST )
ClkGHld
                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        CIKTPW
Clock Tree Pulse Width
                                             (DATA ARRIVAL TIME + SETUP < CLOCK
TRAILING EDGE ) Setup
                                    Setup
                                                   ( DATA ARRIVAL TIME - HOLD >
ARRIVAL TIME + ADJUST ) Hold
                                            Hold
                                                                 ( DATA ARRIVAL TIME +
CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle
                                                      EndOfC
                                                                            (CLOCK
                                                                 ClkPW
CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation
                                                                               ClkSep
( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop
          ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST )
                                Slack discontinuity due to failed test
Arrival Time Limiting
                      ATLimit
                                                                  Num/
                                         Delay/ Failed Test/ Test PinName-
LimitedAT/
          AT Slack Slew CL FO Cell
                                                 P Func T.Adj NetName
E Phase
                                                                1345 -416
                                                                             123 1078 7
                                                      R C3+R
                    1 dcd_succ_last
                                                                                 929
PO
                       0 dcd succ last_t1 RAT
                                                1345 -416 123 1078 7 cs_invvn
                                      R C3+R
0 ----> C2744/v
                                                                       FC3+R
                                                                                 1279
                 0 dcd_succ_last_t1 ---> C2744/a
18c cs invvn18c
                                  18c cs_invvn18c 66 N675 ---->{a} C2738/y
       83 302 4 cs invvn
                       83 302 4 cs_nnd2n
                                                   14c cs nnd2n14c
                                                                   0 N675 ---->
          1279 -416
F C3+R
                               R C3+R
                                         1228 -416 118 1261 4 cs_nnd2n
                                                                                   14c
C2738/b
cs nnd2n14c 50 N1098 ----> C2734rwr/y
                                                             R C3+R
                                                                       1228
                                                                            -416
                                                                                  118
                       19c cs_invvn19c
                                         0 N1098 ----> C2734rwr/a
1261 4 cs_invvn
```

```
C3+R 1172 -416 54 310 1 cs_invvn 19c cs_invvn19c 56 N1097 --->
C2728rwr/v
         F C3+R 1172 -416 54 310 1 cs_invvn
R C3+R 1139 -416 104
C3+R 1139 -416 104 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 --->
C2725rwr/a
                     F C3+R 1083 -416 91 161 2 cs_nnd2n
cs_nnd2n13c 56 N1479 ---->{c} C2721rwr/y F C3+
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ----> C2721rwr/a
                                          FC3+R 1083 -416 91
R C3+R 1019 -416 199 115 2 cs_nnd3n 12c cs_nnd3n12c 65 N1497 ---->{d}
          R C3+R 1019 -416 199 115 2 cs_nor3n 10c cs_nor3n10c 0
N1497 ----> C2709rwr/c
                       F C3+R 907 -416 92 52 1 cs_nor3n
10c cs_nor3n10c 111 N1976 ---->{e} C2579rwr_0_0/y
                                      F C3+R 907 -416
FC3+R 747 -416 109
C2440rwr/b R C3+R 679 -416 144 18 1 cs_nnd4n 03c cs_nnd4n03c 68 N283 ---->{h} C2318/y R C3+R 679 -416 144 18 1 cs_oa21n 04c cs_oa21n04c 0 N283 ----> C2318/a1 F
three_branches F C3+R 598 -416 81 37 2 PI 0
three_branches
-415 119 302 4 cs_invvn 18c cs_invvn18c 53 N675 ---->{a} C2738/y
R C3+R 1241 -415 119 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 --->
                   F C3+R 1175 -415 76 1261 4 cs_nnd2n 14c
C2734rwr/y F C3+R 1175 -415 76
cs_nnd2n14c 66 N1098 ----> C2734rwr/y F C3+ 1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a
                                         F C3+R 1175 -415 76
C3+R 1130 -415 80 310 1 cs_invvn 19c cs_invvn19c 45 N1097 ---->
C2728rwr/y
                    R C3+R 1130 -415 80 310 1 cs_invvn
                                                       16c
F C3+R 1089 -415 72
C3+R 1089 -415 72 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ---->
C2725rwr/a
                    R C3+R 1041 -415 132 161 2 cs_nnd2n
cs_nnd2n13c 48 N1479 ---->{c} C2721rwr/y
                                    R C3+R 1041 -415 132
161 2 cs_nnd3n 12c cs_nnd3n12c 0 N1479 ---> C2721rwr/c
    12c cs_nnd3n12c 72 N892 ---->{d} C2338/y
                                                F C3+R 969
-415 60 113 2 cs_nnd2n 13c cs_nnd2n13c 0 N892 ----> C2338/a
R C3+R 937 -415 72 124 3 cs_nnd2n 13c cs_nnd2n13c 32 N1119 --->
C2905/v
                     R C3+R 937 -415 72 124 3 cs_invvn 13c
FC3+R 901 -415 63 90
1 cs_invvn 13c cs_invvn13c 36 N2010 ---->{e} C2906/y
901 -415 63 90 1 cs_nor2n 12c cs_nor2n12c 0 N2010 ----> C2906/a
dcd_blk_dsucc
               > report_area    Design: /IDCDSUC - Area: 4516.000000, Area(Weight):
```

2441.000000 > cputime Used 14.14 cpu seconds or 00:00:15 wall time, used 0 bytes or 0

```
> echo. {=== Discretization process finished ===} === Discretization process finished ===
                                                     User Transform
                                                                         New For all nets
                                           Count
Good names for IDCDSUC
                                                                             44.84% For I/O
         556
                 0
                       452 For all nets
                                                  1008
                                                         55.16%
                                                                    0.00%
1008
                                   0.00%
                                                                               166
                                                                                    100.00%
                                            31.28% For register output nets
                  195
                        68.72%
port nets
                                           User Transform
                                                                 New For all boxes
                                   Count
0.00%
         0.00%
                       475 For all boxes
                                                  787
                                                                    2.80%
                                                                             60.36% For
                                                         36.85%
                22
787
       290
                                                 0.00% For linked boxes
register boxes
                                       0.00%
                      83
                           100.00%
                                     > echo {Custom Synzilla Report} Custom Synzilla Report
          2.80%
                   60.31%
36.90%
                                              1 instances 0 upcells
                                                                      122 IN ports 73 OUT ports
> ps -cell Design /HISVHDL/IDCDSUC has:
                                                                      0 buses
                                                                                  1008 nets (0
787 cells (1 AND; 0 XOR; 0 SEQ; 0 TRI; 786 LINKED; 0 UNLINKED; 0 DC)
                                                                                  1551 literals
                                   2632 pins (0 inversions) 2.61 pins per net
multiply-driven; 0 undriven)
                                                          Cell Information
                                   15 max fanout
21 levels
           10 max fanin
                                                                      PSEUDO_REG
                                                      0)
                                                                                       (ncount
FUNC STRAIGHT_WIRE_DESIGN (ncount 180 : area
                                                                   480)
                                   cb_clk_32_1 (ncount
                                                          6: area
83 : area
           0)
                                                          cs_ao12n03c (ncount
                                   70)
                                                                                  6: area
cb mode block (ncount
                        1 : area
                                                                                  cs ao22n10c
                       cs ao22n03c (ncount
                                             15 : area
                                                          90)
24)
                                              cs_invvn01c
                                                           (ncount 129 : area
                                                                                258)
                   18)
(ncount
         1 : area
                                                          cs_invvn04c (ncount
                                                                                5 : area
                                                                                           10)
cs invvn02c (ncount
                       7: area
                                 14)
                                                                      cs_invvn06c (ncount
                                                                                             9. .
           cs_invvn05c (ncount 13: area
                                             26)
                                   cs_invvn07c (ncount 10: area
                                                                     20)
        18)
: area
                                                          cs_invvn09c (ncount
                                                                                 7: area
                                                                                           28)
                       3: area
cs_invvn08c (ncount
                                                                      cs_invvn11c (ncount
                                                                                             5
           cs_invvn10c (ncount
                                  6: area
                                             24)
                                                         21 : area
                                   cs invvn12c (ncount
                                                                    126)
        30)
                                                                                            8)
                                                          cs_invvn14c (ncount
                                 32)
                                                                                 1 : area
cs_invvn13c (ncount
                       4 : area
                                                                      cs invvn16c (ncount
                                             40)
           cs_invvn15c (ncount
                                  4: area
                                   cs_invvn18c
                                                          1 : area
                                                                    20)
                                                (ncount
: area
        42)
                                                          cs_nnd2n02c (ncount 185 : area
                                 25)
cs invvn19c (ncount
                       1: area
                                                                                  cs nnd2n04c
                       cs_nnd2n03c
                                               3: area
                                                       9)
555)
                                     (ncount
                                                                                  cs nnd2n06c
                       cs_nnd2n05c
                                               3 : area
                                                         12)
       9)
                                     (ncount
                                   cs_nnd2n07c (ncount
                                                         3 : area
                                                                     12)
(ncount
         1: area
                                                          cs_nnd2n12c (ncount
                                                                                  1: area
cs_nnd2n11c (ncount
                        1: area
                                  11)
                                                         60)
                                                                                  cs nnd2n14c
                       cs_nnd2n13c
                                     (ncount
                                               4: area
                                                                                 108)
                                               cs_nnd3n02c (ncount 27: area
(ncount 2: area
                    38)
                                                                                 1 : area
cs nnd3n07c (ncount
                       2: area -- 12)
                                                          cs_nnd3n09c (ncount
                                                                                  cs nnd4n03c
                       cs nnd3n12c (ncount
                                               1: area
                                                         22)
12)
(ncount 6: area
                                               cs_nnd4n09c (ncount
                                                                      1 : area
                                                                                 16)
                    30)
cs_nor2n02c (ncount
                                  30)
                                                          cs_nor2n04c (ncount
                                                                                  2: area
                      10: area
                                                                      cs_nor3n03c (ncount
            cs nor2n12c (ncount
                                  1 : area
                                             12)
                                                                                  cs_oa21n03c
                                                         12)
                       cs nor3n10c (ncount "1: area
: area
                                   cs oa21n04c (ncount
                                                           1 : area
(ncount
         1 : area
                    5)
                                                          cs_oa22n03c (ncount
                                                                                  1: area
                                   8)
cs oa21n05c (ncount
                        1: area
                                                                                  cs xbo2n01d
                       cs xbn2n01b
                                     (ncount 1: area
                                                          8)
6)
                                   Total Area = 2441 (Comb = 1891 : Non-Comb = 550)
                    8)
         1: area
(ncount
> write_end_point_report -points 2 [ET-0018]:>Begin...New EndPoint Report
                                                                            for file
/tmp/end_point_report..147522. [ET-0019]:<End.....New Endpoint Report.
                                                                        Sun Apr 18 21:57:46
                                                          EDA EinsTimer EndPoint Report
1999 Part : IDCDSUC Mode : Late Mode / Nominal
Release Level: 03.01 and Compiled: Fri Feb 5 09:05:11 1999 Min. Slack: -1.13427E+38
                                                        Max. Endpoints: 2 Cause of Slack
Max. Slack: 1.13427E+38 Sort Field: Slack
Abbreviation Comparison/Description
                              Slack due to a point downstream on path Required Arrival Time
                  SIkCont
Continuation
          ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT
( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup
                                                                                 ClkGSet
DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating
                       ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME
            ClkGHld
                                                   ( CLOCK LEADING EDGE + PULSE WIDTH <
                                       CIKTPW
+ ADJUST ) Clock Tree Pulse Width
```

```
CLOCK TRAILING EDGE ) Setup Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST ) Hold ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST ) EndOfCycle EndOfC ( DATA ARRIVAL TIME
   + CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth
                                                    ClkPW (CLOCK
   LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) ClockSeparation ClkSep
   ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) LOOP
   ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST)
   Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/
   LimitedAT/
                                Delay/ Failed Test/ Test PinName
   E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName
                                     .
     0 dcd_succ_last_t1 RAT
                                                             929
   1345 -416 123 1078 7 cs_invvn 18c cs_invvn18c 0 dcd_succ_last_t1 ---->
                      F C3+R
                                1279 -416 83 302 4 cs invvn 18c
   cs_invvn18c 66 N675 ---->{a} C2738/v
                                             F C3+R 1279 -416 83
   302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 ---> C2738/b
   C3+R 1228 -416 118 1261 4 cs_nnd2n 14c cs_nnd2n14c 50 N1098 ---->
   C2734rwr/y
                         R C3+R 1228 -416 118 1261 4 cs_invvn
   FC3+R 1172 -416 54
   310 1 cs_invvn 19c cs_invvn19c 56 N1097 ----> C2728rwr/y
   C3+R 1172 -416 54 310 1 cs_invvn 16c cs_invvn16c 0 N1097 ---->
                         R C3+R 1139 -416 104 181 2 cs_invvn 16c
   C2728rwr/a
   cs_invvn16c 33 N1692 ---->{b} C2725rwr/y R C3+R 1139 -416 104 181 2 cs_nnd2n 13c cs_nnd2n13c 0 N1692 ----> C2725rwr/a
   F C3+R 1083 -416 91 161 2 cs_nnd2n 13c cs_nnd2n13c 56 N1479 ---->{c} C2721rwr/y F C3+R 1083 -416 91 161 2 cs_nnd3n 12c
   R C3+R 1019 -416 199
2709rwr/y
   R C3+R 679 -416 144 18 1 cs_nnd4n 03c
   C2440rwr/b
   cs_nnd4n03c 68 N283 ---->{h} C2318/y
                                              R C3+R 679 -416 144
   C3+R 598 -416 81 37 2 cs_oa21n 04c cs_oa21n04c 81 three_branches ---->
                                  598 -416 81 37 2 PI 0
                        F C3+R
   three_branches
   three_branches
   ----- 2 dcd_succ_last
                                  F C3+R 1294 -415 79 1078 7
     0 ----> C2744/v
                                 F C3+R 1294 -415 79 1078 7 cs_invvn
   R C3+R 1241
   -415 119 302 4 cs_invvn 18c cs_invvn18c 53 N675 ---->{a} C2738/y
   R C3+R 1241 -415 119 302 4 cs_nnd2n 14c cs_nnd2n14c 0 N675 --->
                        F C3+R 1175 -415 76 1261 4 cs_nnd2n 14c
   C2738/b
   cs_nnd2n14c 66 N1098 ----> C2734rwr/y
                                              FC3+R 1175 -415 76
   1261 4 cs_invvn 19c cs_invvn19c 0 N1098 ----> C2734rwr/a
   C3+R 1130 -415 80 310 1 cs_invvn 19c cs_invvn19c 45 N1097 --->
                        R C3+R 1130 -415 80 310 1 cs_invvn
   C2728rwr/v
                                                              16c
```

```
1089 -415
                                                                                   72
                                                            FC3+R
             0 N1097 ----> C2728rwr/a
cs invvn16c
                                                                                       F
                      16c cs_invvn16c 41 N1692 ---->{b} C2725rwr/y
181 2 cs_invvn
                     72 181 2 cs_nnd2n
                                                 13c cs nnd2n13c
                                                                   0 N1692 ---->
        1089 -415
C3+R
                                          1041 -415
                                                      132 161 2 cs_nnd2n
                                                                                    13c
                                R C3+R
C2725rwr/a
                                                              RC3+R
                                                                                    132
              48 N1479 ---->{c} C2721rwr/y
                                                                        1041 -415
cs_nnd2n13c
                                          0 N1479 ----> C2721rwr/c
                       12c cs nnd3n12c
161 2 cs_nnd3n
                                                                  72 N892 ---->{d} C2338/y
                                                 12c cs_nnd3n12c
                    60 113 2 cs nnd3n
C3+R
        969
             -415
                                                                     0 N892 ---> C2338/a
                                                  13c cs_nnd2n13c
          969 -415
                      60 113 2 cs_nnd2n
FC3+R
                                                   13c cs_nnd2n13c
                                                                    32 N1119 ---->
                          124 3 cs_nnd2n
              -415
R C3+R
          937
                      72
                                                     72 124 3 cs_invvn
                                                                                 13c
                               RC3+R
                                         937
                                              -415
C2905/v
                                                                                      90
                                                           FC3+R
                                                                     901
                                                                                 63
             0 N1119 ----> C2905/a
                                                                           -415
cs_invvn13c
                  13c cs_invvn13c 36 N2010 ---->{e} C2906/y
                                                                                  FC3+R
1 cs_invvn
                                                         0 N2010 ---> C2906/a
901 -415
                 90 1 cs_nor2n
                                       12c cs_nor2n12c
            63
                                                  12c cs_nor2n12c 33 dcd_blk_dsucc ---->
              -415
                      80 76 1 cs_nor2n
R C3+R
          868
                                 RC3+R
                                            868
                                                 -415
                                                        80
                                                            76 1 PI
dcd_blk_dsucc
dcd_blk_dsucc
.
                          > report area Design: /IDCDSUC - Area: 4516.000000, Area(Weight):
                     > cputime Used 1.71 cpu seconds or 00:00:01 wall time, used 0 bytes or 0 byte.
2441.000000
[hnl_attr]: Attributes registered for copy for type: PORT. MASK_ANYTHING_MASKED_ON_PORT
[hnl attr]: Attributes registered for copy for type: CELL. MASK_ANYTHING_MASKED_ON_CELL
MASK_USER_CELL_NOCHANGE MASK_USER_CELL_NODESTROY
MASK_USER_CELL_NOTOUCH SUGGESTED_LIBRARY_CELL SUGGESTED_PARALLEL_FANOUT
SUGGESTED_SIZE SUGGESTED_SWAP SYN_USAGE_BOX_HIDE [hnl_attr]: Attributes registered for
copy for type: PIN. MASK_ANYTHING_MASKED_ON_PIN MASK_USER_PIN_NOADD
MASK_USER_PIN_NOCHANGE MASK_USER_PIN_NONEWNET MASK_USER_PIN_NOTOUCH
SUGGESTED_SERIAL_FANOUT SYN_SAS_NAME [hnl_attr]: Attributes registered for copy for type:
nl_attr]: 0 port(s) have attribute(s) registered for copy. [hnl_attr]: 197 cell(s) have attribute(s) registered for
copy. [hnl_attr]: 10 net(s) have attribute(s) registered for copy. [hnl_attr]: 1242 pin(s) have attribute(s)
```

registered for copy. [hnl. attrl: Attributes registered for copy for type: PORT. MASK\_ANYTHING\_MASKED\_ON\_PORT [hnl\_attr]: Attributes registered for copy for type: CELL. MASK ANYTHING\_MASKED\_ON\_CELL MASK\_USER\_CELL\_NOCHANGE MASK\_USER\_CELL\_NOTOUCH SUGGESTED\_LIBRARY\_CELL\_ SUGGESTED\_PARALLEL\_FANOUT SUGGESTED\_SIZE SUGGESTED\_SWAP SYN USAGE BOX HIDE [hnl attr]: Attributes registered for copy for type: PIN. MASK ANYTHING MASKED ON PIN MASK USER PIN NOADD MASK\_USER\_PIN\_NOCHANGE MASK\_USER\_PIN\_NONEWNET.MASK\_USER\_PIN\_NOTOUCH SUGGESTED\_SERIAL\_FANOUT SYN\_SAS\_NAME [hnl\_attr]: Attributes registered for copy for type: NET. MASK\_ANYTHING\_MASKED\_ON\_NET MASK\_USER\_NET\_NOTOUCH [hnl\_attr]: 0 port(s) have attribute(s) registered for copy. [hnl\_attr]: 197 cell(s) have attribute(s) registered for copy. [hnl\_attr]: 10 net(s) have attribute(s) registered for copy. [hnl\_attr]: 1242 pin(s) have attribute(s) registered for copy. > add\_reg -idesign \_\_CiType\_13\_30da5570 -cloning 100 [SYNZ\_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP, and below. [ET-0112]:Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP; and below. [SYNZ MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]: Deleting timing for design: PSEUDO REG, analysis mode:SLOW\_CHIP, and below. [ET-0112]:Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP, and below. [SYNZ\_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP, and below. [ET-0112]:Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP, and below. [SYNZ MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]: Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP, and below. [SYNZ\_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design: PSEUDO\_REG, analysis mode:SLOW\_CHIP, and below. [SYNZ MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]: Deleting timing for design: PSEUDO REG, analysis mode:SLOW\_CHIP, and below. [SYNZ\_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]: Deleting timing for design: PSEUDO\_REG, analysis mode: SLOW\_CHIP, and

```
below. [SYNZ_MAP-1]: Cloning gate 'C2077' of type 'cs_invvn14c' [ET-0112]: Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-1]: Cloning gate 'C2020' of type 'cs_invvn09c' [ET-0112]: Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW CHIP, and below.
design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-3]: Inserting an inverter to drive
register from PI [ET-0112]: Deleting timing for design: PSEUDO_REG, analysis mode: SLOW_CHIP, and
below. [SYNZ_MAP-3]: Inserting an inverter to drive register from PI [ET-0112]:Deleting timing for
design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-3]: Inserting an inverter
to drive register from PI [ET-0112]: Deleting timing for design: PSEUDO_REG, analysis
mode:SLOW_CHIP, and below. [SYNZ_MAP-3]: Inserting an inverter to drive register from PI
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-3]: Inserting an inverter to drive register from PI [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-8]: No register with the
appropriate logic input could be found, inserting inverter [ET-0112]:Deleting timing for design:
```

```
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO REG. analysis mode:SLOW CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-1]: Cloning gate 'C2622' of type
'cs_nor2n02c' [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]: Deleting timing for design:
PSEUDO REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
T-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]: Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [SYNZ_MAP-2]: Inserting an inverter, instead
of cloning gate [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and
below. [SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
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PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO REG, analysis mode:SLOW CHIP, and below. [SYNZ_MAP-1]: Cloning gate 'C1959' of type
'cs invvn01c' [ET-0112]: Deleting timing for design: PSEUDO_REG, analysis mode: SLOW_CHIP, and
below. [ET-0112]:Deleting timing for design: PSEUDO_REG, analysis mode:SLOW_CHIP, and below.
[SYNZ_MAP-2]: Inserting an inverter, instead of cloning gate [ET-0112]:Deleting timing for design:
PSEUDO REG, analysis mode:SLOW_CHIP, and below. [ET-0112]:Deleting timing for design:
PSEUDO_REG, analysis mode:SLOW_CHIP, and below. add_reg processed 83 register cells inserted
                                                            Instead of cloning
                       Pls or reg driven or brkpt 5
22 inverters:
No matching register input 1 Cloned gates 4 Unmapped registers 0 ***** end Synzilla *****
SYNZPROMPT
                       > hnl::hnl_nets_preserve -restore
                                                           > write_vim -dir
□[10Creturn_to_bdz
/data/laceyl/synztmp/IDCDSUC/IDCDSUC -r -... [VIM-7701]: Design: IDCDSUC :: Writing DEF:
/data/laceyl/synztmp/IDCDSUC/IDCDSUC/DEF/IDCDSUC, View:
/data/laceyl/synztmp/IDCDSUC/IDCDSUC/HISVHDL/IDCDSUC. [VIM-7721]: Unmapped constant cell(s)
                                                       > echo NORMAL_RETURN >
skipped: 1. [VIM-7722]: BRKPT cell(s) processed: 180.
use cds
       > read_vim -library /data/laceyl/synztmp/IDCDSUC/IDCDSUC -...
[ET-112]: Deleting timing for design: IDCDSUC, analysis mode:default, and below.
Reading proto IDCDSUC...
       > padnet
       > msg::set_level -msgid ICM-23 -hidden
        > read_timer_parms -file /data/laceyl/synztmp/IDCDSUC/IDCD...
[ICM-15]: >Begin...Parm Reader
       for file /data/laceyl/synztmp/IDCDSUC/IDCDSUC.tparms.
[ICM-16]: <End.....Parm Reader.
       > msg::set_level -msgid ICM-23 -error
       > hide_clock_tree -hierarchy
[ET-203]: Timing top level created for design: IDCDSUC, analysis mode: default.
[ET-415]: Timer/Delay computation has been triggered.
```

[ET-27]: No subsequent messages of this type will be reported.

```
Increase timing debug level for complete set of these messages.
[ET-601]: (W) The model build for block: gptr_latch, cell name: cb_mode_block failed.
     Default modelling will be used for this block.
0 gates were hidden.
      > is_parm no_tech_redund
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/rm_tech_redund.tcl
         > ECMarkOriginalBoxes
         > str_parm tgfs_effort
         > is_parm remove_redundant_regs
          > make_constants_in nonreg_only
         > ignore_trivial_expansions EQNVIEW
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/ECgenexp.tcl
           > expansions_from_tib EQNVIEW
           > expansions_from_eqn EQNVIEW
           > copy_def_to_proto EQNVIEW
            > apply decide boolean(EQNVIEW)
generated 1 paths in 70 milliseconds
         > apply Hstructure(EQNVIEW)
generated 1 paths in 40 milliseconds
         > gen_nonreg_tib_expns TIB_EXPANSIONS
         > apply Hunstructure()
         > expandable_name
            > set_nochange
              > constmod mark_modified_boxes
              > is_parm keep_bad_pgroups
> bad_pgroups_expandable
             > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
             > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
            > headless
> cleanse1
     > cleanse1
     > nochange
            > set_nochange
           > constmod mark_modified_boxes
              > is_parm keep_bad_pgroups
     > bad_pgroups_expandable
              > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
              > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
              > headless
              > cleanse1
             > nochange
          > set_nochange
          > apply {Hstructure( EQNVIEW TIB EXPANSIONS)}
generated 1 paths in 60 milliseconds
          > rtolbox {Htqfsredund( 100 )}
          > apply Hunstructure()
          > nochange
         > DeleteAllProtosUnderView TIB_EXPANSIONS
[SRULE-17175]: Deleted 5 Proto Boxes
         > randsim q
         > randsim q
         > is_parm keep_bad_pgroups
          > copyinfo
          > fix_bad_pgroups
         > basetype
         > copyinfo
```

```
> cleanse
          > nextbox tchname(NOERR)
          > cleanse
          > copyinfo
          > has_children CONSTANT
            > tiegen FOLIM(8)
          > nextbox {EChideBoxes(ALL OLD HIDE)}
          > nextbox {EChideBoxes(PERI OLD RESTORE)}
          > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...
          > compare_key_slack_limit TIME_REDUND
[ET-1301]: (W) Applied default arrival time for
      boundary pin clkg.
[ET-27]: No subsequent messages of this type will be reported.
     Increase timing debug level for complete set of these messages.
[ET-413]: (W) Using default pin capacitance 0.200000 for boundary output pin scan_out.
[ET-27]: No subsequent messages of this type will be reported.
      Increase timing debug level for complete set of these messages.
[ET-1302]: (W) Applied default required arrival time for
      boundary pin scan_out.
[ET-27]: No subsequent messages of this type will be reported.
     Increase timing debug level for complete set of these messages.
           > reset_key_slack_limit TIME_REDUND
           > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
           > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}
          > compare_key_slack_limit TIME_REDUND
          > delete_key_slack_limit TIME_REDUND
          > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
          > quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
          > nextbox {EChideBoxes(ALL OLD RESTORE)}
          > ECdeleteAllKeys
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_setup_timer.tcl
      > ::setup_timer
[make_feedthru_boxes]: IOPADs, BRKPTs, etc. set to FEEDTHRU boxes.
[set slew prop]: Setting slew propagation to 0 (OFF)
[setup_timer]: ETE_CAP_LIMIT_MODE parm or env.var. was not set.
[setup_timer]: Default cap limit formula will be used.
[setup_timer]: GLOBAL_SLEW_LIMIT parm or env.var. was not set.
[setup_timer]: Delay-rule limits will be used.
[ET-110]: License obtained for ..... EinsTimer_Statistics 1.1
[set_LM_and_EM_delay_combinations]: Global linear combination box delay (LCD) multipliers have been
[set_LM_and_EM_delay_combinations]: Linear combination box delay (LCD) multipliers have been set for
default amode:
[set_LM_and_EM_delay_combinations]: LM_WC = 1, LM_BC = 0, LM_NOM = 0
[set_LM_and_EM_delay_combinations]: EM_WC = 1, EM_BC = 0, EM_NOM = 0
[setup_timer]: BOX_DELAY_MULTIPLIER parm or env.var. was not set.
[setup_timer]: Box dly multiplier will not be set. Default = 1.0
[use_clock_overrides]: Clock override usage has been set to NO.
[set_timer_msg_function]: EinsTimer message handler was set to synmsg.
[set_timer_good_reg_function]: EinsTimer good-reg-function was set to the default (good_reg_name).
[set_tib_timing_coefficients]: Asserting TIB delays:
[set_tib_timing_coefficients]: TIB_GATE_DLY = 100, TIB_FANIN_DLY = 10, TIB_FANOUT_DLY = 0,
```

> nextbox {mapprim, mapterm}

```
[set_tib_timing_coefficients]: TIB_R_OUT = 0.3, TIB_PINCAP = 20,
[set_tib_timing_coefficients]: TIB_SETUP = 0, TIB_HOLD = 0
[set_clock_gate_constraints]: Clock gate constraints set: SETUP=100, HOLD=100, PW=0.
[setup_timer]: Setting up the cap and RC subsystem.
[set_cap_calc]: ETE-style net cap estimation turned ON.
[set_cap_calc]: ETE techEST rule will be used for wire cap estimation.
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/pdlink.dll
pdlink.dll version 4.1 (Apr 14 1999 17:21:59)
[set_rc_calc]: ETE-style RC estimation turned ON.
[set_rc_calc]: ETE RCN rule will be used.
[set_rc_calc]: RC delays and slew effects turned OFF!.
[setup_timer]: ETE_ESTRULE parm or env.var. was not set.
[setup_timer]: ETE wire ESTimation rule will not be read.
[setup_timer]: ETE_RCN parm or env.var. was not set.
[setup_timer]: ETE RCN rule will not be read.
[setup_timer]: ETEPATH environment variable not set
       > read_timer_parms -file /afs/apd/func/vlsi/alliance00/tim...
[ICM-15]: >Begin...Parm Reader
        for file /afs/apd/func/vlsi/alliance00/timing/parms/cpsynz.parms.
[ICM-16]: <End.....Parm Reader.
       > set_cap_limit_formula TYPE0
       > set_slew_prop ON
[set_slew_prop]: Setting slew propagation to 1 (ON)
       > set_net_delay_calc -mode_noest
[CTE::gp390_setup_timer]: setting nominal delay mode
        > set_delay_mode -nominal
       > set_vdd -vdd_best 1.7 -vdd_worst 1.45 -vdd_nominal 1.45
       > set_temp -temp_best -10 -temp_worst 10 -temp_nominal 10
        > use_clock_overrides YES
[use_clock_overrides]: Clock override usage has been set to YES.
        > read_phase_file -file /afs/apd/func/vlsi/alliance00/bscc...
[ET-0018]: >Begin...PHASE reader
        for file /afs/apd/func/vlsi/alliance00/bscc8/v4/ndr/a00.phase.
[ET-0019]: <End.....PHASE reader.
       > set_default_slew -slew 151
        > idm::all_inputs
        > set_max_capacitance -cap 141 -ports {op_dsbl_after eu_iu...
        > set_default_pincap -value 1001
        > idm::all_outputs
        > set_max_transition -time 301 -ports {iu_eu_opcode_cmp iu...
        > read_assertions -path /afs/apd/func/vlsi/alliance00/timi...
[ET-0018]: >Begin...PIS reader
        for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pis.
[ET-0016]: (E) Pin/Net: aa_blk_dcd_prtl not found on line no: 31.
[ET-0016]: (E) Pin/Net: clkg0 not found on line no: 132.
[ET-0016]: (E) Pin/Net: clkg_0 not found on line no: 133.
[ET-0016]: (E) Pin/Net: clkg_00 not found on line no: 134.
[ET-0016]: (E) Pin/Net: clkg1 not found on line no: 135.
```

- [ET-0016]: (E) Pin/Net: clkg\_1 not found on line no: 136.
- [ET-0016]: (E) Pin/Net: clkg\_01 not found on line no: 137.
- [ET-0016]: (E) Pin/Net: clkg\_2 not found on line no: 139.
- [ET-0016]: (E) Pin/Net: clkg\_02 not found on line no: 140.
- [ET-0016]: (E) Pin/Net: clkg3 not found on line no: 141.
- [ET-0016]: (E) Pin/Net: clkg\_3 not found on line no: 142.
- [ET-0016]: (E) Pin/Net: clkg\_03 not found on line no: 143.
- [ET-0016]: (E) Pin/Net: clkg4 not found on line no: 144.
- [ET-0016]: (E) Pin/Net: clkg\_4 not found on line no: 145.
- [ET-0016]: (E) Pin/Net: clkg\_04 not found on line no: 146.
- [ET-0016]: (E) Pin/Net: clkg5 not found on line no: 147.
- [ET-0016]: (E) Pin/Net: clkg\_5 not found on line no: 148.
- [ET-0016]: (E) Pin/Net: clkg\_05 not found on line no: 149.
- [ET-0016]: (E) Pin/Net: clkg6 not found on line no: 150.
- [ET-0016]: (E) Pin/Net: clkg\_6 not found on line no: 151.
- [ET-0016]: (E) Pin/Net: clkg\_06 not found on line no: 152.
- [ET-0016]: (E) Pin/Net: clkg7 not found on line no: 153.
- [ET-0016]: (E) Pin/Net: clkg\_7 not found on line no: 154.
- [ET-0016]: (E) Pin/Net:.clkg\_07 not found on line no: 155.
- [ET-0016]: (E) Pin/Net: clkg8 not found on line no: 156.
- [ET-0016]: (E) Pin/Net: clkg\_8 not found on line no: 157.
- [ET-0016]: (E) Pin/Net: clkg\_08 not found on line no: 158.
- [ET-0016]: (E) Pin/Net: clkg9 not found on line no: 159.
- [ET-0016]: (E) Pin/Net: clkg\_9 not found on line no: 160.
- [ET-0016]: (E) Pin/Net: clkg\_09 not found on line no: 161.
- [ET-0016]: (E) Pin/Net: clkg11 not found on line no: 162.
- [ET-0016]: (E) Pin/Net: clkg22 not found on line no: 163.
- [ET-0016]: (E) Pin/Net: clkg33 not found on line no: 164.

```
[ET-0019]: <End.....PIS reader.
[ET-0018]: >Begin...ETA reader
        for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.eta.
[ET-0019]: <End.....ETA reader.
[ET-0018]: >Begin...POS reader
        for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/actual/IDCDSUC.pos.
[ET-0019]: <End.....POS reader.
        > idm::all_inputs
         > get_asserted_phases -pin op_dsbl_after -at
         > get_asserted_phases -pin eu iu spare1 -at
         > get_asserted_phases -pin second_op_lat -at
         > get_asserted_phases -pin mcr41_trap -at
         > get_asserted_phases -pin ifet_xcptn -at
         > get_asserted_phases -pin iu_eu_xcpt_pend -at
         > get_asserted_phases -pin iq_blk_d1 -at
         > get_asserted_phases -pin clkl_mode7 -at
Pin: NO PHASES for clkl_mode7: asserting default C3+R
          > set_arrival -time 401 -phase C3+R -ports clkl_mode7 -late
          > set_arrival -time 101 -phase C3+R -ports clkl_mode7 -early
         > get_asserted_phases -pin dcd_op 44 -at
         > get_asserted_phases -pin ru write in ig -at
         > get_asserted_phases -pin a_clk -at
Pin: NO PHASES for a_clk: asserting default C3+R
          > set_arrival -time 401 -phase C3+R -ports a clk -late
          > set_arrival -time 101 -phase C3+R -ports a_clk -early
         > get_asserted_phases -pin b_clk -at
Pin: NO PHASES for b_clk: asserting default C3+R
          > set_arrival -time 401 -phase C3+R -ports b_clk -late
          > set_arrival -time 101 -phase C3+R -ports b_clk -early
         > get_asserted_phases -pin ru_iu_rcvy_rst -at
         > get_asserted_phases -pin eu_iu_enter_slow md -at
         > get_asserted_phases -pin id_instr_stores -at
         > get_asserted_phases -pin op_inq_stores -at
         > get_asserted_phases -pin test_c1 -at
Pin: NO PHASES for test_c1: asserting default C3+R
          > set_arrival -time 401 -phase C3+R -ports test_c1 -late
          > set_arrival -time 101 -phase C3+R -ports test c1 -early
         > get_asserted_phases -pin iq_blk_aa -at
         > get_asserted_phases -pin aa_ofc_available -at
         > get_asserted_phases -pin eu_iu_mmode -at
         > get_asserted_phases -pin eu_iu_mcset_e1 -at
         > get_asserted_phases -pin aa_ofc_hold -at
         > get_asserted_phases -pin ru_98_43 -at
         > get_asserted_phases -pin srlz_op_match -at
         > get_asserted_phases -pin first_op_lat -at
         > get_asserted_phases -pin zero_branches -at
         > get_asserted_phases -pin dcd_mcr41_blk -at
         > get_asserted_phases -pin xu_iu_xlat_busy -at
         > get_asserted_phases -pin du_iu_hold_aa_reg -at
         > get_asserted_phases -pin eu_iu_fpu_end op -at
         > get_asserted_phases -pin eu_iu_misc_hold -at
         > get_asserted_phases -pin op_cmp_raw -at
```

```
> get_asserted_phases -pin op_dsbl_before -at
         > get asserted_phases -pin op_drain -at
         > get asserted_phases -pin eu_iu_fxu_end_op -at
         > get asserted_phases -pin op_mcend_raw -at
         > get_asserted_phases -pin eu_iu_br_wrong -at
         > get_asserted_phases -pin need_opnd_req -at
         > get_asserted_phases -pin legal_bht_br -at
         > get_asserted_phases -pin clkg -at
         > get_asserted_phases -pin bht_branch_req -at
Pin: NO PHASES for bht_branch_req: asserting default C3+R
          > set arrival -time 401 -phase C3+R -ports bht_branch_req ...
          > set_arrival -time 101 -phase C3+R -ports bht_branch_req ...
         > get_asserted_phases -pin id_ex_in_mm -at
         > get_asserted_phases -pin du_iu_quiesced -at
         > get_asserted_phases -pin iu_op_cmp_hit_a -at
         > get asserted_phases -pin iu_op_cmp_hit_b -at
         > get_asserted_phases -pin iu_op_cmp_hit_c -at
         > get asserted_phases -pin iu_op_cmp_hit_d -at
         > get_asserted_phases -pin dcd_frc_milli -at
         > get_asserted_phases -pin iq_empty -at
         > get_asserted_phases -pin op_serialize -at
         > get_asserted_phases -pin gptr_scan_in -at
Pin: NO PHASES for gptr_scan_in: asserting default C3+R
          > set arrival -time 401 -phase C3+R -ports gptr_scan_in -late
          > set_arrival -time 101 -phase C3+R -ports gptr_scan_in -e...
         > get_asserted_phases -pin aa_agi_lat -at
         > get_asserted_phases -pin branch_request -at
         > get_asserted_phases -pin ru_9a_52 -at
         > get_asserted_phases -pin bu_iu_quiesced -at
         > get_asserted_phases -pin dcd_blk_dsucc -at
         > get_asserted_phases -pin op_eim_dcd -at
         > get_asserted_phases -pin iqmcode_mod_390gr -at
         > get_asserted_phases -pin scan_in -at
Pin: NO PHASES for scan_in: asserting default C3+R
           > set arrival -time 401 -phase C3+R -ports scan_in -late
           > set_arrival -time 101 -phase C3+R -ports scan_in -early
         > get_asserted_phases -pin eu_iu_e1_exc_cond -at
         > get_asserted_phases -pin aa_ofc_block_req -at
         > get_asserted_phases -pin eu_iu_fpu_excpn -at
         > get asserted phases -pin block_aa_branch -at
         > get_asserted_phases -pin ru_iu_rq_blk -at
         > get_asserted_phases -pin op_chkpt_synch -at
         > get_asserted_phases -pin ireg_valid -at
         > get_asserted_phases -pin ru_9a_36 -at
         > get_asserted_phases -pin three_branches -at
          > get_asserted_phases -pin bht_block_dcd -at
Pin: NO PHASES for bht block_dcd: asserting default C3+R
           > set_arrival -time 401 -phase C3+R -ports bht_block_dcd -...
           > set arrival -time 101 -phase C3+R -ports bht_block_dcd -...
          > get asserted phases -pin ru_9a_20 -at
         > get_asserted_phases -pin iu_eu_data_blocked -at
          > get_asserted_phases -pin gptr_a_clk -at
Pin: NO PHASES for gptr_a_clk: asserting default C3+R
           > set arrival -time 401 -phase C3+R -ports gptr_a_clk -late
```

```
> set_arrival -time 101 -phase C3+R -ports gptr_a_clk -early
         > get_asserted_phases -pin gptr_b_clk -at
Pin: NO PHASES for gptr_b_clk: asserting default C3+R
           > set_arrival -time 401 -phase C3+R -ports gptr b clk -late
           > set_arrival -time 101 -phase C3+R -ports qptr_b_clk -early
         > get_asserted_phases -pin op_is_44 -at
         > get_asserted_phases -pin inst_fetches -at
         > get_asserted_phases -pin clkg2 -at
         > get_asserted_phases -pin eu_iu_fxu_exc_cond -at
         > get_asserted_phases -pin ru_9a_04 -at
         > get_asserted_phases -pin br_wrong_targ -at
         > get_asserted_phases -pin scan_enable -at
         > get_asserted_phases -pin du_iu_store status(0) -at
         > get_asserted_phases -pin du ju store status(1) -at
         > get_asserted_phases -pin du_iu_store_status(2) -at
         > get_asserted_phases -pin eu_iu_srlz op actn(0) -at
         > get_asserted_phases -pin eu iu srlz op actn(1) -at
         > get_asserted_phases -pin ru_9a_0001(0) -at
         > get_asserted_phases -pin ru_9a_0001(1) -at
         > get_asserted_phases -pin ireg_0_1(0) -at
         > get_asserted_phases -pin ireg_0_1(1) -at
         > get_asserted_phases -pin num_dcd_cyl(0) -at
         > get_asserted_phases -pin num_dcd_cyl(1) -at
         > get_asserted_phases -pin ru_9a_3233(32) -at
         > get_asserted_phases -pin ru_9a_3233(33) -at
         > get_asserted_phases -pin eu_iu_interrupt_info(0) -at
         > get_asserted_phases -pin eu_iu_interrupt info(1) -at
         > get_asserted_phases -pin eu_iu_interrupt_info(2) -at
         > get_asserted_phases -pin eu_iu_interrupt_info(3) -at
         > get_asserted_phases -pin ru_9a_1617(16) -at
         > get_asserted_phases -pin ru_9a_1617(17) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(0) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(1) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(2) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(3) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(4) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(5) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(6) -at
         > get_asserted_phases -pin eu_iu_srlz op encode(7) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(8) -at
         > get_asserted_phases -pin eu iu srlz op encode(9) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(10) -at
         > get_asserted_phases -pin eu_iu_srlz_op_encode(11) -at
         > get_asserted_phases -pin ru_9a_4849(48) -at
         > get_asserted_phases -pin ru_9a_4849(49) -at
         > get_asserted_phases -pin ireg_1631(22) -at
         > get_asserted_phases -pin ireg 1631(23) -at
         > get_asserted_phases -pin ireg_1631(24) -at
         > get_asserted_phases -pin ireg_1631(25) -at
         > get_asserted_phases -pin ireg_1631(26) -at
         > get_asserted_phases -pin ireg_1631(27) -at
         > get_asserted_phases -pin ireg 1631(28) -at
         > get_asserted_phases -pin ireg_1631(29) -at
         > get_asserted_phases -pin ireg_1631(30) -at
        > idm::all_outputs
```

```
> get_asserted_phases -pin iu_eu_opcode_cmp -rat
         > get_asserted_phases -pin iu_rcvry_reset -rat
         > get_asserted_phases -pin iu_reset_op_c -rat
         > get_asserted_phases -pin dcd_succ_last_t1 -rat
Pin: NO PHASES for dcd_succ_last_t1:
          > set_required -time 999 -phase C3+R -ports dcd_succ_last_...
          > set_required -time -999 -phase C3+R -ports dcd_succ_last...
         > get_asserted_phases -pin iu_milli_mode -rat
         > get_asserted_phases -pin iu_reset_op_c_t1 -rat
Pin: NO PHASES for iu_reset_op_c_t1:
          > set_required -time 999 -phase C3+R -ports iu_reset_op_c_...
          > set_required -time -999 -phase C3+R -ports iu_reset_op_c...
         > get_asserted_phases -pin dcd_succ_last -rat
         > get_asserted_phases -pin iu_eu_op_nomatch -rat
         > get_asserted_phases -pin ds_1st_maybe -rat
         > get_asserted_phases -pin id_xcute_targ -rat
         > get_asserted_phases -pin xc_frc_ia_to_if_t1 -rat
         > get_asserted_phases -pin dcd_success_tr -rat
         > get_asserted_phases -pin dsucc_or_agi_n -rat
         > get_asserted_phases -pin dsucc_or_agi -rat
         > get asserted phases -pin iu_slow_mode -rat
         > get_asserted_phases -pin slwmd_blk_n -rat
         > get_asserted_phases -pin xc_frc_milli -rat
          > get asserted phases -pin dcd_succ_first_t1 -rat
         > get_asserted_phases -pin iu_reset_all -rat
          > get_asserted_phases -pin iu_milli_mode_t1 -rat
          > get_asserted_phases -pin iu_milli_mode_t2 -rat
          > get_asserted_phases -pin iu_milli_mode_t3 -rat
          > get asserted phases -pin xc_frc_milli_t1 -rat
          > get asserted phases -pin iu_exc_cond -rat
          > get_asserted_phases -pin slow_mode_tr -rat
          > get_asserted_phases -pin iu_eu_slow_mode -rat
          > get asserted phases -pin dcd_success -rat
          > get_asserted_phases -pin iu_milli_mode_tr -rat
          > get_asserted_phases -pin iu_reset_if -rat
          > get asserted phases -pin exc_cond_tr -rat
         > get_asserted_phases -pin dcd_succ_first -rat
          > get_asserted_phases -pin execute_recovery -rat
          > get_asserted_phases -pin execute_xcptn -rat
          > get_asserted_phases -pin xc_frc_ia_to_if -rat
          > get_asserted_phases -pin iu_slow_mode_t1 -rat
Pin: NO PHASES for iu slow mode t1:
           > set_required -time 999 -phase C3+R -ports iu_slow_mode_t...
           > set_required -time -999 -phase C3+R -ports iu_slow_mode_...
          > get_asserted_phases -pin gptr_scan_out -rat
Pin: NO PHASES for gptr_scan_out:
           > set_required -time 999 -phase C3+R -ports gptr_scan_out ...
           > set_required -time -999 -phase C3+R -ports gptr_scan_out...
          > get_asserted_phases -pin iu_reset_fst -rat
          > get_asserted_phases -pin scan_out -rat
Pin: NO PHASES for scan_out:
           > set required -time 999 -phase C3+R -ports scan_out -late
           > set_required -time -999 -phase C3+R -ports scan_out -early
          > get_asserted_phases -pin iu_eu_dcd_succ_tr -rat
          > get_asserted_phases -pin idcdsuc_err -rat
```

```
Pin: NO PHASES for idcdsuc_err:
           > set_required -time 999 -phase C3+R -ports idcdsuc_err -late
           > set_required -time -999 -phase C3+R -ports idcdsuc err -...
          > get_asserted phases -pin frc milli -rat
          > get_asserted_phases -pin iu_intrupt_info(0) -rat
          > get_asserted_phases -pin iu_intrupt info(1) -rat
          > get_asserted_phases -pin iu_intrupt_info(2) -rat
          > get_asserted_phases -pin iu_intrupt_info(3) -rat
          > get_asserted_phases -pin blk_dcd_info_tr(0) -rat
          > get_asserted_phases -pin blk_dcd_info_tr(1) -rat
          > get_asserted_phases -pin blk_dcd_info_tr(2) -rat
          > get_asserted_phases -pin blk_dcd_info_tr(3) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(0) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(1) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(2) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(3) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(4) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(5) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(6) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(7) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(8) -rat
          > get_asserted_phases -pin iu srlz op encode(9) -rat
          > get_asserted_phases -pin iu srlz op encode(10) -rat
          > get_asserted_phases -pin iu_srlz_op_encode(11) -rat
          > get_asserted_phases -pin decode ilc(0) -rat
          > get_asserted_phases -pin decode ilc(1) -rat
          > get_asserted_phases -pin srlz_actn_tr(0) -rat
          > get_asserted_phases -pin srlz_actn_tr(1) -rat
          > get_asserted_phases -pin intrpt_info_tr(0) -rat
          > get_asserted_phases -pin intrpt_info_tr(1) -rat
          > get_asserted_phases -pin intrpt_info_tr(2) -rat
          > get_asserted_phases -pin intrpt_info_tr(3) -rat
          > get_asserted_phases -pin op_44 info tr(0) -rat
          > get_asserted_phases -pin op_44_info_tr(1) -rat
          > get_asserted_phases -pin dcd_c_cnt(0) -rat
          > get_asserted_phases -pin dcd c cnt(1) -rat
        > read_dcadi_file -file /afs/apd/func/vlsi/alliance00/bscc...
[ET-0018]: >Begin...ETE DCADJ reader
        for file /afs/apd/func/vlsi/alliance00/bscc8/v5/ndr/a00.dcadj.
[ET-0019]: <End.....ETE DCADJ reader.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_set_rc.tcl
  > write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report
        for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
*****POU92000-0107US1***** code invocation date
Sun Apr 18 21:58:17 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                         EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                      Max. Slack: 1.13427E+38
Sort Field: Slack
                                   Max. Endpoints: 2
 Cause of Slack
```

Abbreviation Comparison/Description

Slack Continuation		
Required Arrival Tim	SIkCont Slack due to a point downstream on path Per RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)	
Assorted Poquired /	Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL	
TIME)		
Clock Gating Setup ARRIVAL TIME + AD	ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK JUST)	
Clock Gating Hold	CIKGHID (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK	
ARRIVAL TIME + AD Clock Tree Pulse W	,	
TRAILING EDGE )	Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +	
Setup ADJUST)		
Hold	Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +	
ADJUST ) EndOfCycle	EndOfC ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +	
ADJUST) ClockPulseWidth	CIKPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK	
TRAILING EDGE)	· · · · · · · · · · · · · · · · · · ·	
ClockSeparation ARRIVAL TIME + AD	ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2	-
Loop	ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM	
CLOCK + ADJUST )		
Arrival Time Limiting	ATLimit Slack discontinuity due to failed test	
Num/	LimitedAT/ Delay/ Failed Test/	
Test PinName	E Phase AT Slack Slew CL FO Cell P Func T.Adj	
NetName		
•		
1 ded succ last	t1 R C3+R 3242 -2243 3621 1011 1 PO 0	
1 dcd_succ_last_dcd_succ_last_t1	_t1 R C3+R 3242 -2243 3621 1011 1 PO 0	
1 dcd_succ_last_dcd_succ_last_t1	999 0	
dcd_succ_last_t1 RAT> BOX714/OUT	999 0	-
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675>{a} C2738/y	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> {a} C2738/y 0 N675> C2738/b 48 dcd_success&0	999 0 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_nnd2n 14c NAND	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> {a} C2738/y 0 N675> C2738/b	999 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> C2738/y 0 N675> C2738/b 48 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/a	999 0 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_nnd2n 14c NAND	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> C2738/y 0 N675> C2734rwr/y 0 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/a 53 N1097> C2728rwr/y	999 0 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 Cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_invvn 19c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> {a} C2738/y 0 N675> C2738/b 48 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/a 53 N1097> C2728rwr/y 0 N1097	999 0 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_invvn 19c NOT  F C3+R 1236 -2243 40 310 1 cs_invvn 19c NOT  F C3+R 1236 -2243 40 310 1 cs_invvn 19c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> C2738/y 0 N675> C2738/b 48 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/a 53 N1097> C2728rwr/y 0 N1097> C2728rwr/a 31 N1692	999 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND R C3+R 1289 -2243 93 1261 4 cs_invvn 19c NOT F C3+R 1289 -2243 93 1261 4 cs_invvn 19c NOT F C3+R 1236 -2243 40 310 1 cs_invvn 19c NOT F C3+R 1236 -2243 40 310 1 cs_invvn 16c NOT R C3+R 1205 -2243 84 181 2 cs_invvn 16c NOT	
dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t18> C167/y 0 dcd_succ_last_t18> C167/a 1906 N675> {a} C2738/y 0 N675> C2738/b 48 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/y 0 dcd_success&0> C2734rwr/a 53 N1097> C2728rwr/y 0 N1097> C2728rwr/a	999 0 0 R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 IOPAD IOPAD  R C3+R 3242 -2243 3621 1011 1 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_invvn 01c NOT  F C3+R 1337 -2243 65 302 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_nnd2n 14c NAND  R C3+R 1289 -2243 93 1261 4 cs_invvn 19c NOT  F C3+R 1236 -2243 40 310 1 cs_invvn 19c NOT  F C3+R 1236 -2243 40 310 1 cs_invvn 19c NOT	

> C2725rwr/a	F C3+R 1148 -2243 98 161 2 cs_nnd2n 13c NAND
57 N1479 >{c} C2721rwr/y	F C3+R 1148 -2243 98 161 2 cs_nnd3n 12c NAND
0 N1479 > C2721rwr/a	R C3+R 1085 -2243 184 115 2 cs_nnd3n 12c NAND
63 N1497 >{d} C2709rwr/y	R C3+R 1085 -2243 184 115 2 cs_nor3n 10c NOR
0 N1497 > C2709rwr/c	F C3+R 973 -2243 97 52 1 cs_nor3n 10c NOR
112 N1976 >{e} C2579rwr_0_0/y 0 N1976	F C3+R 973 -2243 97 52 1 cs_nnd3n 07c NAND
> C2579rwr_0_0/b 64 N127	R C3+R 909 -2243 223 61 2 cs_nnd3n 07c NAND
> C2538/y N127	R C3+R 909 -2243 223 61 2 cs_invvn 01c NOT 0
> C2538/a blk_dcd_in(0)	F C3+R 785 -2243 85 16 1 cs_invvn 01c NOT 124
>{f} C2480rwr/y 0 blk_dcd_in(0)	F C3+R 785 -2243 85 16 1 cs_nnd3n 02c NAND
> C2480rwr/a 55 N393	R C3+R 730 -2243 121 17 1 cs_nnd3n 02c NAND
>{g} C2324/y 0 N393	R C3+R 730 -2243 121 17 1 cs_nnd2n 02c NAND
> C2324/b 89 N1728	F C3+R 641 -2243 203 215 8 cs_nnd2n 02c NAND
> C2224/y N1728	F C3+R 641 -2243 203 215 8 cs_invvn 06c NOT 0
> C2224/a 144 N1371	R C3+R 497 -2243 300 87 3 cs_invvn 06c NOT
>{h} C2061/y 0 N1371	R C3+R 497 -2243 300 87 3 cs_nnd2n 02c NAND
> C2061/a 169 dcd_cyl_cnt_q(0)	F C3+R 328 -2243 96 124 4 cs_nnd2n 02c NAND
> dcd_cyl_cnt.reg_n.lat_0/l2_ou SRL 0 dcd_cyl_cnt_q(0)	t_n F C3+R 328 -2243 96 124 4 cl_nnd2n 07c
> dcd_cyl_cnt.reg_n.lat_0/c2 168 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_nnd2n 07c SRL
> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
dcd_succ_last_t1	F C3+R 2696 -1697 2124 1011 1 PO 0
RAT> BOX714/OUT	999 F C3+R 2696 -1697 2124 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0	F C3+R 2696 -1697 2124 1011 1 IOPAD IOPAD
	F C3+R 2696 -1697 2124 1011 1 cs_invvn 01c NOT
> C167/a 1457 N675	R C3+R 1240 -1697 97 302 4 cs_invvn 01c NOT
>{a} C2738/y 0 N675	R C3+R 1240 -1697 97 302 4 cs_nnd2n 14c NAND

> C2738/b	FC3+R	1179 -1697	56	1261 4 cs_nnd2n	14c NAND
61 dcd_success&0	E 00 D	4470 4007		4004 4 incom	10° NOT
> C2734rwr/y	F C3+R	1179 -1697	56	1261 4 cs_invvn	19c NOT
0 dcd_success&0 > C2734rwr/a	R C3+R	1138 -1697	58	310 1 cs_invvn	19c NOT
41 N1097	11 00111	. 1100 1007	-	010 1 00 <u>_</u>	
> C2728rwr/y	R C3+R	1138 -1697	58	310 1 cs_invvn	16c NOT
0 N1097					
> C2728rwr/a	F C3+R	1099 -1697	61	181 2 cs_invvn	16c NOT
39 N1692	F C3+R	1099 -1697	61	181 2 cs_nnd2n	13c NAND
>{b} C2725rwr/y 0 N1692	r OJTN	1099 -1097	01	101 2 00_111021	1001010
> C2725rwr/a	R C3+R	1056 -1697	98	161 2 cs_nnd2n	13c NAND
43 N1479					
>{c} C2721rwr/y	R C3+R	1056 -1697	98	161 2 cs_nnd3r	12c NAND
0 N1479	E CO. D	992 -1697	86	115 2 cs_nnd3n	12c NAND
> C2721rwr/a 64 N1497	FC3+R	992 -1097	00	115 2 CS_IIIIUSII	12C NAIND
>{d} C2709rwr/y	FC3+R	992 -1697	86	115 2 cs_nor3n	10c NOR
0 N1497					
> C2709rwr/c	R C3+R	927 -1697	117	52 1 cs_nor3n	10c NOR
65 N1976	П СО.	D 007 160	1.77 <b>1</b>	17	3n 07c NAND
>{e} C2579rwr_0_0/y 0 N1976	R C3+	R 927 -169	<i>31</i> I	17 52 1 cs_nnd	OIL OLCHAND
> C2579rwr_0_0/b	F C3+F	R 842 -169	7 13	31 61 2 cs_nnd3	n 07c NAND
85 N127	,	•			
> C2538/y	F C3+R	842 -1697	131	61 2 cs_invvn (	one NOT 0
N127	D CO. D	752 -1697	96	16 1 cs_invvn 0	1c NOT 90
> C2538/a blk_dcd_in(0)	R C3+R	752 -1097	90	TO I CS_IIIVVII C	TICHOI 90
>{f} C2480rwr/y	R C3+R	752 -1697	96	16 1 cs_nnd3n	02c NAND
0 blk_dcd_in(0)			-		
> C2480rwr/a	FC3+R	688 -1697	90	17 1 cs_nnd3n	02c NAND
64 N393	E 00. B	600 1607	00	17 1 cs_nnd2n	02c NAND
>{g} C2324/y 0 N393	F C3+R	688 -1697	90	17 T CS_HHUZH	UZC NAND
> C2324/b	R C3+R	632 -1697	286	215 8 cs_nnd2n	02c NAND
56 N1728					
> C2224/y	R C3+R	632 -1697	286	215 8 cs_invvn	06c NOT 0
N1728	E 00 . D	450 1607	212	87 3 cs_invvn	neo NOT
> C2224/a 180 N1371	F C3+R	452 -1697	212	87 3 CS_IIIVVII	JOC INC I
>{h} C2061/y	F C3+R	452 -1697	212	87 3 cs_nnd2n	02c NAND
0·N1371					· : · · ·
> C2061/a	R C3+R	315 -1697	111	124 4 cs_nnd2n	02c NAND
137 dcd_cyl_cnt_q(0)		. CO. D 01E	1607	7 111 104 4 6	nnd2n 07a
> dcd_cyl_cnt.reg_n.lat_0/l2_or	ut_n H	C3+H 315	-109/	' 111 124 4 cl	_1110211 070
> dcd_cyl_cnt.reg_n.lat_0/c2	R C	3+ 160 N	/C	60 222 13 cl_nno	d2n 07c SRL
155 slow_mode.c2_1					
> slow_mode.clockblock/c2	RO	C3+ 160 I	N/C	60 222 13 cb_cl	k_32_1 LCB
0 slow_mode.c2_1					

<sup>&</sup>gt; timing\_reset

[timing\_reset]: Timing has been reset. > write\_end\_point\_report -points 2 [ET-0018]: >Begin...New EndPoint Report for file /tmp/end\_point\_report..92476. [ET-0019]: <End.....New Endpoint Report. Sun Apr 18 21:58:18 1999 Part: IDCDSUC Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38 Sort Field: Slack Max. Endpoints: 2 Cause of Slack Abbreviation Comparison/Description Slack Continuation SIkCont Required Arrival Time RAT Asserted Required Arrival Time AssrtRAT

Test PinName

NetName

Slack due to a point downstream on path ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating Hold ClkGHld ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width **CIKTPW** ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + Hold Hold ADJUST) EndOfCycle **EndOfC** ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST ) ClockPulseWidth ClkPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ClkSep ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop .. **ALTest** ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting **ATLimit** Slack discontinuity due to failed test Num/ LimitedAT/ Delay/ Failed Test/

1 dcd succ last t1 RC3+R 3242 -2243 3621 1011 1 PO dcd succ last t1 RAT 999 ----> BOX714/OUT R C3+R 3242 -2243 3621 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1 ----> BOX714/IN R C3+R 3242 -2243 3621 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1&0 ----> C167/y R C3+R 3242 -2243 3621 1011 1 cs\_invvn 01c NOT 0 dcd\_succ last t1&0 ----> C167/a FC3+R 1337 -2243 65 302 4 cs invvn 01c NOT 1906 N675 ---->{a} C2738/v FC3+R 1337 -2243 65 302 4 cs\_nnd2n 14c NAND

AT Slack Slew CL FO Cell

P Func T.Adi

E Phase

0 N675	
> C2738/b	R C3+R 1289 -2243 93 1261 4 cs_nnd2n 14c NAND
48 dcd_success&0	
> C2734rwr/y	R C3+R 1289 -2243 93 1261 4 cs_invvn 19c NOT
0 dcd_success&0	A NOT
> C2734rwr/a	F C3+R 1236 -2243 40 310 1 cs_invvn 19c NOT
53 N1097	F C3+R 1236 -2243 40 310 1 cs invvn 16c NOT
> C2728rwr/y	F C3+R 1236 -2243 40 310 1 cs_invvn 16c NOT
0 N1097	R C3+R 1205 -2243 84 181 2 cs_invvn 16c NOT
> C2728rwr/a	N 03+N 1203 -2243 04 101 2 05_IIIVVII 100 1001
31 N1692 >{b} C2725rwr/y	R C3+R 1205 -2243 84 181 2 cs_nnd2n 13c NAND
0 N1692	1100111 1200 2210 01 101 2 05
> C2725rwr/a	F C3+R 1148 -2243 98 161 2 cs_nnd2n 13c NAND
57 N1479	
>{c} C2721rwr/y	F C3+R 1148 -2243 98 161 2 cs_nnd3n 12c NAND
0 N1479	
> C2721rwr/a	R C3+R 1085 -2243 184 115 2 cs_nnd3n 12c NAND
63 N1497	
>{d} C2709rwr/y	R C3+R 1085 -2243 184 115 2 cs_nor3n 10c NOR
0 N1497	5 00 D 070 0040 07 50 1 00 nor0n 100 NOD
> C2709rwr/c	F C3+R 973 -2243 97 52 1 cs_nor3n 10c NOR
112 N1976	F C3+R 973 -2243 97 52 1 cs_nnd3n 07c NAND
>{e} C2579rwr_0_0/y 0 N1976	F C3+N 973 -2243 97 32 1 63_111doi1 070 Willo
> C2579rwr_0_0/b	R C3+R 909 -2243 223 61 2 cs_nnd3n 07c NAND
64 N127	
	R C3+R 909 -2243 - 223 61 2 cs_invvn 01c NOT 0.
N127	·
> C2538/a	F C3+R 785 -2243 85 16 1 cs_invvn 01c NOT 124
blk_dcd_in(0)	The second of the second of MAND
>{f} C2480rwr/y	F C3+R 785 -2243 85 16 1 cs_nnd3n 02c NAND
0 blk_dcd_in(0)	R C3+R 730 -2243 121 17 1 cs_nnd3n 02c NAND
> C2480rwr/a	R C3+R 730 -2243 121 17 1 cs_nnd3n 02c NAND
55 N393	R C3+R 730 -2243 121 17 1 cs_nnd2n 02c NAND
>{g} C2324/y 0 N393	11 OUT11 700 2270 121 17 100_1110211 020 17/110
> C2324/b	F C3+R 641 -2243 203 215 8 cs_nnd2n 02c NAND
89 N1728	
> C2224/y	F C3+R 641 -2243 203 215 8 cs_invvn 06c NOT 0
N1728	
> C2224/a	R C3+R 497 -2243 300 87 3 cs_invvn 06c NOT
144 N1371	
>{h} C2061/y	R C3+R 497 -2243 - 300 87 3 cs_nnd2n 02c NAND
0 N1371	E OO D
> C2061/a	F C3+R 328 -2243 96 124 4 cs_nnd2n 02c NAND
169 dcd_cyl_cnt_q(0)	out n FC3+R 328 -2243 96 124 4 cl_nnd2n 07c
> dcd_cyl_cnt.reg_n.lat_0/l2_o	NICTI F C3+M 320 -2243 90 124 4 CI_IIIU211 0/C
SRL 0 dcd_cyl_cnt_q(0)	R C3+ 160 N/C 60 222 13 cl_nnd2n 07c SRL
> dcd_cyl_cnt.reg_n.lat_0/c2 168 slow_mode.c2_1	TOOT TO TWO SO ELETS OF MINELLY STOCKE
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	.,

.

```
87 3 cs_nnd2n 02c NAND
                                           452 -1697
                                                       212
                                FC3+R
---->{h} C2061/y
0 N1371
                                R C3+R
                                           315 -1697
                                                       111 124 4 cs_nnd2n 02c NAND
----> C2061/a
137 dcd_cyl_cnt_q(0)
                                                  315 -1697
                                                              111 124 4 cl_nnd2n 07c
----> dcd_cyl_cnt.reg_n.lat_0/l2_out_n
                                       R C3+R
        0 dcd_cyl_cnt_q(0)
SRL
                                                     N/C
                                                            60 222 13 cl_nnd2n 07c SRL
                                     R C3+
                                               160
----> dcd_cyl_cnt.reg_n.lat_0/c2
155 slow_mode.c2_1
                                                160
                                                     N/C
                                                            60 222 13 cb_clk_32_1 LCB
                                      R C3+
----> slow_mode.clockblock/c2
0 slow mode.c2_1
  > accTime enable
[BD-13116]: Initializing accounting
  > write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 21:58:18 1999
Part: IDCDSUC
                                    EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                 Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                              Max. Endpoints: 2
Sort Field: Slack
                       Abbreviation Comparison/Description
 Cause of Slack
                                   Slack due to a point downstream on path
 Slack Continuation
                      SlkCont
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
                         RAT
                                      ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                        ClkGSet
 Clock Gating Setup
ARRIVAL TIME + ADJUST )
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                        CIkGHId
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 Clock Tree Pulse Width
                          CIKTPW
TRAILING EDGE )
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
 Setup
ADJUST)
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                   Hold
 Hold
ADJUST )
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                      EndOfC
 EndOfCycle
ADJUST)
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        CIkPW
 ClockPulseWidth
TRAILING EDGE)
                                   ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
                        ClkSep
 ClockSeparation
ARRIVAL TIME + ADJUST )
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                    ALTest
 Loop
CLOCK + ADJUST )
                                   Slack discontinuity due to failed test
 Arrival Time Limiting
                        ATLimit
                                                                     Delay/ Failed Test/
                                  LimitedAT/
  Num/
                                             AT Slack Slew CL FO Cell
                                                                            P Func T.Adi
  Test PinName
                                  E Phase
NetName
```

144 N1371 497 -2243 300 87 3 cs nnd2n 02c NAND R C3+R ---->{h} C2061/y 0 N1371 FC3+R 328 -2243 96 124 4 cs nnd2n 02c NAND ----> C2061/a 169 dcd\_cyl\_cnt\_q(0) 328 -2243 96 124 4 cl\_nnd2n 07c ----> dcd\_cyl\_cnt.reg\_n.lat\_0/l2\_out\_n FC3+R 0 dcd cyl\_cnt\_q(0) SRL 60 222 13 cl\_nnd2n 07c SRL N/C ----> dcd\_cyl\_cnt.reg\_n.lat\_0/c2 R C3+ 160 168 slow mode.c2\_1 ----> slow\_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb clk\_32\_1 LCB 0 slow mode.c2\_1 F C3+R 2696 -1697 2124 1011 1 PO 0 2 dcd\_succ\_last\_t1 dcd\_succ\_last\_t1 999 RAT 2696 -1697 2124 1011 1 IOPAD **IOPAD** FC3+R ----> BOX714/OUT 0 dcd\_succ\_last\_t1 **IOPAD** 2696 -1697 2124 1011 1 IOPAD ----> BOX714/IN FC3+R 0 dcd succ last\_t1&0 2696 -1697 2124 1011 1 cs\_invvn 01c NOT ----> C167/y FC3+R 0 dcd\_succ\_last\_t1&0 97 302 4 cs\_invvn 01c NOT R C3+R 1240 -1697 ----> C167/a 1457 N675 ---->{a} C2738/y RC3+R 1240 -1697 97 302 4 cs\_nnd2n 14c NAND .0 N675 1179 -1697 56 1261 4 cs\_nnd2n 14c NAND FC3+R ----> C2738/b 61 dcd success&0 FC3+R 1179 -1697 56 1261 4 cs\_invvn 19c NOT ----> C2734rwr/y 0 dcd success&0 310 1 cs\_invvn 19c NOT R C3+R 1138 -1697 58 ----> C2734rwr/a 41 N1097 310 1 cs\_invvn 16c NOT 1138 -1697 58 R C3+R ---> C2728rwr/y 0 N1097 1099 -1697 61 181 2 cs\_invvn 16c NOT . . . . . F C3+R ----> C2728rwr/a 39 N1692 181 2 cs\_nnd2n 13c NAND FC3+R 1099 -1697 61 ---->{b} C2725rwr/y 0 N1692 R C3+R 1056 -1697 98 161 2 cs\_nnd2n 13c NAND ----> C2725rwr/a 43 N1479 98 161 2 cs\_nnd3n 12c NAND RC3+R 1056 -1697 ---->{c} C2721rwr/y 0 N1479 FC3+R 992 -1697 86 115 2 cs\_nnd3n 12c NAND ----> C2721rwr/a 64 N1497 992 -1697 86 115 2 cs\_nor3n 10c NOR FC3+R ---->{d} C2709rwr/y 0 N1497 117 52 1 cs\_nor3n 10c NOR 927 -1697 R C3+R ----> C2709rwr/c 65 N1976 117 52 1 cs\_nnd3n 07c NAND 927 -1697 R C3+R ---->{e} C2579rwr\_0\_0/y 0 N1976 61 2 cs\_nnd3n 07c NAND 842 -1697 131 FC3+R ----> C2579rwr\_0\_0/b 85 N127 61 2 cs\_invvn 01c NOT 0 131 FC3+R 842 -1697 ----> C2538/y N127 96 16 1 cs\_invvn 01c NOT R C3+R 752 -1697 ----> C2538/a

blk_dcd_in(0) >{f} C2480rwr/y	R C3+R	752	-1697	96	16 1 cs_nnd3n	02c NAND	
0 blk_dcd_in(0) > C2480rwr/a	F C3+R		-1697		17 1 cs_nnd3n		
64 N393		•					
>{g} C2324/y 0 N393	F C3+R	688 -	1697	90	17 1 cs_nnd2n	02c NAND	
> C2324/b 56 N1728	R C3+R	632 -1	1697	286	215 8 cs_nnd2n	02c NAND	
> C2224/y	R C3+R	632 -1	697	286	215 8 cs_invvn	06c NOT	0
N1728 > C2224/a	F C3+R	452 -1	697	212	87 3 cs_invvn	OSC NOT	-
180 N1371							
>{h} C2061/y 0 N1371	F C3+R	452 -	1697	212	87 3 cs_nnd2n	02c NAND	
> C2061/a 137 dcd_cyl_cnt_q(0)	R C3+R	315 -1	1697	111	124 4 cs_nnd2n	02c NAND	
> dcd_cyl_cnt.reg_n.lat_0/l2_ot SRL 0 dcd_cyl_cnt_q(0)	ut_n R	C3+R	315	-1697	111 124 4 cl	_nnd2n <u>_</u> 07c	
> dcd_cyl_cnt.reg_n.lat_0/c2	R C	3+ 16	60 N/	C (	60 222 13 cl_nn	d2n 07c SRL	-
155 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1	RC				60 222 13 cb_c	lk_32_1 LCB	

#### > checkfan

## Electrical Violations in Network 'IDCDSUC'

		Capacitance Slew Fanout
Pin/Port		Limit / AdjLim / Actual Limit / AdjLim / Actual
eu_iu_enter_slow_md	-> eu_iu_enter_slo	w_md 141.00 / 141.00 / 16.89 290.00
/ 290.00 / 352.00 * 1		
eu_iu_mmode	-> eu_iu_mmode	141.00 / 141.00 / 32.56 290.00 /
290.00 / 326.00 * 1		
du_iu_hold_aa_req	-> du_iu_hold_aa_re	q 141.00 / 141.00 / 73.63 290.00 /
290.00 / 424.00 * 1		
eu_iu_fpu_end_op	-> eu_iu_fpu_end_op	141.00 / 141.00 / 15.67 290.00 /
290.00 / 339.00 * 1		
eu_iu_misc_hold	<pre>-&gt; eu_iu_misc_hold</pre>	141.00 / 141.00 / 18.88 290.00 /
290.00 / 332.00 * 1		
clkg	-> clkg	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 1		
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 16.89 290.00 /
290.00 / 338.00 * 1		
iq_empty	-> iq_empty	141.00 / 141.00 / 174.31 * 290.00 / 290.00
/ 116.00 1		
gptr_scan_in	-> gptr_scan_in	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1		
gptr_a_clk	-> gptr_a_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1		
gptr_b_clk	-> gptr_b_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1		
clkg2	-> clkg2	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 1		

```
141.00 / 141.00 / 15.67
                                                                                     290.00
                            -> eu iu fxu exc cond
eu iu_fxu_exc_cond
/ 290.00 / 390.00 * 1
                                                           141.00 / 141.00 / 16.89
                                                                                   290.00 /
                            -> du_iu_store_status(2)
du iu store status(2)
290.00 / 500.00 * 1
                                                            141.00 / 141.00 / 47.57
                                                                                    290.00 /
                            -> eu_iu_srlz_op_actn(0)
eu iu_srlz_op_actn(0)
290.00 / 374.00 * 1
                                                            141.00 / 141.00 / 47.57
                                                                                    290.00 /
                            -> eu_iu_srlz_op_actn(1)
eu_iu_srlz_op_actn(1)
290.00 / 341.00 * 1
                              -> eu_iu_srlz_op_encode(0)
                                                               141.00 / 141.00 / 16.89
eu iu srlz op encode(0)
290.00 / 290.00 / 401.00 * 1
                                                               141.00 / 141.00 / 16.89
                              -> eu iu srlz op encode(1)
eu iu srlz op_encode(1)
290.00 / 290.00 / 400.00 * 1
                                                               141.00 / 141.00 / 16.89
                              -> eu_iu_srlz_op_encode(2)
eu iu srlz op_encode(2)
290.00 / 290.00 / 420.00 * 1
                              -> eu_iu_srlz_op_encode(3)
                                                               141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(3)
290.00 / 290.00 / 302.00 * 1
                                                               141.00 / 141.00 / 16.89
                              -> eu_iu_srlz_op_encode(4)
eu_iu_srlz_op_encode(4)
290.00 / 290.00 / 406.00 * 1
                                                               141.00 / 141.00 / 16.89
eu iu srlz op encode(5)
                              -> eu iu srlz op_encode(5)
290.00 / 290.00 / 373.00 * 1
                                                               141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(6)
                              -> eu_iu_srlz_op_encode(6)
290.00 / 290.00 / 354.00 * 1
                                                               141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(7)
                              -> eu_iu_srlz_op_encode(7)
290.00 / 290.00 / 398.00 * 1
eu iu srlz op encode(8)
                              -> eu_iu_srlz_op_encode(8)
                                                               141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 * 1
eu_iu_srlz_op_encode(9)
                              -> eu_iu_srlz_op_encode(9)
                                                               141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 1
                              -> eu_iu_srlz_op_encode(11)
                                                                141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(11)
290.00 / 290.00 / 500.00 * 1
                                                                   78.50 / 78.50 / 220.92 *
c1@slow mode.clockblock:cb clk 32_1 -> slow mode.c1_1
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                                                   78.50 / 78.50 / 222.27 *
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
200.00 / 200.00 / 60.00 13 KEEP BTR KEEP BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
                                                                    78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                                                    78.50 / 78.50 / 237.92 *
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                                                    78.50 / 78.50 / 239.36 *
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2
                                                                    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                                                    78.50 / 78.50 / 237.92
c1@slow mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                                                    78.50 / 78.50 / 239.37 *
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3
                                                                    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4
                                                                    78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                                    78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4
                                                                    78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
                                                                    78.50 / 78.50 / 237.91 *
```

## 200.00 / 200.00 / 60.00 14 KEEP\_BTR KEEP\_BHC NO\_PARALLEL NO\_SERIAL

	Capacit	ance S	Slew Fa	anout
Pin/Port -> Net	Limit /	AdjLim / Actual	Limit / AdjLir	n / Actual
c2@slow_mode.clockblock_4:cb_clk_	32> slow_mode.c2_	5	78.50 / 78.5	0 / 239.37 *
200.00 / 200.00 / 60.00 14 KEEP_	_BTR KEEP_BHC NO_	PARALLEL NO	_SERIAL	
clka@slow_mode.clockblock_4:cb_cll	C3 -> slow mode.clka	5	78.50 / 78.50	0 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEF	P_BTR KEEP_BHC NO	_PARALLEL NO	D_SERIAL	
c1@slow_mode.clockblock_5:cb_clk_	32> slow_mode.c1	7	78.50 / 78.50	/ 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_	BTR KEEP_BHC NO_	PARALLEL NO	_SERIAL	
c2@slow_mode.clockblock_5:cb_clk_	32> slow_mode.c2	7	78.50 / 78.50	/ 239.37 *
200.00 / 200.00 / 60.00 14 KEEP_	BTR KEEP_BHC NO_	PARALLEL NO	SERIAL	
clka@slow_mode.clockblock_5:cb_clk	<ul><li>&lt;_3 -&gt; slow_mode.clka</li></ul>	7	8.50 / 78.50	/ 228.73 *
200.00 / 200.00 / 198.79 14 KEEF	BTR KEEP_BHC NO	PARALLEL NO	D_SERIAL	
y@C167:cs_invvn01c -> de	cd_succ_last_t1&0	68.00 /	68.00 / 101	1.00 * 301.00
/ 301.00 / 3676.28 * 1 KEEP_BTR				
	<b>1</b> 18&0	68.00 / 68.	00 / 1011.00	* 301.00 /
301.00 / 3608.92 * 1		4		
	N1371	70.00 / 70	.00 / 86.53 *	290.00 /
290.00 / 309.86 * 3				
	l146&0	68.00 / 68	.00 / 1011.00	* 301.00 /
301.00 / 3604.78 * 1				
	l1728	208.00 / 20	8.00 / 214.85	* 290.00 /
290.00 / 285.51 8	•			
	iu_reset_op_c_t1&0	70.00	/ 70.00 / 104	44.40 *
290.00 / 290.00 / 3683.69 * 3				
y@C2496:cs_nnd4n03c>	N1435	85.00 / 85	.00 / 97.83 *	290.00 /
290.00 / 353.82 * 5				
· · · · · · · · · · · · · · · · · · ·	l1645	133.00 / 13	3.00 / 150.69	* 290.00 /
290.00 / 273.28 6				
	N23	70.00 / 70.0	00 / 92.41 * 2	290.00 /
290.00 / 326.23 * 3	•	•		
	l1333	167.00 / 16	7.00 / 180.24	* 290.00 /
290.00 / 266.70 8				
y@C2794:cs_ao12n03c ->	N73	86.00 / 86.0	00 / 92.41 * 2	290.00 /
290.00 / 466.30 * 3	- · · · · · · · · · · · · · · · · · · ·	:		
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl	-> trc_blk_1cyc_q	247.0	0 / 247.00 /	256.34 *
290.00 / 290.00 / 205.99 8				

[BD-500900]: (W) There were 57 electrical violations. > checkfan

# Electrical Violations in Network 'IDCDSUC'

	Ca	apacitance S	lew Fanoi	ut
Pin/Port	-> Net	imit / AdjLim / Actual	Limit / AdiLim /	Actual
eu_iu_enter_slow_md / 290.00 / 352.00 * 1	-> eu_iu_enter_slow_		/ 141.00 / 16.8	
eu_iu_mmode 290.00 / 326.00 * 1	-> eu_iu_mmode	141.00 / 14	1.00 / 32.56 2	90.00 /
du_iu_hold_aa_req 290.00 / 424.00 * 1	-> du_iu_hold_aa_req	141.00 / 1	141.00 / 73.63	290.00 /
eu_iu_fpu_end_op 290.00 / 339.00 * 1	-> eu_iu_fpu_end_op	141.00 /	141.00 / 15.67	290.00 /
eu_iu_misc_hold	<pre>-&gt; eu_iu_misc_hold</pre>	141.00 / 14	1.00 / 18.88 2	290.00 /

```
290.00 / 332.00 * 1
                                               141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                      -> clkg
clkg
60.00
                          -> du_iu_quiesced
                                                         141.00 / 141.00 / 16.89
                                                                                  290.00 /
du_iu_quiesced
290.00 / 338.00 * 1
                                                    141.00 / 141.00 / 174.31 * 290.00 / 290.00
                        -> iq_empty
ia empty
/ 116.00
                                                      141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                         -> gptr_scan_in
gptr_scan_in
0.00 1
                                                    141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
gptr_a_clk
                        -> gptr_a_clk
0.00 1
                                                    141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                        -> gptr_b_clk
gptr_b_clk
0.00 1
                                                141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                      -> clkg2
clkg2
60.00
                                                             141.00 / 141.00 / 15.67
                                                                                      290.00
eu_iu_fxu_exc_cond
                             -> eu_iu_fxu_exc_cond
/ 290.00 / 390.00 * 1
                                                            141.00 / 141.00 / 16.89
                                                                                     290.00 /
du iu store status(2)
                            -> du_iu_store_status(2)
290.00 / 500.00 * 1
                                                             141.00 / 141.00 / 47.57
                                                                                      290.00 /
eu iu srlz_op_actn(0)
                             -> eu_iu_srlz_op_actn(0)
290.00 / 374.00 * 1
eu_iu_srlz_op_actn(1)
                             -> eu_iu_srlz_op_actn(1)
                                                             141.00 / 141.00 / 47.57
                                                                                      290.00 /
290.00 / 341.00 * 1
                              -> eu_iu_srlz_op_encode(0)
                                                                141.00 / 141.00 / 16.89
eu iu srlz op encode(0)
290.00 / 290.00 / 401.00 * 1
                              -> eu_iu_srlz_op_encode(1)
                                                                141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(1)
290.00 / 290.00 / 400.00 * 1
                                                                141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(2)
                              -> eu_iu_srlz_op_encode(2)
290.00 / 290.00 / 420.00 * 1
                                                                141.00 / 141.00 / 16.89
eu iu srlz op encode(3)
                              -> eu_iu_srlz_op_encode(3)
290.00 / 290.00 / 302.00 * 1
                                                               141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(4)
                              -> eu_iu_srlz_op_encode(4)
290.00 / 290.00 / 406.00 * 1
                                                                141.00 / 141.00 / 16.89
eu iu srlz op encode(5)
                              -> eu_iu_srlz_op_encode(5)
290.00 / 290.00 / 373.00 * 1
                                                                141.00 / 141.00 / 16.89
eu iu srlz_op_encode(6)
                              -> eu_iu_srlz_op_encode(6)
290.00 / 290.00 / 354.00 * 1
eu_iu_srlz_op_encode(7)
                              -> eu_iu_srlz_op_encode(7)
                                                                141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 * 1
                                                                141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(8)
                              -> eu_iu_srlz_op_encode(8)
290.00 / 290.00 / 367.00 * 1
                                                                141.00 / 141.00 / 16.89
eu iu srlz op encode(9)
                              -> eu_iu_srlz_op_encode(9)
290.00 / 290.00 / 323.00 * 1
                               -> eu_iu_srlz_op_encode(11)
                                                                 141.00 / 141.00 / 16.89
eu iu srlz_op_encode(11)
290.00 / 290.00 / 500.00 * 1
                                                                     78.50 / 78.50 / 220.92 *
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow mode.clockblock:cb clk 32_1 -> slow_mode.c2_1
                                                                     78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00 13 KEEP BTR KEEP BHC NO_PARALLEL NO_SERIAL
clka@slow mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
                                                                     78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
                                                                     78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                                                     78.50 / 78.50 / 239.36 *
c2@slow mode.clockblock 1:cb clk 32 -> slow mode.c2 2
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
```

		,
clka@slow_mode.clockblock_1:c 200.00 / 200.00 / 198.79 14	b_clk_3 -> slow_mode.clka_	_2
c1@slow_mode.clockblock_2:cb	_clk_32> slow_mode.c1_3	3
200.00 / 200.00 / 60.00 14 K c2@slow_mode.clockblock_2:cb	_clk_32> slow_mode.c2_;	3 78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 14 K	EEP_BTR KEEP_BHC NO_	PARALLEL NO_SERIAL _3
200.00 / 200.00 / 198.79 14	KEEP_BTR KEEP_BHC NO	_PARALLEL NO_SERIAL
c1@slow_mode.clockblock_3:cb	_clk_32> slow_mode.c1_4	4 78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 K c2@slow_mode.clockblock_3:cb	_clk_32> slow_mode.c2_4	4 78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 K	EEP_BTR KEEP_BHC NO_I	PARALLEL NO_SERIAL
clka@slow_mode.clockblock_3:c 200.00 / 200.00 / 198.79 14 ł	:b_cik_3 -> siow_mode.cika_ KEEP_BTR_KEEP_BHC_NO	_4
c1@slow_mode.clockblock_4:cb	_clk_32> slow_mode.c1_{	5 78.50 / 78.50 / 237.91 *
200.00 / 200.00 / 60.00 14 KI	EEP_BTR KEEP_BHC NO_	PARALLEL NO_SERIAL
Pin/Port -> Net	Capacita	ince Slew Fanout AdjLim / Actual Limit / AdjLim / Actual
	Limit / A	Adjlim / Actual   Limit / Adjlim / Actual   5   78.50   78.50   239.37 *
200.00 / 200.00 / 60.00 14 KI	_CIK_32> SIOW_MODE.C2_; EED_RTD_KEED_BUC_NO_I	78.50 / 78.50 / 239.37 °
clka@slow_mode.clockblock_4:c	h cik 3 -> slow mode cike	FANALLEL NO_SERIAL 5
200.00 / 200.00 / 198.79 14 k	KEEP BTR KEEP BHC NO	5 78.50 / 78.50 / 228.73 * _PARALLEL NO_SERIAL
c1@slow mode.clockblock 5:cb	clk 32 -> slow mode.c1	78 50 / 78 50 / 237 92 *
200.00 / 200.00 / 60.00 14 KI	EEP BTR KEEP BHC NO I	PARALLEL NO SERIAL
c2@slow_mode.clockblock_5:cb_	_clk_32> slow_mode.c2	78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 14 KI	EEP_BTR KEEP_BHC NO_I	PARALLEL NO_SERIAL
clka@slow_mode.clockblock_5:c	b_clk_3 -> slow_mode.clka	78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 H	KEEP_BTR KEEP_BHC NO.	_PARALLEL NO_SERIAL
y@C167:cs_invvn01c / 301.00 / 3676.28 * 1 KEEP_E	-> dcd_succ_last_t1&0 RTR	68.00 / 68.00 / 1011.00 * 301.00
/ 301.00 / 3676.28 * 1 KEEP_E y@C2013:cs_invvn01c 301.00 / 3608.92 * 1	-> N18&0	68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3608.92 * 1	NA OZA	
290.00 / 309.86 * 3	-> N10/1	70.00 / 70.00 / 86.53 * 290.00 /
y@C2082:cs_invvn01c	-> N146&0	68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 * 1	÷ •	
y@C2224:cs_invvn06c	-> N1728	208.00 / 208.00 / 214.85 * 290.00 /
290.00 / 285.51 8		<b>-0.00</b> / <b>-0.00</b> / / / / / / / / / / / / / / / / / /
y@C2393:cs_nnd2n02c 290.00 / 290.00 / 3683.69 * 3	-> iu_reset_op_c_t1&0	70.00 / 70.00 / 1044.40 *
y@C2496:cs_nnd4n03c	-> N1435	85.00 / 85.00 / 97.83 * 290.00 /
290.00 / 353.82 * 5	-> 141455	65.00 / 65.00 / 97.83 ** 290.00 /
y@C2646:cs_invvn04c	-> N1645	133.00 / 133.00 / 150.69 * 290.00 /
290.00 / 273.28 6		200.00 /
y@C2724:cs_nnd2n02c 290.00 / 326.23 * 3	-> N23	70.00 / 70.00 / 92.41 * 290.00 /
y@C2750:cs_invvn05c	-> N1333	167.00 / 167.00 / 180.24 * 290.00 /
y@C2794:cs_ao12n03c	-> N73	86.00 / 86.00 / 92.41 * 290.00 /
290.00 / 466.30 * 3	A = 1	
l2_out_n@frc_blk_1cyc.reg_n.lat_ 290.00 / 290.00 / 205.99 8	_U:cl -> trc_blk_1cyc_q	247.00 / 247.00 / 256.34 *

[BD-500900]: (W) There were 57 electrical violations.

> optimize\_delay -medium

[BD-80000]: check\_tech CMVC version 1.6 compiled on Apr 8 1999 at 05:20:06

bdz> late\_time 0 1

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/late\_time.tcl

> get\_default\_delay\_synlimit

> get\_default\_synlimit

> echo {In David's Exp. Timing Opt Scenario}

In David's Exp. Timing Opt Scenario

> checkfan

#### Electrical Violations in Network 'IDCDSUC'

		Capacitance Slew Fanout
Pin/Port	-> Net	Limit / AdjLim / Actual Limit / AdjLim / Actual
eu_iu_enter_slow_md	-> eu_iu_enter_st	ow_md 141.00 / 141.00 / 16.89 290.00
/ 290.00 / 352.00 * 1		
eu_iu_mmode	-> eu_iu_mmode	141.00 / 141.00 / 32.56 290.00 /
290.00 / 326.00 * 1		
du_iu_hold_aa_req	-> du_iu_hold_aa_r	eq 141.00 / 141.00 / 73.63 290.00 /
290.00 / 424.00 * 1		
eu_iu_fpu_end_op	-> eu_iu_fpu_end_d	op 141.00 / 141.00 / 15.67 290.00 /
290.00 / 339.00 * 1		
eu_iu_misc_hold	-> eu_iu_misc_hold	141.00 / 141.00 / 18.88 290.00 /
290.00 / 332.00 * 1		
clkg	-> clkg	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 1	•	
du_iu_quiesced	-> du_iu_quiesced	141.00 / 141.00 / 16.89 290.00 /
290.00 / 338.00 * 1	. •.	
iq_empty	-> iq_empty	141.00 / 141.00 / 174.31 * 290.00 / 290.00
/ 116.00 1	-	
gptr_scan_in	-> gptr_scan_in	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1		· .
gptr_a_clk	-> gptr_a_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1		
gptr_b_clk	-> gptr_b_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 1		
clkg2	-> clkg2	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 1		
eu_iu_fxu_exc_cond	-> eu_iu_fxu_exc_	cond 141.00 / 141.00 / 15.67 290.00
/ 290.00 / 390.00 * 1		(2)
du_iu_store_status(2)	-> du_iu_store_stat	us(2) 141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 * 1		. (0)
eu_iu_srlz_op_actn(0)	-> eu_iu_srlz_op_a	ictn(0) 141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 * 1		444.00 / 444.00 / 47.57
eu_iu_srlz_op_actn(1)	-> eu_iu_srlz_op_a	ictn(1) 141.00 / 141.00 / 47.57 290.00 /
290.00 / 341.00 * 1		1 (0) 444 00 / 444 00 / 40 00
eu_iu_srlz_op_encode(		_encode(0) 141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.		1 (4) 444 00 / 444 00 / 40 00
eu_iu_srlz_op_encode(	1) -> eu_iu_srlz_op	_encode(1) 141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.		1 (0) 444 00 / 444 00 / 40 00
eu_iu_srlz_op_encode(		_encode(2) 141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.		d-(0) 444.00 / 444.00 / 40.00
eu_iu_srlz_op_encode(		_encode(3) 141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.		144.00 / 444.00 / 40.00
eu_iu_srlz_op_encode(	4) -> eu_iu_srlz_op	_encode(4) 141.00 / 141.00 / 16.89

```
290.00 / 290.00 / 406.00 * 1
eu iu srlz op encode(5)
                             -> eu_iu_srlz_op_encode(5)
                                                             141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 * 1
eu_iu_srlz_op_encode(6)
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(6)
290.00 / 290.00 / 354.00 * 1
eu_iu_srlz_op_encode(7)
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(7)
290.00 / 290.00 / 398.00 * 1
eu iu srlz op encode(8)
                             -> eu_iu_srlz_op_encode(8)
                                                             141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 * 1
eu iu srlz op encode(9)
                             -> eu iu srlz op encode(9)
                                                             141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 * 1
eu iu srlz_op_encode(11)
                             -> eu_iu_srlz_op_encode(11)
                                                              141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 * 1
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1
                                                                 78.50 / 78.50 / 220.92 *
200.00 / 200.00 / 60.00 13 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
                                                                 78.50 / 78.50 / 222.27 *
200.00 / 200.00 / 60.00 13 KEEP BTR KEEP BHC NO PARALLEL NO SERIAL
clka@slow mode.clockblock:cb clk 32 -> slow mode.clka 1
                                                                 78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 13 KEEP BTR KEEP BHC NO PARALLEL NO SERIAL
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
                                                                  78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
                                                                 78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2
                                                                 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP BTR KEEP BHC NO PARALLEL NO SERIAL
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
                                                                  78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3
                                                                  78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow mode.clka 3
                                                                 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP BTR KEEP BHC NO PARALLEL NO SERIAL
c1@slow mode.clockblock 3:cb clk 32 -> slow mode.c1 4
                                                                  78.50 / 78.50 / 237.92
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                                  78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4
                                                                 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP BTR KEEP BHC NO PARALLEL NO SERIAL
c1@slow mode.clockblock 4:cb clk 32 -> slow mode.c1 5
                                                                  78.50 / 78.50 / 237.91 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
                                            Capacitance
                                                                Slew
                                                                           Fanout
Pin/Port
                      -> Net
                                              Limit / AdjLim / Actual Limit / AdjLim / Actual
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5
                                                                  78.50 / 78.50 / 239.37
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5
                                                                 78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP BTR KEEP BHC NO PARALLEL NO SERIAL
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1
                                                                78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
c2@slow_mode.clockblock 5:cb_clk_32_ -> slow_mode.c2
                                                                78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 14 KEEP_BTR KEEP_BHC NO_PARALLEL NO_SERIAL
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                                                                78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 14 KEEP_BTR KEEP_BHC NO PARALLEL NO SERIAL
y@C167:cs_invvn01c
                            -> dcd_succ_last_t1&0
                                                           68.00 / 68.00 / 1011.00 * 301.00
/ 301.00 / 3676.28 * 1 KEEP_BTR
y@C2013:cs_invvn01c
                             -> N18&0
                                                       68.00 / 68.00 / 1011.00 * 301.00 /
```

```
301.00 / 3608.92 * 1
                                                             70.00 / 70.00 / 86.53 * 290.00 /
                                 -> N1371
v@C2061:cs_nnd2n02c
290.00 / 309.86 * 3
                                                             68.00 / 68.00 / 1011.00 * 301.00 /
v@C2082:cs_invvn01c
                                -> N146&0
301.00 / 3604.78 * 1
                                                            208.00 / 208.00 / 214.85 * 290.00 /
                                -> N1728
v@C2224:cs_invvn06c
290.00 / 285.51 8
                                                                  70.00 / 70.00 / 1044.40 *
v@C2393:cs nnd2n02c
                                 -> iu_reset_op_c_t1&0
290.00 / 290.00 / 3683.69 * 3
                                                             85.00 / 85.00 / 97.83 * 290.00 /
                                 -> N1435
v@C2496:cs nnd4n03c
290.00 / 353.82 * 5
                                                             133.00 / 133.00 / 150.69 * 290.00 /
y@C2646:cs_invvn04c
                                -> N1645 .
290.00 / 273.28 6
                                                            70.00 / 70.00 / 92.41 * 290.00 /
                                 -> N23
y@C2724:cs_nnd2n02c
290.00 / 326.23 * 3
                                                             167.00 / 167.00 / 180.24 * 290.00 /
y@C2750:cs_invvn05c
                                -> N1333
290.00 / 266.70 8
                                                            86.00 / 86.00 / 92.41 * 290.00 /
                                 -> N73
v@C2794:cs_ao12n03c
290.00 / 466.30 * 3
                                                                   247.00 / 247.00 / 256.34 *
12 out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
290.00 / 290.00 / 205.99 8
[BD-500900]: (W) There were 57 electrical violations.
        > echo {Standard Late Time}
Standard Late Time
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/lx.tcl
       > echo {Delay Effort = 5}
Delay Effort = 5
       > echo {Area Effort = 4}
Area Effort = 4
       > echo {initialize window repower}
initialize window repower
         > hide -clear -cells { cs_ao12f }
         > find cell cs ao12f*
         > hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
         > hide -clear -cells { cs_nnd2f cs_nnd2w }
         > find cell cs nnd2f*
         > hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
         > find cell cs_nnd2w*
         > hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
          > hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
          > find cell cs_nnd3f*
          > hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
          > find cell cs_nnd3h*
          > hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
          > find cell cs nnd3w*
          > hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
          > find cell cs_nnd3y*
          > hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
          > hide -clear -cells { cs_nor2f cs_nor2w }
          > find cell cs_nor2f*
          > hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...
          > find cell cs_nor2w*
          > hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...
```

```
> hide -clear -cells { cs_nor3f cs_nor3h }
 > find cell cs_nor3f*
 > hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
 > find cell cs_nor3h*
 > hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
 > hide -clear -cells { cs_oa12f }
 > find cell cs_oa12f*
 > hide -clear -cells {cs_oa12f03b cs_oa12f03c cs_oa12f03d ...
 > hide -clear -cells { "cs_invvv" }
 > find cell cs invvv*
 > hide -clear -cells {cs invvv01b cs invvv01c cs invvv01d ...
 > hide -clear -cells { cs_ao12v cs_ao12g }
 > find cell cs_ao12v*
 > hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
 > find cell cs ao12g*
 > hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
 > hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
 > find cell cs_nnd2v*
 > hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
 > find cell cs_nnd2g*
 > hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
 > find cell cs nnd2x*
 > hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
 > hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
 > find cell cs nnd3v*
 > hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
> find cell cs_nnd3g*
 > hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
 > find cell cs_nnd3i*
 > hide -clear -cells {cs_nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
 > find cell cs_nnd3x*
 > hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
> find cell cs nnd3z*
 > hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
> hide -clear -cells { cs_nnd4v }
 > find cell cs nnd4v*
 > hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
 > hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
 > find cell cs nor2v*
 > hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
 > find cell cs_nor2g*
 > hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
 > find cell cs nor2x*
 > hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
 > hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
 > find cell cs_nor3v*
 > hide -clear -cells {cs_nor3v03b cs_nor3v03c cs_nor3v03d ...
 > find cell cs_nor3g*
 > hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...
 > find cell cs_nor3i*
 > hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
 > hide -clear -cells { cs_oa12v cs_oa12g }
 > find cell cs_oa12v*
 > hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
```

> find cell cs\_oa12g\*

```
> hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
      > init gain based repower REPOWER_INTERVAL(8)
Delays are given in units of 1.000000e-12 seconds
Fuzziness is 5.000000e-02[ET-0203]: Timing top level created for design: def_proto, analysis mode:
default.
      > str_parm unhide_rules
      > hide_def_with_view XPANDVIEW,SRULE
      > syn hide_boxes_clear
      > copy_hide
      > trulegen
[BD-502300]: Created 80 timing expansions.
      > traceset {syntrace HOWMANY}
[traceset]: trace string = syntrace HOWMANY
[tracing]: set trace variable syntrace to 20
      > setmaxfanout
      > set_maxarea
      > nextbox syn_hide_set(!HIDE_DOMINANT)
>>]: nextbox( syn_hide_set(!HIDE_DOMINANT) );
[syn hide set]: Rel 0.2 Compiled on Mar 10 1999 at 05:19:36.
[syn hide set]: Setting synthesis hide = 0, clear = 4
[syn_hide_set]: Number of boxes affected was 946.
       > write_end_point_report -points 10
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 21:58:28 1999
Part: IDCDSUC
                                     EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                  Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                               Max. Endpoints: 10
Sort Field: Slack
 Cause of Slack
                        Abbreviation Comparison/Description
                                    Slack due to a point downstream on path
                         SlkCont
 Slack Continuation
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                         RAT
 Required Arrival Time
                                         ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 Clock Gating Setup
                         ClkGSet
ARRIVAL TIME + ADJUST )
                                    ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                         CIkGHId
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                           CIKTPW
 Clock Tree Pulse Width
TRAILING EDGE )
                               ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 Setup
                     Setup
ADJUST)
                              ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 Hold
                    Hold
ADJUST)
                                   ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                       EndOfC
 EndOfCycle
ADJUST)
                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                         CIkPW
 ClockPulseWidth
TRAILING EDGE)
                                   ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
                         ClkSep
 ClockSeparation
```

ARRIVAL TIME + ADJUST ) Loop ALTest ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting **ATLimit** Slack discontinuity due to failed test Num/ LimitedAT/ Delay/ Failed Test/ Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adi NetName 1 dcd\_succ\_last\_t1 R C3+R 3242 -2243 3621 1011 1 PO 0 dcd\_succ\_last\_t1 RAT 999 ----> BOX714/OUT R C3+R 3242 -2243 3621 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1 ----> BOX714/IN R C3+R 3242 -2243 3621 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1&0 ----> C167/y\_\_ R C3+R 3242 -2243 3621 1011 1 cs\_invvn 01c NOT 0 dcd\_succ\_last\_t1&0 ----> C167/a FC3+R 1337 -2243 65 302 4 cs invvn 01c NOT 1906 N675 ---->{a} C2738/v F C3+R 1337 -2243 65 302 4 cs\_nnd2n 14c NAND 0 N675 ----> C2738/b R C3+R 1289 -2243 93 1261 4 cs\_nnd2n 14c NAND 48 dcd\_success&0 ----> C2734rwr/y R C3+R 1289 - -2243 93 1261 4 cs\_invvn 19c NOT 0 dcd\_success&0 ----> C2734rwr/a F C3+R 1236 -2243 40 310 1 cs\_invvn 19c NOT 53 N1097 ----> C2728rwr/y F C3+R 1236 -2243 40 310 1 cs\_invvn 16c NOT 0 N1097 ----> C2728rwr/a R C3+R 1205 -2243 84 181 2 cs\_invvn 16c NOT 31 N1692 .... ---->{b} C2725rwr/v " R C3+R 1205 -2243 84 181 2 cs\_nnd2n 13c NAND 0 N1692 ----> C2725rwr/a FC3+R 1148 -2243 98 161 2 cs\_nnd2n 13c NAND 57 N1479 1148 -2243 98 161 2 cs\_nnd3n 12c NAND ---->{c} C2721rwr/y FC3+R 0 N1479 ----> C2721rwr/a R C3+R 1085 -2243 184 115 2 cs\_nnd3n 12c NAND 63 N1497 ---->{d} C2709rwr/y R C3+R 1085 -2243 184 115 2 cs\_nor3n 10c NOR 0 N1497 ----> C2709rwr/c FC3+R 973 -2243 97 52 1 cs nor3n 10c NOR 112 N1976 ---->{e} C2579rwr\_0\_0/v FC3+R 973 -2243 52 1 cs\_nnd3n 07c NAND 97 0 N1976 ----> C2579rwr 0 0/b R C3+R 909 -2243 61 2 cs\_nnd3n 07c NAND 223 64 N127 ----> C2538/v R C3+R 909 -2243 223 61 2 cs\_invvn 01c NOT

FC3+R

FC3+R

785 -2243

785 -2243

85

85

16 1 cs\_invvn 01c NOT

16 1 cs\_nnd3n 02c NAND

124

N127

----> C2538/a

0 blk\_dcd\_in(0)

blk\_dcd\_in(0) ---->{f} C2480rwr/v

> C2480rwr/a	R C3+R	730 -2243	121	17 1 cs_nnd3n	02c NAND	
55 N393	11 00111	700 2210		,, , , , , , , , , , , , , , , , , , ,	02010012	
>{g} C2324/y	R C3+R	730 -2243	121	17 1 cs_nnd2n	02c NAND	
0 N393	E 00. D	641 0040	202	O1E G oo nadOn	OOO NIANID	
> C2324/b 89 N1728	F C3+R	.641 -2243	203	215 8 cs_nnd2n	UZC INAIND	
> C2224/y	F C3+R	641 -2243	203	215 8 cs_invvn	06c NOT	0
N1728						
> C2224/a	R C3+R	497 -2243	300	87 3 cs_invvn (	06c NOT	
144 N1371	D CO. D	407 0040	200	07 2 oc and2n	OSC NAND	
>{h} C2061/y 0 N1371	R C3+R	497 -2243	300	87 3 cs_nnd2n	UZC NAND	
> C2061/a	F C3+R	328 -2243	96 ·	124 4 cs_nnd2n	02c NAND	
169 dcd_cyl_cnt_q(0)						
> dcd_cyl_cnt.reg_n.lat_0/l2_o	ut_n F	C3+R 328	-2243	96 124 4 cl_	nnd2n 07c	
SRL 0 dcd_cyl_cnt_q(0)	В.С	o. 160 h		60 222 13 cl_nnc	12n 07c SRI	
> dcd_cyl_cnt.reg_n.lat_0/c2 168 slow_mode.c2_1	H C	3+ 160 l	<b>V/C</b>	00 222 13 01_11110	IZII U/C SILL	
> slow_mode.clockblock/c2	RO	3+ 160	N/C	60 222 13 cb_cl	k_32_1 LCB	
0 slow_mode.c2_1						
 2 dcd_succ_last_t1	F C3+B	2696 -169	97 212	24 1011 1 PO	0	
dcd_succ_last_t1	1 00111	2000 .00			_	
RAT	999			0 .		
> BOX714/OUT	F C3+	R 2696 -16	97 21	24 1011 1 IOPA	D IOPAD	
0 dcd_succ_last_t1	- E Ca. B		7 212	4 1011 1 IOPAD	: IOPAD	
> BOX714/IN 0 dcd_succ_last_t1&0	F U3+N	2090 -1097	. 212	- IOTT FIOPAD	IOFAD	
> C167/y	FC3+R	2696 -1697	2124	1011 1 cs_invvn	01c NOT	
0 dcd_succ_last_t1&0						
> C167/a	R C3+R	1240 -1697	97	302 4 cs_invvn	01c NOT	
1457 N675	D CO. D	1040 1607	07	302 4 cs_nnd2n	140 NAND	
>{a} C2738/y 0 N675	R C3+R	1240 -1697	97	302 4 CS_IIIUZII	14C NAIND	
> C2738/b	FC3+R	1179 -1697	56	1261 4 cs_nnd2n	14c NAND	
61 dcd_success&0						
> C2734rwr/y	FC3+R	1179 -1697	56	1261 4 cs_invvn	19c NOT	
0 dcd_success&0 > C2734rwr/a	R C3+R	1138 -1697	7 58	310 1 cs_invvn	19c NOT	
41 N1097	11 00+11	1100 1007	30	010 1 00	1001101	
> C2728rwr/y	R C3+R	1138 -1697	<sup>7</sup> 58	310 1 cs_invvn	16c NOT	
0 N1097				. 404 0 :	40- NOT	٠.
> C2728rwr/a	F C3+R	1099 -1697	61	181 2 cs_invvn	16C NOT	
39 N1692 >{b} C2725rwr/y	F C3+R	1099 -169	7 61	181 2 cs_nnd2i	n 13c NAND	
0 N1692	1 00111	1000 100		.0. 2 00		
> C2725rwr/a	R C3+R	1056 -1697	7 98	161 2 cs_nnd2r	13c NAND	
43 N1479						
>{c} C2721rwr/y	R C3+R	1056 -169	7 98	161 2 cs_nnd3	n 12c NAND	
0 N1479 > C2721rwr/a	F C3+R	992 -1697	86	115 2 cs_nnd3n	12c NAND	
64 N1497	i OUTN	332 -1031	00	. 10 2 00_1110011	120 17/110	
>{d} C2709rwr/y	FC3+R	992 -1697	7 86	115 2 cs_nor3n	10c NOR	
0 N1497						

 0  8:  N  bl	85 N127 > C2538/y N127 > C2538/a	R C3+F F C3+R F C3+R	8- 84				52 1 cs_nr	nd3n 07c NA	
 8:  N  bl	> C2579rwr_0_0/b 35 N127 > C2538/y N127 > C2538/a			12 -169	<del>)</del> 7 1:	31	61 2 cs nno	13n 070 NA	ND
 N  bl	> C2538/y \127 > C2538/a	F C3+R						ASH OVERNA	שמ
<b>N</b>  bl	N127 > C2538/a	F C3+R	842 -						
 bl	> C2538/a			-1697	131	61	2 cs_invvn	01c NOT	0
bl			_		,				
		R C3+R	752 -	-1697	96	16	1 cs_invvn	01c NOT	90
	olk_dcd_in(0)								
	>{f} C2480rwr/y	R C3+R	752	-1697	96	16	i 1 cs_nnd3r	n 02c NAND	<i>,</i>
	blk_dcd_in(0)				•	• • • •			
	> C2480rwr/a	F C3+R	688	-1697	90	17	1 cs_nnd3n	02c NAND	
	64 N393	_							
	>{g} C2324/y	F C3+R	688	-1697	90	17	1 cs_nnd2n	02c NAND	
	N393								
	> C2324/b	R C3+R	632 -	-1697	286	215	8 cs_nnd2n	02c NAND	)
	6 N1728								
		R C3+R	632 -	-1697	286	215	8 cs_invvn	06c NOT	. 0
	N1728								
	> C2224/a	F C3+R	452 -	-1697	212	87	3 cs_invvn	06c NOT	
	80 N1371								
		F C3+R	452	-1697	212	87	3 cs_nnd2n	02c NAND	
	N1371	٠							
		R C3+R	315 -	-1697	111	124	.4 cs_nnd2n	02c NAND	٠, .
	37 dcd_cyl_cnt_q(0)								
	> dcd_cyl_cnt.reg_n.lat_0/l2_out SRL	t_n RC	23+R	315 .	1697	7 1	11 124.40	:l_nnd2n _ 07	C
	GRL 0 dcd_cyl_cnt_q(0) > dcd_cyl_cnt.reg_n.lat_0/c2 55 slow mode c2 1	R C3	+ 1	160 N	1/C	60	222 13 cl nr	nd2n 07c SF	al
	> slow_mode.clockblock/c2	R C3	3+	160 1	N/C	- 60	222 13 cb (	alk 32 1 LC	R
0	slow_mode.c2_1							///	

3 local_milli_t2.reg_n.lat_0/a 46 N2054	FC3	+R 2888 -15	574 72 31 1 cl_invvn 07c SRL
Setup local_milli_t2.reg_n.lat_0/c 1200 slow_mode.c1_4	1 F(	C3- 160	60 238 14 cl_invvn 07c
> C3011/y N2054	FC3+R	2888 -1574	72 31 1 cs_invvn 07c NOT 0
> C3011/a 37 N73	R C3+R	2851 -1574	466 92 3 cs_invvn 07c NOT
>{a} C2794/y 0 N73	R <sub>.</sub> C3+R	2851 -1574	466 92 3 cs_ao12n 03c AOI
> C2794/a2 253 N1866	F C3+R	2598 -1574	157 18 1 cs_ao12n 03c AOI
>{b} C2555/y 0 N1866	F C3+R	2598 -1574	157 18 1 cs_ao12n 03c AOI
> C2555/b 109 iu_reset_op_c_t1&0	R C3+R	2489 -1574	3605 1044 3 cs_ao12n 03c AOI
>{c} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2489 -1574	3605 1044 3 cs_nnd2n 02c NAND
> C2393/a 2011 gbfonet_6	F C3+R	479 -1574	89 137 3 cs_nnd2n 02c NAND
> gbfocell_6/y	F C3+R	479 -1574	89 137 3 cs_invvn 09c NOT 0

gbfonet_6	
> gbfocell_6/a	R C3+R 416 -1574 201 43 1 cs_invvn 09c NOT
62 N2031	
>{d} C2162/y	R C3+R 416 -1574 201 43 1 cs_nnd3n 02c NAND
0 N2031	F CO. D. 1000 1574 57 40 0 co mod0n 1000 NAND
> C2162/c	F C3+R 303 -1574 57 49 3 cs_nnd3n 02c NAND
113 exc_cond_q	n F C3+R 303 -1574 57 49 3 cl_invvn 07d SRL
> exc_cond.reg_n.lat_0/l2_out_	U - 603+U 202 -1274 27 48 2 0 1 110411 674 2115
0 exc_cond_q	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
> exc_cond.reg_n.lat_0/c2 143 slow_mode.c2_4	// 004 100 140 00 200 14 01_111411 074 0112
> slow_mode.clockblock_3/c2	R C3+ 160 N/C 60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4	11007 100 140 00 200.77 02_000
<del></del>	
4 local_milli_t1.reg_n.lat_0/a	F C3+R 2888 -1574 72 31 1 cl_invvn 07c SRL
46 N2052	
Setup local_milli_t1.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	
> C3008/y	F C3+R 2888 -1574 72 31 1 cs_invvn 07c NOT 0
N2052	D. CO. D
> C3008/a	R C3+R 2851 -1574 466 92 3 cs_invvn 07c NOT
37 N73	R C3+R 2851 -1574 466 92 3 cs_ao12n 03c AOI
>{a} C2794/y	R C3+R 2851 -1574 466 92 3 cs_ao12n 03c AOI
0 N73 > C2794/a2	F C3+R 2598 -1574 157 18 1 cs_ao12n 03c AOI
253 N1866	1 00111 2000 1077 107 107 105 200 200 200 200 200 200 200 200 200 2
>{b} C2555/y	F C3+R 2598 -1574 157 18 1 cs_ao12n 03c AOI
0 N1866	
> C2555/b	R C3+R 2489 -1574 3605 1044 3 cs_ao12n 03c AOI
109 iu_reset_op_c_t1&0	···
>{c} C2393/y	R C3+R 2489 -1574 3605 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	
> C2393/a	F C3#Ŕ 479 -1574 89 137 3 cs_nnd2n 02c NAND 11
2011 gbfonet_6	F C3+R 479 -1574 89 137 3 cs_invvn 09c NOT 0
> gbfocell_6/y	P C3+M 4/9 -15/4 69 15/ 3 CS_IIIVVII 09C NOT 0
gbfonet_6 > gbfocell_6/a	R C3+R 416 -1574 201 43 1 cs_invvn 09c NOT
62 N2031	11 00411 410 1074 201 10 1 00_10011 000 110 1
>{d} C2162/y	R C3+R 416 -1574 201 43 1 cs_nnd3n 02c NAND
0 N2031	
> C2162/c	F C3+R 303 -1574 57 49 3 cs_nnd3n 02c NAND
113 exc cond a	
> exc_cond.reg_n.lat_0/l2_out_	n F C3+R 303 -1574 57 49 3 cl_invvn 07d SRL
0 exc_cond_q	
> exc_cond.reg_n.lat_0/c2	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
143 slow_mode.c2_4	D 00 400 N/O 00 000 44 -b -dl- 00 4 LOD
	R C3+ 160 N/C 60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4	
5 local milli reg n lat 0/a	F C3+R 2888 -1574 72 31 1 cl_invvn 07c SRL
46 N2040	
Setup local_milli.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c 1200
slow_mode.c1_2	
·	

> C2962/y N2040	F C3+R 2888 -1574 72 31 1 cs_invvn 07c NOT 0
> C2962/a	R C3+R 2851 -1574 466 92 3 cs_invvn 07c NOT
37 N73	
>{a} C2794/y 0 N73	R C3+R 2851 -1574 466 92 3 cs_ao12n 03c AOI
> C2794/a2 253 N1866	F C3+R 2598 -1574 157 18 1 cs_ao12n 03c AOI
>{b} C2555/y 0 N1866	F C3+R 2598 -1574 157 18 1 cs_ao12n 03c AOI
> C2555/b 109 iu_reset_op_c_t1&0	R C3+R 2489 -1574 3605 1044 3 cs_ao12n 03c AOI
>{c} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2489 -1574 3605 1044 3 cs_nnd2n 02c NAND
> C2393/a 2011 gbfonet_6	F C3+R 479 -1574 89 137 3 cs_nnd2n 02c NAND
> gbfocell_6/y	F C3+R 479 -1574 89 137 3 cs_invvn 09c NOT 0
gbfonet_6 > gbfocell_6/a	R C3+R 416 -1574 201 43 1 cs_invvn 09c NOT
62 N2031 >{d} C2162/y	R C3+R 416 -1574 201 43 1 cs_nnd3n 02c NAND
0 N2031 > C2162/c	F C3+R 303 -1574 57 49 3 cs_nnd3n 02c NAND
113 exc_cond_q > exc_cond.reg_n.lat_0/l2_out_	n F C3+R 303 -1574 57 49 3 cl_invvn 07d SRL
U exc_cona_q	
> _exc_cond.reg_n.lat_0/c2 143 slow_mode.c2_4	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
> slow_mode.clockblock 3/c2	R C3+ 160 N/C 60 239 14 cb_clk_32_1 LCB
6 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2489 -1490 3605 1011 1 PO 0
	999
> BOX716/OUT	R C3+R 2489 -1490 3605 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1 > BOX716/IN 0 iu_reset_op_c_t1&0	R C3+R 2489 -1490 3605 1044 3 IOPAD IOPAD
>{a} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2489 -1574 3605 1044 3 cs_nnd2n 02c NAND
> C2393/a 2011 gbfonet_6	F C3+R 479 -1574 89 137 3 cs_nnd2n 02c NAND
> gbfocell_6/y gbfonet_6	F C3+R 479 -1574 89 137 3 cs_invvn 09c NOT 0
> gbfocell_6/a 62 N2031	R C3+R 416 -1574 201 43 1 cs_invvn 09c NOT
>{b} C2162/y 0 N2031	R C3+R 416 -1574 201 43 1 cs_nnd3n 02c NAND
> C2162/c 113 exc_cond_q	F C3+R 303 -1574 57 49 3 cs_nnd3n 02c NAND
> exc_cond.reg_n.lat_0/l2_out_r 0 exc_cond_q	n F C3+R 303 -1574 57 49 3 cl_invvn 07d SRL
> exc_cond.reg_n.lat_0/c2 143 slow_mode.c2_4	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL

7 local_milli_t2.reg_n.lat_0/a	R C3+	·R 2832 -14	69 88 31 1 cl_invvn 07c SRL
-3 N2054			0004445
Setup local_milli_t2.reg_n.lat_0/c1	FC	3- 160	60 238 14 cl_invvn 07c
1200 slow_mode.c1_4			an at the ATL NOT O
> C3011/y	R C3+R	2832 -1469	88 31 1 cs_invvn 07c NOT 0
N2054			000 00 0 1 1 1 1 0 To NOT
> C3011/a	F C3+R	2771 -1469	263 92 3 cs_invvn 07c NOT
62 N73			000 00 0 100 000 101
>{a} C2794/y	FC3+R	2771 -1469	263 92 3 cs_ao12n 03c AOI
0 N73			07 47 440- 00- 401
> C2794/b	R C3+R	2604 -1469	87 17 1 cs_ao12n 03c AOI
166 N1988	5.00.5	0004 4400	07 47 4 so mmd0n 00s NAND
>{b} C2748/y	R C3+R	2604 -1469	87 17 1 cs_nnd2n 02c NAND
0 N1988	5 00 D	0540 4400	00 17 1 co nod0o 00o NAND
> C2748/a	F C3+R	2546 -1469	92 17 1 cs_nnd2n 02c NAND
58 N639	E 00 - D	2546 -1469	92 17 1 cs_nnd2n 02c NAND
>{c} C2466/y	F C3+R	2546 -1469	92 17 1 CS_INICEN OF TAND
0 N639	D CO. D	2490 1460	3605 1044 3 cs_nnd2n 02c NAND
> C2466/b	R C3+R	2409 - 1409	3003 1044 3 CS_IIIdZII 02C 14/142
57 iu_reset_op_c_t1&0	R C3+R	2480 -1574	3605 1044 3 cs_nnd2n 02c NAND
>{d} C2393/y	n Co+n	2403 -1374	3003 1044 0 03_IIIIdZII 02010 010
0 iu_reset_op_c_t1&0 > C2393/a	F C3+R	479 -1574	89 137 3 cs_nnd2n 02c NAND
2011 gbfonet_6	1 00111	470 . 1077	
> gbfocell_6/y	F C3+R	479 -1574	89 137 3 cs_invvn 09c NOT 0
gbfonet_6	. 00		
> gbfocell_6/a	R C3+R	416 -1574	201 43 1 cs_invvn 09c NOT
62 N2031			
>{e} C2162/y	R C3+R	416 -1574	201 43 1 cs_nnd3n 02c NAND
0 N2031			
> C2162/c	F C3+R	303 -1574	57 49 3 cs_nnd3n 02c NAND
113 exc_cond_q			·
> exc_cond.reg_n.lat_0/l2_out_	n F	C3+R 303	-1574 57 49 3 cl_invvn 07d SRL
0 exc_cond_q			
> exc_cond.reg_n.lat_0/c2	RC	3+ 160 N	I/C 60 239 14 cl_invvn 07d SRL
143 slow_mode.c2_4	_		
> slow_mode.clockblock_3/c2	R	C3+ 160	N/C 60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4			
0.5 1 20° 44 man in 144 0/a	П СО	.D 2022 1/	469 88 31 1 cl_invvn 07c SRL
8 local_milli_t1.reg_n.lat_0/a	R C3	+H 2002 -12	109 66 31 1 CI_IIIVVII 07C 311E
-3 N2052	E (	C3- 160	60 238 14 cl_invvn 07c
Setup local_milli_t1.reg_n.lat_0/c1	г	J3* 100	00 200 14 CI_IIIVVII 07C
1200 slow_mode.c1_4	R C3+R	2832 -1469	88 31 1 cs_invvn 07c NOT 0
> C3008/y	n ostn	~002 -1403	00 01 1 00_1110711 0701101
N2052 > C3008/a	F C3+R	2771 -1469	263 92 3 cs_invvn 07c NOT
62 N73	i OUTII	_,,, 1 1700	
>{a} C2794/y	F C3+R	2771 -1469	263 92 3 cs_ao12n 03c AOI
0 N73	. 55	2	
> C2794/b	R C3+R	2604 -1469	87 17 1 cs_ao12n 03c AOI

100 111000	
166 N1988	
>{b} C2748/y	R C3+R 2604 -1469 87 17 1 cs_nnd2n 02c NAND
0 N1988	
> C2748/a	F C3+R 2546 -1469 92 17 1 cs_nnd2n 02c NAND
58 N639	÷
>{c} C2466/y	F C3+R 2546 -1469 92 17 1 cs_nnd2n 02c NAND
0 N639	
> C2466/b	R C3+R 2489 -1469 3605 1044 3 cs_nnd2n 02c NAND
57 iu_reset_op_c_t1	80
>{d} C2393/y	R C3+R 2489 -1574 3605 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t18	k0
> C2393/a	F C3+R 479 -1574 89 137 3 cs_nnd2n 02c NAND
2011 gbfonet_6	
> gbfocell_6/y	F C3+R 479 -1574 89 137 3 cs_invvn 09c NOT 0
gbfonet_6	
> gbfocell_6/a	R C3+R 416 -1574 201 43 1 cs_invvn 09c NOT
62 N2031	10 100_01011 000_01001
>{e} C2162/y	R C3+R 416 -1574 201 43 1 cs_nnd3n 02c NAND
0 N2031	TO THE TOTAL TO THE TOTA
> C2162/c	F C3+R 303 -1574 57 49 3 cs_nnd3n 02c NAND
113 exc_cond_q	020 MAN
> exc_cond.reg	_n.lat_0/l2_out_n
o exc_cona_q	en e
> exc_cond.reg	_n.lat_0/c2 R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
143 Slow mode,c2 4	
> slow mode.clo	ockblock 3/c2 P.C31 160 N/C so conditable to
0 slow_mode.c2_4	_ 100 100 00 200 14 CD_CIK_02_1 LOB
en e	n.lat 0/a B C3+B 2832 -1469 88 31 1 d inter 075 CD
-3 N2040	77 30111 2002 1403 00 31 1 CLINVII U/C SHE
Setup local_milli.reg slow_mode.c1_2	g_n.lat_0/c1

9 local_milli.reg_n.lat_0/a -3 N2040	R C3+R 2	2832 -146	69 88 31 1 cl_invvn 07c SRL
Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2	F C3-	160	60 238 14 cl_invvn 07c 1200
> C2962/y N2040	R C3+R 283	2 -1469	88 31 1 cs_invvn 07c NOT 0
> C2962/a 62 N73	F C3+R 277	1 -1469	263 92 3 cs_invvn 07c NOT
>{a} C2794/y 0 N73	F C3+R 277	71 -1469	263 92 3 cs_ao12n 03c AOI
> C2794/b 166 N1988	R C3+R 260	4 -1469	87 17 1 cs_ao12n 03c AOI
>{b} C2748/y 0 N1988	R C3+R 260	04 -1469	87 17 1 cs_nnd2n 02c NAND
> C2748/a 58 N639	F C3+R 2546	6 -1469	92 17 1 cs_nnd2n 02c NAND
>{c} C2466/y 0 N639	F C3+R 254	6 -1469	92 17 1 cs_nnd2n 02c NAND
> C2466/b 57 iu_reset_op_c_t1&0	R C3+R 2489	9 -1469	3605 1044 3 cs_nnd2n 02c NAND
>{d} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 248	39 -1574	3605 1044 3 cs_nnd2n 02c NAND
> C2393/a 2011 gbfonet_6	F C3+R 479	-1574	89 137 3 cs_nnd2n 02c NAND
> gbfocell_6/y gbfonet_6	F C3+R 479	-1574	89 137 3 cs_invvn 09c NOT 0

```
43 1 cs_invvn 09c NOT
                            R C3+R
                                     416 -1574 201
----> gbfocell_6/a
62 N2031
                                                     43 1 cs_nnd3n 02c NAND
                            R C3+R
                                     416 -1574
                                                201
---->{e} C2162/y
0 N2031
                                               57 49 3 cs_nnd3n 02c NAND
                           F C3+R . 303 -1574
----> C2162/c
113 exc_cond_q
                                                      57 49 3 cl_invvn 07d SRL
                                F C3+R
                                           303 -1574
----> exc_cond.reg_n.lat_0/l2_out_n
0 exc_cond_q
                                        160 N/C
                                                   60 239 14 cl_invvn 07d SRL
                                R C3+
---> exc cond.reg_n.lat_0/c2
143 slow_mode.c2_4
                                R C3+
                                          160 N/C
                                                     60 239 14 cb_clk_32_1 LCB
----> slow_mode.clockblock_3/c2
0 slow_mode.c2_4
                            R C3+R 2126 -1127 3605 1011 1 PO
                                                                         0
  10 idcdsuc_err
N146
                               999
                                                           0
RAT
                                       2126 -1127 3605 1011 1 IOPAD
                                                                       IOPAD
                              R C3+R
----> BOX750/OUT
0 N146
                             R C3+R 2126 -1127 3605 1011 1 IOPAD
---> BOX750/IN
0 N146&0
                                    2126 -1127 3605 1011 1 cs_invvn 01c NOT
                            R C3+R
----> C2082/v
0 N146&0
                                                48 32 2 cs_invvn 01c NOT
                            F C3+R
                                     295 -1127
----> C2082/a
1831 dcdsuc_err_q
                                                      48 32 2 cl_nnd2n 07c
                                           295 -1127
                                  FC3+R
----> dcdsuc_err.reg_n.lat_0/l2_out_n
       0 dcdsuc_err_q
SRL
----> dcdsuc_err.reg_n.lat_0/c2
                                                    60 222 13 cl_nnd2n 07c-SRL
                               R C3+
                                         160 N/C
135 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+
                                                  60 222 13 cb_clk_32_1 LCB
                                         160 N/C
0 slow_mode.c2_1
> measure
[levelize][get_ltor]: number of levels = 19
 The model <IDCDSUC> has:
```

122 Primary Inputs = 73 Primary Outputs = Primary BIDIs = 0 1167 Signals 946 Gate Count 1783 Connections Master REG Bits = 83 Slave REG Bits 83 4487 Internal Area External Area 0 0.530566 Gates/Connects = Fanout Count 1783 Average Fanout = 1.527849 Avg Tech Box Size = 4.743129 Tech Box Size Stddev = 0.010329 0.000000 Power =

<sup>\*\*\*</sup>R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\*

```
792
 Real boxes
                             571
 Real connections
                               1408
 Real LSTs
                             2200
                 =
 Real ICells/box
                           7.858144
 Real LSTs/box
                            3.852890
                   =
 Real nets/box
                           1.387040
 Cell
               Total
 Each
                Cell
Type Cnt Boxname
                                Power Level Function
                                                        Int Ext
                                                                  Power
                                                                          Int
                                                                               Ext
                                                                                    Power
  7
      cs_ao22n03c
                                 03c
                                             AOI
                                                    6
                                                           0:000
                                                                    42
                                       >
                                                        0
                                                                          0
                                                                             0.000
  5
      cs ao12n03c
                                 03c
                                       >
                                             AOI
                                                    4
                                                        0
                                                            0.000
                                                                    20
                                                                          0
                                                                             0.000
  1
      cs_ao22n10c
                                 10c
                                             AOI
                                                   18
                                                         0
                                       >
                                                            0.000
                                                                    18
                                                                          0
                                                                              0.000
 180
       BRKPT
                                    >
                                         BRKPT
                                                   0
                                                        0
                                                           0.000
                                                                    0
                                                                         0
                                                                            0.000
       IOPAD
 195
                                    >
                                         IOPAD
                                                   0
                                                       0
                                                           0.000
                                                                   0
                                                                        0
                                                                           0.000
 166
       cs_nnd2n02c
                                  02c
                                             NAND
                                                       3
                                        >
                                                           0
                                                              0.000
                                                                      498
                                                                             0
                                                                               0.000
 24
       cs nnd3n02c
                                 02c
                                             NAND
                                       >
                                                      4
                                                           0
                                                              0.000
                                                                      96
                                                                            0
                                                                               0.000
  3
      cs_nnd2n05c
                                            NAND
                                05c
                                                      4
                                       >
                                                          0
                                                             0.000
                                                                      12
                                                                           0
                                                                               0.000
  6
      cs_nnd4n03c
                                03c
                                       >
                                            NAND
                                                     5
                                                          0
                                                             0.000
                                                                      30
                                                                           0
                                                                               0.000
  4
      cs_nnd2n13c
                                 13c
                                       >
                                            NAND
                                                     15
                                                          0
                                                              0.000
                                                                      60
                                                                               0.000
                                                                            0
  3
      cs nnd2n04c
                                04c
                                       >
                                            NAND
                                                     3
                                                          0
                                                             0.000
                                                                      9
                                                                           0
                                                                              0.000
  2
      cs_nnd3n07c
                                07c
                                       >
                                            NAND
                                                     6
                                                          0
                                                             0.000
                                                                      12
                                                                           0
                                                                               0.000
  3
      cs_nnd2n03c
                                03c
                                            NAND
                                       >
                                                     3
                                                          0
                                                             0.000
                                                                      9
                                                                           0
                                                                              0.000
  1
      cs_nnd2n12c
                                12c
                                            NAND
                                                     12
                                                          0
                                       >
                                                             0.000
                                                                      12
                                                                            0
                                                                               0.000
 2
      cs_nnd2n14c
                                14c
                                            NAND
                                       >
                                                     19
                                                          0
                                                              0.000
                                                                      38
                                                                            0
                                                                               0.000
  1
      cs_nnd3n12c
                                12c
                                       >
                                            NAND
                                                     22
                                                          0
                                                              0.000
                                                                      22
                                                                            0
                                                                               0.000
  1
      cs nnd4n09c
                                09c
                                       >
                                            NAND
                                                     16
                                                              0.000
                                                          0
                                                                      16
                                                                            0
                                                                               0.000
 4
      cs_nnd2n07c
                                07c
                                      . >
                                            NAND
                                                          0
                                                     4
                                                             0.000
                                                                      16
                                                                           0
                                                                               0.000
  1
      cs_nnd2n11c
                                11c
                                            NAND
                                                          0
                                       >
                                                     11
                                                              0.000
                                                                      11
                                                                            0
                                                                               0.000
  1
      cs_nnd2n06c
                                06c
                                            NAND
                                                     4
                                                          0
                                       >
                                                             0.000
                                                                      4
                                                                           0
                                                                              0.000
 1
      cs_nnd3n09c
                                09c
                                            NAND
                                                     12
                                       >
                                                          0
                                                             0.000
                                                                      12
                                                                               0.000
 10
      cs_nor2n02c
                                02c
                                             NOR.
                                                     3
                                                         0
                                                            0.000
                                                                     30
                                                                           0
                                                                              0.000
 1
      cs_nor3n03c
                                03c
                                      >
                                            NOR
                                                    4
                                                            0.000
                                                         0
                                                                     4
                                                                         0
                                                                             0.000
 1
      cs_nor2n12c
                                12c
                                            NOR
                                                    12
                                                            0.000
                                                                     12
                                      >
                                                         0
                                                                          0
                                                                              0.000
 2
      cs_nor2n04c
                                04c
                                            NOR
                                                    3
                                      >
                                                         0
                                                            0.000
                                                                     6
                                                                         0
                                                                             0.000
 1
      cs_nor3n10c
                                10c
                                            NOR
                                                   12
                                      >
                                                         0
                                                            0.000
                                                                     12
                                                                          0
                                                                              0.000
102
       cs_invvn01c
                                01c
                                            NOT
                                                    2
                                      >
                                                         0
                                                            0.000
                                                                    204
                                                                           0
                                                                              0.000
 5
      cs_invvn11c
                               11c
                                           NOT
                                                   6
                                                        0
                                                                            0.000
                                     >
                                                           0.000
                                                                   30
                                                                         0
 6
      cs invvn10c
                               10c
                                           NOT
                                                        0
                                                           0.000
                                     >
                                                   4
                                                                   24
                                                                         0
                                                                             0.000
 21
      cs invvn12c
                                12c
                                            NOT
                                                    6
                                      >
                                                        0
                                                           0.000
                                                                   -126
                                                                          0
                                                                             0.000
 7
      cs invvn09c
                               09c
                                     >
                                           NOT
                                                   4
                                                        0
                                                           0.000
                                                                   28
                                                                         0
                                                                             0.000
 33
      cs_invvn07c
                                07c
                                      >
                                            NOT
                                                    2
                                                        0
                                                            0.000
                                                                    66
                                                                          0
                                                                             0.000
 4
      cs_invvn15c
                               15c
                                           NOT
                                                   10
                                                        0
                                     >
                                                            0.000
                                                                    40
                                                                          0
                                                                             0.000
 9
      cs_invvn06c
                               06c
                                                   2
                                     >
                                           NOT
                                                        0
                                                           0.000
                                                                   18
                                                                         0
                                                                             0.000
 13
      cs_invvn05c
                               05c
                                            NOT
                                                        0
                                                            0.000
                                                                    26
                                                                         0
                                                                             0.000
 4
      cs_invvn13c
                               13c
                                     >
                                           NOT
                                                   8
                                                        0
                                                           0.000
                                                                   32.
                                                                         0
                                                                            0.000
 3
      cs_invvn08c
                               08c
                                     >
                                           NOT
                                                   4
                                                        0
                                                           0.000
                                                                   12
                                                                         0
                                                                            0.000
 7
      cs_invvn02c
                               02c
                                     >
                                           NOT
                                                   2
                                                        0
                                                           0.000
                                                                   14
                                                                         0
                                                                            0.000
 1
      cs_invvn14c
                               14c
                                     >
                                           NOT
                                                   8
                                                        0
                                                           0.000
                                                                    8
                                                                        0
                                                                            0.000
 5
      cs_invvn04c
                               04c
                                           NOT
                                                   2
                                                        0
                                     >
                                                           0.000
                                                                   10
                                                                         0
                                                                            0.000
 1
      cs_invvn18c
                               18c
                                     >
                                           NOT
                                                   20
                                                        0
                                                           0.000
                                                                    20
                                                                         0
                                                                             0.000
 3
      cs invvn16c
                               16c
                                     >
                                           NOT
                                                   14
                                                        0
                                                           0.000
                                                                    42
                                                                         0
                                                                             0.000
 1
      cs invvn19c
                               19c
                                           NOT
                                     >
                                                   25
                                                        0
                                                           0.000
                                                                    25
                                                                         0
                                                                             0.000
 1
      cs_oa21n04c
                                04c
                                            OAL
                                                   5
                                                        0
                                                           0.000
                                                                    5
                                                                        0
                                                                            0.000
```

Real signals

=

```
0.000
                                               0.000
                           03c
                                     OAI
                                           6
                                                          6
    cs_oa22n03c
                                >
1
                                                              0.000
                           05c
                                     OAL
                                           8
                                               0
                                                  0.000
                                                          8
    cs_oa21n05c
                               >
1
                                     REG
                                           25
                                                0
                                                   0.000
                                                         550
                                                               0
                                                                  0.000
    cl_invvn07c
                          07c
22
                               >
                                                         750
                                                                0.000
                                     REG
                                           25
                                                0
                                                   0.000
    cl_invvn07d
                          07d
                                >
30
                                                                0.000
                                     REG
                                           26
                                                   0.000
                                                          468
    cl_nnd2n07c
                           07c
                                >
                                                0
18
                                                   0.000
                                                          264
                                                                0.000
                                     REG
                                           33
                                                0
    cl_ao22n07c
                          07c
8
                                >
                                                          58
                                                               0
                                                                  0.000
                                     REG
                                           29
                                                0
                                                   0.000
    cl_nnd3n07c
                          07c
2
                                >
                                                   0.000
                                                          26
                                                               0
                                                                  0.000
                                    REG
                                           26
                                                0
                          06c
1
    ci nor2n06c
                               >
                                                               0
                                                                  0.000
                                                  0.000
                                                          30
                                     REG
                                           30
                                                0
1
    cl_ao21n07c
                          07c
                                >
                                                          30
                                                               0
                                                                  0.000
                                     REG
                                           30
                                                0
                                                   0.000
    cl oa21n07c
                          07c
1
                                                     0.000
                                                               70
                                                                    0.000
                                                70
                               > SEQUENTIAL
    cb_mode_block
1
                                                   0 0.000 480
                                                                   0.000
                              > SEQUENTIAL
                                             80
    cb_clk_32_1
6
                                                                0
                                                                  0.000
                                     XNOR
                                             8
                                                 0
                                                    0.000
                                                            8
                           01b
1
    cs_xbn2n01b
                                >
                                                   0.000
                                                                  0.000
                                     XOR
                                            8
                                                0
                                                           8
                                                               0
    cs_xbo2n01d
                           01d
1
```

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

#	of	
Level	s Outp	out
0	1	*
1	55	50* plus *****
2	1	*
2	8 -	*****
4	1	*
10	3	***
. 11	. 1	*
12	1	*
14	·· 2	**

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
        7
 0
 2
        20
 3
        1
  4
        5
        2
  5
        6
  6
  7
        4
  8
        4
  9
         1
 10
         6
 12
         1
 14
         1
 15
         5
 16
         4
         7
 17
         2
 18
 19
         14
```

The Histogram Of Fanin vs. Box

```
# of
Fanin
        Ops
       405
              400* plus *****
  1
  2
       203
              200* plus ***
  3
       37
  4
        16
The Histogram Of Fanout vs. Net
   # of
Fanout Nets
       964
              950* plus ***
  1
  2
       102
              100* plus **
  3
       39
  4
       17
 5
        8
 6
       11
        2
 7
 8
        4
 13
        3
 14
        16
 15
[End of measure]
[measure]: Execution time was 0.5 seconds.
       > randsim q -
>>]: randsim(q);
       > checksrc
[BD-40000]: checksrc CMVC version 1.27 compiled on Apr 13 1999 at 18:00:56
[BD-40132]: Network IDCDSUC has no potential problems.
      > is_parm new_assert
        > set_slew_prop OFF
[set_slew_prop]: Setting slew propagation to 0 (OFF)
        > tc_parm CHK_SINKSLEW(N)
[tc_parm]: CMVC version 1.26.2.1 compiled on Apr 1 1999 at 05:20:31.
       > tc_parm {PINTYPE(OUTPUT_PIN),OFFSET(0) MARGIN(0),ATTEMPT...
        > tc_parm USE_AREA,BENEFIT_UNITS(0)
[tc_parm]: benefit units factor is 0.0002
       > measure
[levelize][get_ltor]: number of levels = 19
The model <IDCDSUC> has:
 Primary Inputs
                              122
 Primary Outputs
                               73
 Primary BIDIs
                               0
 Signals
                           1167
 Gate Count
                            946
 Connections
                             1783
 Master REG Bits
                                83
 Slave REG Bits
                               83
 Internal Area
                            4487
```

```
0
External Area
                           0.530566
Gates/Connects
Fanout Count
                            1783
                           1.527849
Average Fanout
                            4.743129
Ava Tech Box Size
Tech Box Size Stddev =
                             0.010329
                       0.000000
Power
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
                            792
Real signals
                =
                            571
Real boxes
                              1408
Real connections
                            2200
Real LSTs
                          7.858144
Real ICells/box
                           3.852890
Real LSTs/box
                  =
                          1.387040
Real nets/box
               Total
Cell
                Cell
Each
                                                                        Int Ext Power
                                                          Ext Power
                               Power Level Function
                                                       Int
Type Cnt Boxname
                                                                           0.000
                                                       0
                                                          0.000
                                                                   42
                                                                        0
                                            AOI
                                                   6
  7
      cs_ao22n03c
                                03c
                                      >
                                                                           0.000
                                            AOI
                                                   4
                                                       0
                                                          0.000
                                                                   20
                                                                        0
  5
      cs ao12n03c
                                03c
                                      >
                                                                            0.000
                                                                         0
                                                  18
                                                        0
                                                           0.000
                                                                   18
      cs_ao22n10c
                                10c
                                      >
                                            AOI
  1
                                                                       0
                                                                          0.000
                                        BRKPT
                                                       0
                                                          0.000
                                                                   0
       BRKPT
                                                  0
 180
                                   >
                                                                          0.000
                                        IOPAD
                                                         0.000
                                                                  0
                                                                      0
 195
       IOPAD
                                                 0
                                                      0
                                                                               0.000
                                                                     498
 166
       cs_nnd2n02c
                                 02c
                                       >
                                            NAND
                                                     3
                                                          0
                                                             0.000
                                                                            0
                                                                             0.000
                                                                          0
                                02c
                                            NAND
                                                     4
                                                         0
                                                             0.000
                                                                     96
       cs_nnd3n02c
 24
                                                                          0.000
                                05c
                                           NAND
                                                    4
                                                         0
                                                            0.000
                                                                    12
  3
      cs nnd2n05c
                                      >
                                                                             0.000
                                03c
                                      >
                                           NAND
                                                    5
                                                         0
                                                            0.000
                                                                    30
                                                                          0
  6
      cs_nnd4n03c
                                                                          0
                                                                             0.000
                                13c
                                           NAND
                                                    15
                                                         0
                                                             0.000
                                                                     60
                                      >
      cs_nnd2n13c
  4
                                                                             0.000
                                           NAND
                                                    3
                                                         0
                                                            0.000
                                                                     9
                                                                         0
                                04c
  3
      cs nnd2n04c
                                      >
                                                                             0.000
                                                    6
                                                         0
                                                            0.000
                                                                    12
                                                                          0
                                07c
                                      >
                                           NAND
  2
      cs nnd3n07c
                                           NAND
                                                    3
                                                         0
                                                            0.000
                                                                     9
                                                                         0
                                                                             0.000
                                03c
                                      >
  3
      cs_nnd2n03c
                                                         0
                                                             0.000
                                                                     12
                                                                          0
                                                                              0.000
                                           NAND
                                                    12
                                12c
      cs_nnd2n12c
                                      >
  1
                                                                     38
                                                                           0
                                                                              0.000
                                                          0
                                                             0.000
                                14c
                                      >
                                           NAND
                                                    19
  2
      cs_nnd2n14c
                                                                     22
                                                    22
                                                          0
                                                             0.000
                                                                           0
                                                                              0.000
                                12c
                                           NAND
      cs_nnd3n12c
                                      >
  1
                                                                           0
                                                                              0.000
                                                         0
                                                             0.000
                                                                     16
                                           NAND
                                                    16
      cs nnd4n09c
                                09c
                                      >
  1
                                                                             0.000
                                                                     16
                                                                          0
                                                         0
                                                            0.000
      cs_nnd2n07c
                                07c
                                      >
                                           NAND
                                                     4
  4
                                                                              0.000
                                           NAND
                                                          0
                                                             0.000
                                                                     11
                                                                           0
                                11c
                                      >
                                                    11
      cs_nnd2n11c
                                                                             0.000
                                            NAND
                                                     4
                                                         0
                                                            0.000
                                                                     4
                                                                          0
                                06c
                                      >
  1
      cs nnd2n06c
                                                    12
                                                          0
                                                             0.000
                                                                     12
                                                                           0
                                                                              0.000
                                09c
                                      >
                                            NAND
      cs_nnd3n09c
  1
                                                         0
                                                            0.000
                                                                    30
                                                                          0
                                                                             0.000
                                02c
                                            NOR
                                                    3
       cs nor2n02c
                                      >
  10
                                                                            0.000
                                                           0.000
                                                                    4
                                                                        0
                                                   4
                                                        0
       cs nor3n03c
                                03c
                                      >
                                            NOR
  1
                                                                    12
                                                                          0.000
                                                   12
                                                         0
                                                            0.000
      cs_nor2n12c
                                12c
                                      >
                                            NOR
  1
                                                        0
                                                           0.000
                                                                    6
                                                                        0
                                                                            0.000
                                04c
                                      >
                                            NOR
                                                   3
  2
       cs nor2n04c
                                                   12
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
                                            NOR
                                                         0
       cs nor3n10c
                                10c
                                      >
  1
                                                                   204
                                            NOT
                                                    2
                                                        0
                                                            0.000
                                                                          0.000
                                01c
 102
        cs_invvn01c
                                                   6
                                                       0
                                                           0.000
                                                                   30
                                                                        0
                                                                            0.000
                                           NOT
  5
       cs invvn11c
                               11c
                                     >
                                                           0.000
                                                                   24
                                                                        0
                                                                            0.000
                                                   4
                                                       0
  6
       cs_invvn10c
                               10c
                                     >
                                           NOT
                                                                   126
                                                                         0.000
                                12c
                                      >
                                            NOT
                                                   6
                                                        0
                                                           0.000
  21
       cs_invvn12c
                                                                            0.000
                                           NOT
                                                   4
                                                       0
                                                           0.000
                                                                   28
                                                                        0
                               09c
  7
       cs invvn09c
                                     >
                                                                            0.000
                                                   2
                                                        0
                                                           0.000
                                                                   66
                                                                         0
                                07c
                                            NOT
  33
       cs_invvn07c
                                      >
                                                        0
                                                           0.000
                                                                   40
                                                                         0
                                                                            0.000
                                           NOT
                                                   10
                               15c
  4
       cs invvn15c
                                     >
                                                           0.000
                                                                   18
                                                                        0
                                                                            0.000
                                                   2
                                                        0
                                           NOT
  9
       cs invvn06c
                               06c
                                      >
                                                   2
                                                                   26
                                                                         0
                                                                            0.000
                                            NOT
                                                        0
                                                           0.000
       cs invvn05c
                                05c
                                      >
  13
```

```
4
    cs_invvn13c
                           13c
                                      NOT
                                >
                                             8
                                                 0
                                                    0.000
                                                           32
                                                                0
                                                                   0.000
3
    cs_invvn08c
                           08c
                                >
                                      NOT
                                             4
                                                 0
                                                    0.000
                                                           12
                                                                0
                                                                   0.000
7
    cs_invvn02c
                           02c
                                >
                                      NOT
                                             2
                                                 0
                                                    0.000
                                                           14
                                                                0
                                                                   0.000
1
    cs_invvn14c
                           14c
                                >
                                      NOT
                                             8
                                                 0
                                                    0.000
                                                           8
                                                                0.000
5
    cs_invvn04c
                           04c
                                >
                                             2
                                      NOT
                                                 0
                                                    0.000
                                                           10
                                                                0
                                                                   0.000
1
    cs_invvn18c
                           18c
                                                 0
                                >
                                      NOT
                                            20
                                                    0.000
                                                           20
                                                                 0.000
3
    cs_invvn16c
                           16c
                                      NOT
                                >
                                            14
                                                 0
                                                    0.000
                                                            42
                                                                 0.000
1
    cs_invvn19c
                           19c
                                      NOT
                                            25
                                                 0
                                                    0.000
                                                           25
                                                                 0.000
1
    cs_oa21n04c
                            04c
                                 >
                                      OAI
                                             5
                                                    0.000
                                                 0
                                                            5
                                                                0.000
1
    cs_oa22n03c
                            03c
                                      OAI
                                             6
                                                    0.000
                                                 0
                                                            6
                                                                0.000
1
    cs_oa21n05c
                            05c
                                      OAI
                                             8
                                                 0
                                                    0.000
                                 >
                                                           8
                                                                0.000
22
    cl invvn07c
                           07c
                                      REG
                                >
                                            25
                                                 0
                                                    0.000
                                                           550
                                                                 0.000
30
    cl_invvn07d
                           07d
                                      REG
                                            25
                                                 0
                                                    0.000
                                                           750
                                                                 0
                                                                    0.000
18
                                      REG
    cl_nnd2n07c
                           07c
                                 >
                                             26
                                                  0
                                                    0.000
                                                           468
                                                                  0
                                                                    0.000
8
    cl_ao22n07c
                           07c
                                >
                                      REG
                                            33
                                                 0
                                                     0.000
                                                           264
                                                                 0.000
2
    cl_nnd3n07c
                           07c
                                >
                                      REG
                                            29
                                                 0
                                                    0.000
                                                           58
                                                                 0
                                                                    0.000
1
    cl_nor2n06c
                           06c
                                >
                                     REG
                                            26
                                                 0
                                                    0.000
                                                           26
                                                                 0
                                                                    0.000
1
    cl_ao21n07c
                           07c
                                            30
                                      REG
                                                 0
                                                    0.000
                                                            30
                                                                 0
                                                                    0.000
1
    cl_oa21n07c
                           07c
                                      REG
                                            30
                                                 0
                                                    0.000
                                                            30
                                                                 0
                                                                    0.000
1
    cb_mode_block
                             Α
                                 > SEQUENTIAL
                                                 70
                                                      0.000
                                                                      0.000
                                                                 70
6
    cb_clk_32 1
                               > SEQUENTIAL
                                              80
                                                    0 0.000 480
                                                                    0.000
1
    cs xbn2n01b
                           01b
                                      XNOR
                                              8
                                                  0.000
                                                             8
                                                                 0.000
1
    cs xbo2n01d
                           01d
                                      XOR
                                             8
                                                 0
                                                    0.000
                                                            8
                                                                0.000
```

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

```
# of
Levels Output
 0
        1
 1
       55
             50* plus *****
 2
        1
 3
        8
 4
        1
 10
        3
 11
        1
 12
        1
 14
        2
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 2
       20
 3
        1
 4
        5
        2
 5
 6
        6
 7
        4
 8
        4
 9
        1
 10
        6
 12
         1
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
              950* plus **********
 1
       964
              100* plus **
 2
       102
 3
       39
 4
        17
 5
        8
 6
        11
 7
        2
 8
        4
         3
 13
 14
        16
 15
         1
```

#### [End of measure]

[measure]: Execution time was 0.6 seconds.

- > tc\_parm SLEW\_LIM(100)
- > tc\_parm CAP\_LIM(100)

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/techredund.tcl

- > str\_parm tgfs\_effort
- > is\_parm no\_tech\_redund
- > is\_parm remove\_redundant\_regs
- > make\_constants\_in nonreg\_only
- > ignore\_trivial\_expansions EQNVIEW
- > expansions\_from\_tib EQNVIEW
- > expansions\_from\_eqn EQNVIEW
- > copy\_def\_to\_proto EQNVIEW
- > apply decide\_boolean(EQNVIEW)

generated 1 paths in 70 milliseconds

> apply Hstructure(EQNVIEW)

generated 1 paths in 30 milliseconds

- > gen\_nonreg\_tib\_expns TIB\_EXPANSIONS
- > apply Hunstructure()
- > expandable\_name

```
> set_nochange
               > constmod
               > is_parm keep_bad_pgroups
                > bad_pgroups_expandable
               > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(EQNVIEW)));
[BD-350000]: [test_key]: CMVC version 1.9 compiled on Apr 8 1999 at 05:15:23.
[simple_expand]: Compiled on Mar 10 1999 at 05:19:51.
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 946 objects as matching keyword criteria.
>>]: nextbox( SASname(PROTECT) ):
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: Compiled on Mar 10 1999 at 05:08:18.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1169 signals, 946 usage boxes and 1783 connections.
[simple_expand]: Modfied 0 gates.
               > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(TIB_EXPANSIONS)));
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 946 objects as matching keyword criteria.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1169 signals, 946 usage boxes and 1783 connections.
[simple_expand]: Modfied 0 gates.
                                        ....
               > headless
[headless]: Compiled on Mar 10 1999 at 05:13:38.
[headless]: Removed 0 boxes
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1169 signals, 946 usage boxes and 1783 connections.
               > cleanse1
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1169 signals, 946 usage boxes and 1783 connections.
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40000]: invrem CMVC version 1.11 compiled on Apr 8 1999 at 05:03:32
[BD-40000]: onein CMVC version 1.12 compiled on Apr 8 1999 at 05:03:55
```

```
[BD-40000]: twoin CMVC version 1.6 compiled on Apr 8 1999 at 05:04:02
 [BD-40600]: Removed 0 double inverters.
 [invrem]: Execution time was 0.0 seconds.
 [BD-40500]: Removed 0 noninverting buffers.
 [BD-40501]: Changed 0 gates to inverters.
 [onein]: Execution time was 0.0 seconds.
 [BD-40550]: Removed 0 redundant pins.
 [twoin]: Execution time was 0.0 seconds.
 [cleanup]: Compiled on Apr 13 1999 at 18:01:26.
 [cleanup]: 0 boxes disconnected
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 1169 signals, 946 usage boxes and 1783 connections.
 >>1: nextbox( twoin() );
 [BD-40550]: Removed 0 redundant pins.
 [twoin]: Execution time was 0.0 seconds.
               > nochange
           > set_nochange
            > apply {Hstructure( EQNVIEW TIB_EXPANSIONS)}
 generated 1 paths in 60 milliseconds
           > rtolbox {Htgfsredund( 100 )}
 >>1: rtolbox( Htgfsredund( 100 ) );
 [BD-330000]: Htgfsredund CMVC version 1.15 compiled on Apr 8 1999 at 05:29:58.
 [BD-330500]: Out of 2898 faults found 0 redundancies, eliminated 0, could not decide 0 in 2 seconds.
            > apply Hunstructure()
           > nochange
           > DeleteAllProtosUnderView TIB_EXPANSIONS
[SRULE-17175]: Deleted 5 Proto Boxes
          > randsim q
 >>1: randsim( q );
 Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/simple_map.tcl
           > randsim q
 >>]: randsim( q );
           > is_parm keep_bad_pgroups
            > copyinfo
            > fix_bad_pgroups
 [BD-80000]: fix_bad_pgroups CMVC version 1.3 compiled on Apr 8 1999 at 05:22:04
 [BD-82400]: Added 0 terminators, deleted 0 pins and tied 0 pins.
           > basetype
 >>]: nextbox_with_test( test_syn_hide(!HIDE_MAP),genmark );
 Itest syn hide]: Number of objects selected was 946 of 946 checked.
 >>]: nextnet( geninv );
           > copyinfo
           > nextbox {mapprim, mapterm}
 >>]: nextbox( mapprim, mapterm );
 [BD-80000]: mapprim CMVC version 1.14 compiled on Apr 13 1999 at 18:10:28
 [BD-80000]: mapterm CMVC version 1.8 compiled on Apr 8 1999 at 05:24:14
 [mapprim]: Execution time was 0.0 seconds.
 [BD-83600]: 0 terminators processed 0 dummy nets removed.
```

```
> cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1169 signals, 946 usage boxes and 1783 connections.
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: CMVC version 1.12 compiled on Apr 13 1999 at 18:01:28.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1169 signals, 946 usage boxes and 1783 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1169 signals, 946 usage boxes and 1783 connections.
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
         > nextbox tchname(NOERR)
>>]: nextbox( tchname(NOERR) );
[BD-80000]: tchname CMVC version 1.13 compiled on Apr 8 1999 at 05:28:02
NOERR option set
[BD-85300]: Looked at 946 gates, bound 0, 0 had hints.
[tchname]: Execution time was 0.0 seconds.
          > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1169 signals, 946 usage boxes and 1783 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1169 signals, 946 usage boxes and 1783 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1169 signals, 946 usage boxes and 1783 connections.
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
         > copyinfo
```

```
> has_children CONSTANT
          > tiegen FOLIM(8)
[BD-80000]: tiegen CMVC version 1.11 compiled on Apr 8 1999 at 05:28:21
        > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
ftc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: ========
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > compare key_slack_limit TIME_REDUND
-2329.30 Avg: -296.08
comparing keyed new slack -2329.3015 to keyed saved slack
> reset_key_slack_limit TIME_REDUND
-2329.30 Avg: -296.08
resetting keyed current slack to -2329.3015
         > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL), ACTUAL, TWO_LEVEL, NO_VIOLATIONS) );
[BD-500000]: critical CMVC version 1.22 compiled on Apr 13 1999 at 18:21:44
-2329.30 Avg: -296.08
maximum area for proto box IDCDSUC is 4487
[BD-500000]: tswap CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-2329.30 Avg: -296.08
ArrayNum: 15 ArrayMax: 946
-2314.78 Avg: -294.64
ArrayNum: 15 ArrayMax: 946
-2306.24 Avg: -294.08
ArrayNum: 15 ArrayMax: 946
-2299.91 Avg: -293.12
ArrayNum: 15 ArrayMax: 946
-2294.80 Avg: -293.12
ArrayNum: 15 ArrayMax: 946
-2294.50 Avg: -293.42
ArrayNum: 15 ArrayMax: 946
[BD-500304]: 12 pins swapped on 5 gates and 0 gates cloned.
[tswap]: Execution time was 0.5 seconds.
[BD-502000]: Called transforms 30 times and applied 5 of them.
          > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}
-2294.50 Avg: -293.42
maximum area for proto box IDCDSUC is 4487
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-2294.50 Avg: -293.42
ArrayNum: 15 ArrayMax: 946
-2273.00 Avg: -289.24
ArrayNum: 13 ArrayMax: 946
-2252.61 Avg: -287.39
```

ArrayNum: 11 ArrayMax: 946

```
-2252.05 Avg: -287.35
ArrayNum: 11 ArrayMax: 946
-2250.42 Avg: -287.20
ArrayNum: 11 ArrayMax: 946
[BD-500026]: repower was applied 4 times.
[repower]: Execution time was 0.8 seconds.
[BD-502000]: Called transforms 27 times and applied 4 of them.
          > compare_key_slack_limit TIME_REDUND
-2250.42 Avg: -287.20
comparing keyed new slack -2250.4236 to keyed saved slack -2306.0085
          > reset_key_slack_limit TIME_REDUND
-2250.42 Avg: -287.20
resetting keyed current slack to -2250.4236
          > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
-2250.42 Avg: -287.20
maximum area for proto box IDCDSUC is 4497
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-2250.42 Avg: -287.20
ArrayNum: 11 ArrayMax: 946
-2249.91 Avg: -287.22
ArrayNum: 11 ArrayMax: 946
-2248.67 Avg: -287.28
ArrayNum: 11 ArrayMax: 946
[BD-500304]: 4 pins swapped on 2 gates and 0 gates cloned.
[tswap]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 15 times and applied 2 of them.
          > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}
critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS) );
-2248.67 Avg: -287.28
maximum area for proto box IDCDSUC is 4497
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-2248.67 Avg: -287.28
ArrayNum: 11 ArrayMax: 946
-2242.84 Avg: -286.73
ArrayNum: 11 ArrayMax: 946
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 0.2 seconds....
[BD-502000]: Called transforms 14 times and applied 1 of them.
         > compare_key_slack_limit TIME_REDUND
-2242.84 Avg: -286.73
comparing keyed new slack -2242.8408 to keyed saved slack -2227.9194
         > delete_key_slack_limit TIME_REDUND
         > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
>>]: [quick]:( onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
[quick]: CMVC version 1.31 compiled on Apr 1 1999 at 05:18:11.
-2242.84 Avg: -286.73
[onebuff]: Compiled on Mar 31 1999 at 11:33:14.
[onebuff]: setting SCORE option to ALL.
```

```
[onebuff]: setting RE_POWER option.
[onebuff]: setting INC mode.
[onebuff]: setting NO_VIOLATIONS option.
-2242.84 Avg: -286.73
maximum area for proto box IDCDSUC is 4503
[quick]: Number of boxes to process is 946.
[quick]: Number of boxes processed is 0.
-2242.84 Avg: -286.73
[onebuff]: was applied 0 times
         > quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
[
>>]: [quick]:( dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-2242.84 Avg: -286.73
[BD-500000]: dinv CMVC version 1.13 compiled on Apr 13 1999 at 18:30:14
setting SCORE option to ALL.
setting RE_POWER option.
setting INC mode.
setting NO VIOLATIONS option.
-2242.84 Avg: -286.73
maximum area for proto box IDCDSUC is 4503
[quick]: Number of boxes to process is 946.
[quick]: Number of boxes processed is 0.
-2227.45 Avg: -238.89
[BD-500500]: Moved 12 sinks and removed 19 inverters.
      > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS), repowe...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-2227.45 Avg: -238.89
maximum area for proto box IDCDSUC is 4460
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-2227.45 Avg: -238.89
ArrayNum: 6 ArrayMax: 927
-2189.99 Avg: -233.31
ArrayNum: 6 ArrayMax: 927
-2168.35 Avg: -233.23
ArrayNum: 6 ArrayMax: 927
-2160.94 Avg: -233.27
ArrayNum: 6 ArrayMax: 927
[BD-500026]: repower was applied 3 times.
[repower]: Execution time was 0.3 seconds.
[BD-500026]: repower was applied 3 times.
[repower]: Execution time was 0.3 seconds.
[BD-502000]: Called transforms 24 times and applied 3 of them.
       > write end point report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
```

Sun Apr 18 21:58:43 1999

Part: IDCDSUC

Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3 Cause of Slack Abbreviation Comparison/Description Slack Continuation SlkCont Slack due to a point downstream on path Required Arrival Time RAT ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating Hold ClkGHld ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width CIKTPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) Setup Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST) CIKPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK ClockPulseWidth TRAILING EDGE ) ClkSep ClockSeparation (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ARRIVAL TIME + ADJUST ) Loop ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM CLOCK + ADJUST ) Arrival Time Limiting Slack discontinuity due to failed test **ATLimit** LimitedAT/ Delay/ Failed Test/ Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adi NetName 1 dcd succ last t1 R C3+R 3160 -2161 3847 1011 1 PO dcd\_succ\_last\_t1 RAT 999 ----> BOX714/OUT R C3+R 3160 -2161 3847 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1 ----> BOX714/IN R C3+R 3160 -2161 3847 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1&0 ----> C167/y R C3+R 3160 -2161 3847 1011 1 cs\_invvn 01c NOT 0 dcd\_succ\_last\_t1&0 ----> C167/a FC3+R 1202 -2161 76 302 4 cs\_invvn 01c NOT 1958 N675 ---->{a} C2738/y FC3+R 1202 -2161 76 302 4 cs nnd2n 14b NAND 0 N675 ----> C2738/a R C3+R 1148 -2161 183 108 1 cs\_nnd2n 14b NAND 54 last\_cycle ---->{b} C2487/y R C3+R 1148 -2161 183 108 1 cs nnd2n 05e NAND 0 last cycle ----> C2487/b FC3+R 1058 -2161 60 42 2 cs\_nnd2n 05e NAND 90 N1587 ----> C1952/v FC3+R 1058 -2161 60 42 2 cs\_invvn 05b NOT

N1587 > C1952/a	R C3+R 1024 -2161 80 53 2 cs_invvn 05b NOT
34 num_dcd_cyl&0(1)	
> BOX679/OUT	R C3+R 1024 -2161 80 53 2 IOPAD IOPAD
0 num_dcd_cyl&0(1) > BOX679/IN	R C3+R 1024 -2161 80 53 2 IOPAD IOPAD 0
num_dcd_cyl(1)	
> num_dcd_cyl(1)	R C3+R 1024 -2161 80 53 2 Pl 0
num_dcd_cyl(1)	
2-dcd_succ_last_t1	F C3+R 2880 -1881 2362 1011 1 PO 0
dcd_succ_last_t1	999 0
RAT > BOX714/OUT	999 0 F C3+R 2880 -1881 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1	1 00+11 2000 1001 2002 1011 1101715 101715
> BOX714/IN	F C3+R 2880 -1881 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&0	
> C167/y	F C3+R 2880 -1881 2362 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0> C167/a	R C3+R 1284 -1881 130 302 4 cs_invvn 01c NOT
1596 N675	17 OOTH 1204 1001 100 002 100_HVVII 0101101
>{a} C2738/y	R C3+R 1284 -1881 130 302 4 cs_nnd2n 14b NAND
0 N675	The state of the s
> C2738/a	F C3+R 1192 -1881 195 108 1 cs_nnd2n 14b NAND
93 last_cycle >{b} C2487/y	F C3+R 1192 -1881 195 108 1 cs_nnd2n 05e NAND
0 last_cycle	
> C248//D	R C3+R 1077 -1881 110 42 2 cs_nnd2n 05e NAND
115 N1587	R C3+R 1077 -1881 110 42 2 cs_invvn 05b NOT
> C1952/y 0 N1587	R C3+R 1077 -1881 110 42 2 cs_invvn 05b NOT
> C1952/a	F C3+R 1016 -1881 80 53 2 cs_invvn 05b NOT 61
num_dcd_cyl&0(1)	
> BOX679/OUT	F C3+R 1016 -1881 80 53 2 IOPAD IOPAD
0 num_dcd_cyi&0(1) > BOX679/IN	F C3+R 1016 -1881 80 53 2 IOPAD IOPAD 0
num_dcd_cyl(1)	1 00+11 1010 1001 00 00 2101715 101715 0
> num_dcd_cyl(1)	F C3+R 1016 -1881 80 53 2 Pl 0
num_dcd_cyl(1)	
3 local_milli_t2.reg_n.lat_0/a	F C3+R 2825 -1505 48 31 1 cl_invvn 07c SRL
41 N2054	
Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4 > C3011/y	F C3+R 2825 -1505 48 31 1 cs_invvn 07c NOT 0
N2054	1 COTIL 2023 -1003 40 01: 1 03_IIIVIII 0701101 0
> C3011/a	R C3+R 2788 -1505 466 92 3 cs_invvn 07c NOT
37 N73	DOO D 0700 4505 400 00 00 400 400 400 400
>{a} C2794/y	R C3+R 2788 -1505 466 92 3 cs_ao12n 03c AOI
0 N73 > C2794/a2	F C3+R 2547 -1505 115 18 1 cs_ao12n 03c AOI
241 N1866	. 55 2511 1000 10 100_501.2 0007101
>{b} C2555/y	F C3+R 2547 -1505 115 18 1 cs_ao12n 03c AOI

0 N1866					
> C2555/b	R C3+R	2438 -1505	3912 1044	3 cs_ao12n	03c AOI
109 iu_reset_op_c_t1&0					
>{c} C2393/y	R C3+R	2438 -1505	3912 1044	3 cs_nnd2n	02c NAND
0 iu_reset_op_c_t1&0		•			
> C2393/a	F C3+R	480 -1505	78 137 3 c	s_nnd2n 02	c NAND
1958 gbfonet_6					
> gbfocell_6/y	F C3+R	480 -1505	78 137 3 6	cs_invvn 09	NOT 0
gbfonet_6					
> gbfocell_6/a	R C3+R	417 -1505	217 43 1	cs_invvn 09	c NOT
64 N2031					
>{d} C2162/y	R C3+R	417 -1505	217 43 1	cs_nnd3n 0	2c NAND
0 N2031					
> C2162/c	F C3+R	303 -1505	57 49 3 cs	s_nnd3n 02d	NAND
113 exc_cond_q	_	_			
> exc_cond.reg_n.lat_0/l2_out_	n F	C3+R 303	-1505 57	49 3 cl_invv	n 07d SRL
0 exc_cond_q					
> exc_cond.reg_n.lat_0/c2	RC	3+ 160 N	I/C 60 239	9 14 cl_invvn	07d SRL
143 slow_mode.c2_4					
> slow_mode.clockblock_3/c2	R	C3+ 160	N/C 60 2	239 14 cb_clk_	_32_1 LCB
0 slow_mode.c2_4					

#### > measure

The model <IDCDSUC> has: Primary Inputs **Primary Outputs** · 73 **Primary BIDIs** 477 117 0 Signals 1148 Gate Count 927 Connections -1764 Master REG Bits 83 Slave REG Bits 83 Internal Area 4461 External Area 0 Gates/Connects 0.525510 **Fanout Count** 1764. Average Fanout 1.536585 Avg Tech Box Size = 4.812298 Tech Box Size Stddev = 0.010650 Power 0.000000

# \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\* Real signals = 773 Real boxes = 552

 Real connections
 =
 1389

 Real LSTs
 =
 2162

 Real ICells/box
 =
 8.081522

 Real LSTs/box
 =
 3.916667

 Real nets/box
 =
 1.400362

Cell Total Each Cell

Type Cnt Boxname Power Level Function Int Ext Power Int Ext Power

```
AOI
                                                        0
                                                           0.000
                                                                   42
                                                                         0
                                                                            0.000
                                03c
                                                   6
7
     cs_ao22n03c
                                      >
                                                   4
                                                                   20
                                                                         0
                                                                            0.000
                                                        0
                                                           0.000
     cs_ao12n03c
                                03c
                                            aoi
5
                                                            0.000
     cs_ao22n10c
                                10c
                                            AOI
                                                  18
                                                        0
                                                                    18
                                                                          0
                                                                             0.000
 1
                                        BRKPT
                                                   0
                                                           0.000
                                                                    0
                                                                        0
                                                                           0.000
                                                       0
      BRKPT
                                   >
180
                                                          0.000
                                                                   0
                                                                       0
                                                                           0.000
      IOPAD
                                   >
                                        IOPAD
                                                  0
                                                      0
195
                                                                     492
                                                      3
                                                              0.000
                                                                             0
                                                                               0.000
                                 02c
                                       >
                                            NAND
                                                          0
      cs nnd2n02c
164
                                                                              0.000
                                           NAND
                                                     8
                                                         0
                                                             0.000
                                                                      8
                                                                          0
                                10c
     cs nnd2n10c
                                      >
1
                                            NAND
                                                     4
                                                          0
                                                             0.000
                                                                      96
                                                                           0
                                                                              0.000
                                02c
                                      >
24
      cs_nnd3n02c
                                           NAND
                                                     4
                                                         0
                                                             0.000
                                                                      8
                                                                          0
                                                                              0.000
                                05c
2
     cs nnd2n05c
                                      >
                                                                     30
                                                                           0
                                                                              0.000
                                                     5
                                                         0
                                                             0.000
     cs nnd4n03c
                                03c
                                           NAND
6
                                      >
                                                          0
                                                             0.000
                                                                      30
                                                                           0
                                                                              0.000
 2
                                13c
                                           NAND
                                                    15
     cs_nnd2n13c
                                      >
                                                                      9
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                                                                              0.000
                                04c
                                           NAND
                                                     3
                                                         0
                                                             0.000
 3
     cs nnd2n04c
                                      >
                                                                           0
                                                                              0.000
                                07c
                                           NAND
                                                     6
                                                         0
                                                             0.000
                                                                     12
 2
                                      >
     cs_nnd3n07c
                                                         0
                                                             0.000
                                                                           0
                                                                              0.000
                                05e
                                           NAND
                                                     4
                                                                      4
 1
     cs_nnd2n05e
                                      >
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                                                                              0.000
                                                             0.000
                                                                      9
                                           NAND
                                                     3
                                                         0
 3
     cs_nnd2n03c
                                03c
                                      >
                                                                     20
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                                                                              0.000
                                           NAND
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 5
     cs nnd2n07c
                                07c
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                                           NAND
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 2
                                12c
     cs nnd2n12c
                                      >
                                                                               0.000
                                                              0.000
                                                                      20
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                                14b
                                           NAND
                                                    20
                                                          0
 1
     cs_nnd2n14b
                                      >
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                                                                               0.000
                                12c
                                           NAND
                                                    22
                                                          0
                                                              0.000
                                                                      22
                                      >
 1
     cs_nnd3n12c
                                                                            0
                                                                               0.000
                                           NAND
                                                    19
                                                          0
                                                              0.000
                                                                      38
 2
                                14c
      cs nnd2n14c
                                      >
                                                                               0.000
                                                          0
                                                              0.000
                                                                      16
                                                                            0
 1
     cs_nnd4n09c
                                09c
                                      >
                                           NAND
                                                    16
                                                          0
                                                              0.000
                                                                      11
                                                                            0
                                                                               0.000
                                11c
                                      >
                                           NAND
                                                    11
 1
      cs_nnd2n11c
                                                     4
                                                         0
                                                             0.000
                                                                      4
                                                                           0
                                                                              0.000
                                06c
                                           NAND
      cs nnd2n06c
                                      >
 1
                                                    12
                                                          0
                                                              0.000
                                                                      12
                                                                            0
                                                                              0.000
                                09c
                                           NAND
      cs_nnd3n09c
                                      >
 1
                                            NOR
                                                         0
                                                            0.000
                                                                     30
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                                                                              0.000
                                02c
                                                    3
                                      >
10
      cs_nor2n02c
                                            NOR
                                                            0.000
                                                                     4
                                                                         0
                                                                             0.000
                                03c
                                                    4
                                                        0
 1
      cs_nor3n03c
                                      >
                                                   12
                                                                     12
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                                                         0
                                                            0.000
                                12c
                                            NOR
 1
      cs nor2n12c
                                      >
                                                                         0 -
                                                                             0.000
                                           NOR
                                                   3
                                                        0
                                                            0.000
                                                                     3
                                04c
                                      >
 1
      cs nor2n04c
                                                   12
                                                                     12
                                                                              0.000
                                                         0
                                                            0.000
                                                                          0
                                            NOR
                                10c
 1
      cs nor3n10c
                                      >
                                                        0
                                                                     7
                                                                         0
                                                                             0.000
                                                    7
                                                            0.000
                                08c
                                      >
                                            NOR
 1
      cs_nor2n08c
                                                                    180
                                                                              0.000
                                            NOT
                                                    2
                                                        0
                                                            0.000
                                                                          0
                                01c
                                      >
90
      cs invvn01c
                                                                         0
                                                                             0.000
                                           NOT
                                                   6
                                                        0
                                                           0.000
                                                                    24
 4
      cs invvn11c
                               11c
                                     >
                                                                             0.000
                                                                    20
                                                                         0
                                                   4
                                                        0
                                                           0.000
 5
      cs_invvn10c
                               10c
                                     >
                                           NOT
                                                    6
                                                        0
                                                            0.000
                                                                    126
                                                                          0
                                                                              0.000
21
      cs_invvn12c
                                12c
                                      >
                                            NOT
                                                                             0.000
                                                   4
                                                        0
                                                           0.000
                                                                    28
                                                                         0
 7
      cs_invvn09c
                               09c
                                     >
                                           NOT
                                                    2
                                                                          0
                                                                             0.000
29
      cs invvn07c
                                07c
                                      >
                                            NOT
                                                        0
                                                            0.000
                                                                    58
                                                   10
                                                        0
                                                            0.000
                                                                    40
                                                                          0
                                                                             0.000
 4
                               15c
                                     >
                                           NOT
      cs_invvn15c
                                           NOT
                                                   2
                                                        0
                                                           0.000
                                                                    18
                                                                         0
                                                                             0.000
                               06c
                                     >
 9
      cs_invvn06c
                                                    2
                                                            0.000
                                                                          0
                                                                             0.000
                                05c
                                      >
                                            NOT
                                                        0
                                                                    24
12
      cs_invvn05c
                               13c
                                           NOT
                                                   8
                                                        0
                                                           0.000
                                                                    32
                                                                         0
                                                                             0.000
                                     >
 4
      cs invvn13c
                                           NOT
                                                   2
                                                        0
                                                           0.000
                                                                    2
                                                                         0
                                                                            0.000
                               05b
 1
      cs invvn05b
                                     >
                                                   4
                                                        0
                                                           0.000
                                                                    12
                                                                         0
                                                                             0.000
                               08c
                                     >
                                           NOT
 3
      cs invvn08c
                                           NOT
                                                   2
                                                        0
                                                           0.000
                                                                    12
                                                                         0
                                                                             0.000
                               02c
                                     >
 6
      cs invvn02c
                                                        0
                                                           0.000
                                                                    8
                                                                         0 1
                                                                            0:000
                                           NOT
                                                   8
                               14c
                                     >
 1
      cs invvn14c
                                                   2
                                                                             0.000
                                                           0.000
                                                                    10
                                                                         0
                               04c
                                     >
                                           NOT
                                                        0
 5
      cs_invvn04c
                                                   20
                                                        0
                                                            0.000
                                                                    20
                                                                          0
                                                                             0.000
                               18c
                                           NOT
      cs invvn18c
                                     >
 1
                                                                    42
                                                                             0.000
                               16c
                                           NOT
                                                   14
                                                        0
                                                            0.000
                                                                          0
 3
      cs invvn16c
                                     >
                               19c
                                           NOT
                                                   25
                                                        0
                                                            0.000
                                                                    25
                                                                          0
                                                                             0.000
                                     >
 1
      cs_invvn19c
                                            OAI
                                                   5
                                                        0
                                                            0.000
                                                                    5
                                                                         0
                                                                            0.000
                                04c
                                      >
 1
      cs_oa21n04c
                                                                    6
                                                                            0.000
                                                            0.000
                                                                         0
                                03c
                                            OAI
                                                   6
                                                        0
 1
      cs_oa22n03c
                                      >
                                                                             0.000
                                                         0
                                                            0.000
                                                                    14
                                                                          0
 1
      cs_oa21n10c
                                10c
                                      >
                                            OAL
                                                   14
                                                                              0.000
                                                   25
                                                         0
                                                            0.000
                                                                    550
                                                                           0
                               07c
                                           REG
22
      cl invvn07c
                                     >
                                                                    750
                                                                           0
                                                                              0.000
                               07d
                                      >
                                            REG
                                                   25
                                                         0
                                                            0.000
 30
      cl invvn07d
                                07c
                                            REG
                                                   26
                                                         0
                                                             0.000
                                                                     468
                                                                            0
                                                                               0.000
 18
      cl nnd2n07c
                                      >
                                                            0.000
                                                                    264
                                                                           0
                                                                              0.000
                                            REG
                                                   33
                                                         0
 8
      cl_ao22n07c
                                07c
```

```
2
   cl_nnd3n07c
                         07c
                                   REG
                                        29
                                              0.000
                                                       58
                                                            0.000
   cl_nor2n06c
1
                        06c
                                  REG
                                                0.000
                             >
                                        26
                                             0
                                                       26
                                                            0
                                                              0.000
   cl_ao21n07c
1
                         07c
                                   REG
                                         30
                                              0
                                                0.000
                                                       30
                                                            0
                                                               0.000
1
   cl_oa21n07c
                         07c
                                   REG
                                         30
                                              0
                                                 0.000
                                                       30
                                                            0
                                                               0.000
1
   cb_mode_block
                             > SEQUENTIAL
                                             70
                                                  0.000
                                                            70
                                                                 0.000
6
   cb_clk_32_1
                            > SEQUENTIAL 80
                                                0 0.000 480
                                                               0.000
1
   cs_xbn2n01b
                         01b
                                   XNOR
                                           8
                                               0.000
                                                         8
                              >
                                                            0.000
   cs_xbo2n01d
1
                         01d
                                   XOR
                                              0.000
                                                        8
                                                            0
                                                              0.000
```

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# O	Ī	
Levels	Outp	out
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

# of

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
Levels Register
 0
 2
       20
 3
        1
        5
 4
 5
        3.
 6
       10
 7
        3
 9
        1
 10
        6
 12
        1
        2
13
        4
14
15
        10
16
        3
17
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
      945
             900* plus *
 1
             100* plus *
 2
      101
 3
       41
 4
       16
 5
       8
 6
       11
 7
       2
 8
        4
        3
 13
 14
        16
 15
        1
[End of measure]
[measure]: Execution time was 0.7 seconds.
      > traceset {repower_paths HOWMANY}
[traceset]: trace string = repower_paths HOWMANY
[tracing]: set trace variable repower_paths to 20
      > tc_parm MARGIN(10000000)
      > repower_paths FUZZY(0.02)
initial slack is -2161
after repower paths slack is -1993
      > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 21:59:01 1999
Part: IDCDSUC
                                      EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                   Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
Sort Field: Slack
                                Max. Endpoints: 3
                        Abbreviation Comparison/Description
 Cause of Slack
                         SlkCont
                                    Slack due to a point downstream on path
 Slack Continuation
                          RAT
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
 Asserted Required Arrival Time AssrtRAT
                                         ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 Clock Gating Setup
                          ClkGSet
ARRIVAL TIME + ADJUST )
                                    ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                         CIKGHId
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                           CIKTPW
                                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 Clock Tree Pulse Width
TRAILING EDGE)
                               ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 Setup
                     Setup
ADJUST)
                              ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 Hold
                    Hold
ADJUST )
                                   ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                        EndOfC
 EndOfCycle
ADJUST)
                                     ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                         CIkPW
 ClockPulseWidth
```

Arrival Time Limiting ATLimit Slack discontinuity due to failed test    Num/		!		RRIVAL TIME + CLOCK SEPARATI	ST)	TRAILING EDGE ) ClockSeparation ARRIVAL TIME + ADJUS Loop AL CLOCK + ADJUST )	,
Test PinName				tinuity due to failed test	ATLimit Slack dis		
dcd_succ_last_t1       999       0         RAT       999       0        > BOX714/OUT       R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD         0 dcd_succ_last_t1       R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD         0 dcd_succ_last_t1&0       O dcd_succ_last_t1&0						Test PinName	1
dcd_succ_last_t1       999       0         RAT       999       0        > BOX714/OUT       R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD         0 dcd_succ_last_t1       R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD         0 dcd_succ_last_t1&0       R C3+R 2992 -1993 3847 1011 1 IOPAD		- ,		the contract of the contract of	.,		_
> BOX714/OUT R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD 0 dcd_succ_last_t1> BOX714/IN R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD 0 dcd_succ_last_t1&0			0	2992 -1993 3847 1011 1 PO	R C3+R		(
> BOX714/IN R C3+R 2992 -1993 3847 1011 1 IOPAD IOPAD 0 dcd_succ_last_t1&0			D IOPAD	_		> BOX714/OUT	-
			IOPAD	992 -1993 3847 1011 1 IOPAD	R C3+R	> BOX714/IN	-
0 dcd_succ_last_t1&0			01c NOT	2 -1993 3847 1011 1 cs_invvn	R C3+R	> C167/y	-
> C167/a F C3+R 1130 -1993 55 139 4 cs_invvn 01c NOT			)1c NOT	0 -1993 55 139 4 cs_invvn (	F C3+R	> C167/a	-
1862 N675 >{a} C2738/y F C3+R 1130 -1993 55 139 4 cs_nnd2n 14b NAND			14b NAND	30 -1993 55 139 4 cs_nnd2n	F C3+R	>{a} C2738/y	· · -
0 N675 > C2738/b R C3+R 1099 -1993 90 159 3 cs_nnd2n 14b NAND			14b NAND	99 -1993 90 159 3 cs_nnd2n	R C3+R	> C2738/b	-
31 N1692 >{b} C2725rwr/y R C3+R 1099 -1993 90 159 3 cs_nnd2n 14c NAND	1.57% 1.57%	•	14c NAND	099 -1993 90 159 3 cs_nnd2i	R C3+R	>{b} C2725rwr/y	-
0 N1692 > C2725rwr/a F C3+R 1050 -1993 93 168 2 cs_nnd2n 14c NAND 49 N1479			14c NAND	50 -1993 93 168 2 cs_nnd2n	F C3+R	> C2725rwr/a	-
>{c} C2721rwr/y F C3+R 1050 -1993 93 168 2 cs_nnd3n 12c NAND 0 N1479			12c NAND	050 -1993 93 168 2 cs_nnd3r	FC3+R	>{c} C2721rwr/y	. · · · · · · · · · · · · · · · · · · ·
> C2721rwr/c R C3+R 990 -1993 179 95 2 cs_nnd3n 12c NAND 59 N1497			12c NAND	90 -1993 179 95 2 cs_nnd3n	R C3+R	> C2721rwr/c	-
>{d} C2709rwr/y R C3+R 990 -1993 179 95 2 cs_nor3n 10c NOR 0 N1497		* * *	10c NOR	990 -1993 179 95 2 cs_nor3n	R C3+R	>{d} C2709rwr/y	<del>-</del>
> C2709rwr/b F C3+R 899 -1993 49 52 1 cs_nor3n 10c NOR 92 N1986			10c NOR	99 -1993 49 52 1 cs_nor3n	FC3+R	> C2709rwr/b	· -
>{e} C2677rwr_0/y F C3+R 899 -1993 49 52 1 cs_nnd2n 12c NAND 0 N1986	•		12c NAND	899 -1993 49 52 1 cs_nnd2r	F C3+R	>{e} C2677rwr_0/y	
> C2677rwr_0/b R C3+R 872 -1993 74 88 2 cs_nnd2n 12c NAND 27 N1094			12c NAND	872 -1993 74 88 2 cs_nnd2n	R C3+R	> C2677rwr_0/b	
>{f} C2909/y R C3+R 872 -1993 74 88 2 cs_nnd2n 14c NAND 0 N1094			14c NAND	2 -1993 74 88 2 cs_nnd2n	R C3+R	>{f} C2909/y	-
> C2909/a F C3+R 835 -1993 80 108 1 cs_nnd2n 14c NAND 37 dcd_mcr41_blk&0			14c NAND	5 -1993 80 108 1 cs_nnd2n	F C3+R	> C2909/a	
> BOX615/OUT F C3+R 835 -1993 80 108 1 IOPAD IOPAD 0 dcd_mcr41_blk&0			IOPAD	835 -1993 80 108 1 IOPAD	F C3+R	> BOX615/OUT	
> BOX615/IN F C3+R 835 -1993 80 108 1 IOPAD IOPAD 0 dcd_mcr41_blk			IOPAD 0	35 -1993 80 108 1 IOPAD	F C3+R	> BOX615/IN	
dcd_mcr41_blk F C3+R 835 -1993 80 108 1 PI 0 dcd_mcr41_blk			0	835 -1993 80 108 1 PI	F C3+R	> dcd_mcr41_blk	

F C3+R 2575 -1576 2362 1011 1 PO	0
999 0	
F C3+R 2575 -1576 2362 1011 1 IOPAD I	OPAD
F C3+R 2575 -1576 2362 1011 1 IOPAD IOI	PAD
F C3+R 2575 -1576 2362 1011 1 cs_invvn 01c NC	TC
R C3+R 1139 -1576 93 139 4 cs_invvn 01c NO	Т
R C3+R 1139 -1576 93 139 4 cs_nnd2n 14b N	IAND
F C3+R 1087 -1576 63 159 3 cs_nnd2n 14b N/	AND
F C3+R 1087 -1576 63 159 3 cs_nnd2n 14c l	NAND
R C3+R 1045 -1576 135 168 2 cs_nnd2n 14c	NAND
R C3+R 1045 -1576 135 168 2 cs_nnd3n 12c	NAND
F C3+R 963 -1576 89 95 2 cs_nnd3n 12c NA	AND
F C3+R 963 -1576 89 95 2 cs_nor3n 10c No	OR
R C3+R 915 -1576 73 52 1 cs_nor3n 10c NC	OR .
R C3+R 915 -1576 73 52 1 cs_nnd2n 12c	NAND
F C3+R 877 -1576 50 88 2 cs_nnd2n 12c N	NAND
F C3+R 877 -1576 50 88 2 cs_nnd2n 14c NA	ND
R C3+R 850 -1576 80 108 1 cs_nnd2n 14c NA	AND
R C3+R 850 -1576 80 108 1 IOPAD IO	PAD
R C3+R 850 -1576 80 108 1 IOPAD IOPA	4D 10
R C3+R 850 -1576 80 108 1 PI	0

2825 -1505 48 31 1 cl\_invvn 07c SRL F C3+R 3 local\_milli\_t2.reg\_n.lat\_0/a 41 N2054 F C3-160 60 238 14 cl\_invvn 07c Setup local\_milli\_t2.reg\_n.lat\_0/c1 1200 slow\_mode.c1\_4 0 FC3+R 2825 -1505 48 31 1 cs\_invvn 07c NOT ----> C3011/y N2054 92 3 cs\_invvn 07c NOT 466 ----> C3011/a R C3+R 2788 -1505 37 N73 92 3 cs\_ao12n 03c AOI 2788 -1505 466 ---->{a} C2794/v RC3+R 0 N73 ----> C2794/a2 FC3+R 2547 -1505 115 18 1 cs\_ao12n 03c AOI 241 N1866

2 dcd succ\_last\_t1

dcd\_succ\_last\_t1

---> C167/y

----> C167/a 1436 N675 ---->{a} C2738/y

---> C2738/b 52 N1692

---->{b} C2725rwr/y

----> C2725rwr/a

---->{c} C2721rwr/y

---> C2721rwr/c

---->{d} C2709rwr/y

----> C2709rwr/b

---->{e} C2677rwr\_0/y

----> C2677rwr\_0/b

---> BOX615/IN dcd\_mcr41\_blk ---> dcd\_mcr41\_blk dcd\_mcr41\_blk

0 N675

0 N1692

42 N1479

0 N1479

82 N1497

0 N1497

49 N1986

0 N1986

37 N1094
---->{f} C2909/y
0 N1094
----> C2909/a
27 dcd\_mcr41\_blk&0
---> BOX615/OUT
0 dcd\_mcr41\_blk&0

---> BOX714/OUT 0 dcd\_succ\_last\_t1 ---> BOX714/IN 0 dcd\_succ\_last\_t1&0

0 dcd\_succ\_last\_t1&0

RAT

>{b} C2555/y	FC3+R	2547 -1505	115	18 1 cs_ao12n	03c AOI
0 N1866					
> C2555/b	R C3+R	2438 -1505	3912 1	044 3 cs_ao12r	n 03c AOI
109 iu_reset_op_c_t1&0					
>{c} C2393/y	R C3+R	2438 -1505	3912	1044 3 cs_nnd2	n 02c NAND
0 iu_reset_op_c_t1&0				•	
> C2393/a	F C3+R	480 -1505	78 13	7 3 cs_nnd2n	02c NAND
1958 gbfonet_6					
> gbfocell_6/y	F C3+R	480 -1505	78 13	37 3 cs_invvn (	09c NOT 0
gbfonet_6					
> gbfocell_6/a	R C3+R	417 -1505	217	43 1 cs_invvn	09c NOT
64 N2031					
>{d} C2162/y	R C3+R	417 -1505	217	43 1 cs_nnd3n	02c NAND
0 N2031					
> C2162/c	F C3+R	303 -1505	57 49	9 3 cs_nnd3n (	D2c NAND
113 exc_cond_q	_				
> exc_cond.reg_n.lat_0/l2_out_	n F	C3+R 303	-1505	57 49 3 cl_ir	nvvn 07d SRL
0 exc_cond_q	5.0		vo 00	000 44 1 1	07 1 001
> exc_cond.reg_n.lat_0/c2	HC	3+ 160 N	I/C 60	239 14 cl_invv	n 0/d SRL
143 slow_mode.c2_4		00 100	N/O	00 44 -1-	W 00 4 LOB
> slow_mode.clockblock_3/c2	н	C3+ 160	N/C	60 239 14 cb_c	CIK_32_1 LUB
0 slow_mode.c2_4		*			-

# > measure

The model <IDCDSUC> has: **Primary Inputs** 122 **Primary Outputs** 73 **Primary BIDIs** 0 Signals . 1148 Gate Count 927 Connections 1764 Master REG Bits 83 Slave REG Bits 83 Internal Area 4533 External Area 0 Gates/Connects 0.5255.10 **Fanout Count** 1764 Average Fanout 1.536585 Avg Tech Box Size = 4.889968 Tech Box Size Stddev = 0.010696 Power 0.000000

\*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\*
Real signals = 773
Real boxes = 552
Real connections = 1389
Real LSTs = 2162
Real ICells/box = 8.211957
Real LSTs/box = 3.916667
Real nets/box = 1.400362

Cell Total Each Cell

Type Cnt Boxname Power Level Function Int Ext Power Int Ext Power

```
0.000
                                            AOI
                                                   6
                                                        0
                                                           0.000
                                                                    42
                                                                         0
     cs_ao22n03c
                                03c
                                      >
7
                                                                             0.000
                                                                    16
                                                                         0
                                                   4
                                                        0
                                                           0.000
                                03c
                                      >
                                            AOI
     cs_ao12n03c
 4
                                            AOI
                                                   18
                                                        0
                                                           0.000
                                                                    18
                                                                          0
                                                                             0.000
                                10c
     cs_ao22n10c
                                      >
 1
                                                           0.000
                                                                    4
                                                                         0
                                                                            0.000
                                            AOI
                                                   4
                                                        0
     cs_ao12n04c
                                04c
 1
                                                                    0
                                                                            0.000
                                        BRKPT
                                                   0
                                                       0
                                                           0.000
                                                                        0
      BRKPT
                                    >
180
                                                                       0
                                                                           0.000
                                                       0
                                                          0.000
                                                                   0
                                        IOPAD
                                                  0
      IOPAD
195
                                   >
                                                                      492
                                                                                0.000
                                                                             0
                                 02c
                                             NAND
                                                      3
                                                           0
                                                              0.000
                                       >
      cs_nnd2n02c
164
                                                                             0.000
                                           NAND
                                                     8
                                                          0
                                                             0.000
                                                                      8
                                                                          0
                                10c
                                      >
1
     cs nnd2n10c
                                                                              0.000
                                            NAND
                                                          0
                                                             0.000
                                                                      96
                                                                            0
                                                     4
                                02c
                                       >
24
      cs_nnd3n02c
                                                                              0.000
                                                          0
                                                                      8
                                                                          0
                                           NAND
                                                     4
                                                             0.000
                                05c
                                      >
2
     cs_nnd2n05c
                                                             0.000
                                                                     25
                                                                           0
                                                                              0.000
                                           NAND
                                                     5
                                                          0
                                03c
 5
     cs nnd4n03c
                                      >
                                                                            0
                                                                              0.000
                                                          0
                                                              0.000
                                                                      15
                                13c
                                           NAND
                                                    15
     cs_nnd2n13c
                                      >
 1
                                                                              0.000
                                           NAND
                                                     3
                                                          0
                                                             0.000
                                                                      9
                                                                           0
                                04c
                                      >
 3
     cs_nnd2n04c
                                                             0.000
                                                     6
                                                          0
                                                                      6
                                                                          0
                                                                              0.000
                                           NAND
                                07c
 1
     cs nnd3n07c
                                      >
                                                              0.000
                                                                            0
                                                                               0.000
                                                          0
                                                                      19
                                            NAND
                                                     19
 1
     cs_nnd2n14e
                                14e
                                      >
                                                                              0.000
                                                          0
                                                             0.000
                                                                      6
                                                                           0
                                03c
                                            NAND
                                                     3
 2
      cs nnd2n03c
                                      >
                                                                               0.000
                                                     4
                                                          0
                                                             0.000
                                                                      12
                                                                           0
 3
     cs nnd2n07c
                                07c
                                      >
                                            NAND
                                                                               0.000
                                                                      22
                                                                            0
                                                          0
                                                              0.000
 2
                                11c
                                      >
                                            NAND
                                                    11
      cs_nnd2n11c
                                                                               0.000
                                                          0
                                                              0.000
                                                                      20
                                                                            0
                                14b
                                            NAND
                                                     20
                                      >
 1
      cs_nnd2n14b
                                                                               0.000
                                                              0.000
                                                                      22
                                                                            0
                                            NAND
                                                    22
                                                          0
      cs nnd3n12c
                                12c
                                      >
 1
                                                                              0.000
                                                                           0
                                            NAND
                                                     8
                                                          0
                                                             0.000
                                                                      8
      cs_nnd4n06c
                                06c
                                      >
 1
                                                                            0
                                            NAND
                                                    19
                                                          0
                                                              0.000
                                                                      114
                                                                                0.000
                                14c
                                      >
 6
      cs_nnd2n14c
                                                                               0.000
                                            NAND
                                                    20
                                                          0
                                                              0.000
                                                                      20
                                                                            0
                                10c
                                      >
      cs nnd4n10c
 1
                                06c
                                            NAND
                                                     4
                                                          0
                                                             0.000
                                                                      4
                                                                           0
                                                                              0.000
                                      >
      cs_nnd2n06c
 1
                                05c
                                            NAND
                                                     6
                                                          0
                                                             0.000
                                                                      6
                                                                           0
                                                                              0.000
                                      >
 1
      cs_nnd3n05c
                                            NAND
                                                     12
                                                          0
                                                              0.000
                                                                      12
                                                                            0
                                                                               0.000
                                12c
      cs nnd2n12c
                                      >
 1
                                                     12
                                                              0.000
                                                                      ·12
                                                                            O
                                                                               0.000
                                            NAND
                                                          0
      cs_nnd3n10c
                                10c
                                      >
 1
                                                     3
                                                         0
                                                             0.000
                                                                     30
                                                                           0
                                                                              0.000
                                            NOR
                                02c
 10
      cs nor2n02c
                                       >
                                                    4
                                                            0.000
                                                                     4
                                                                          0
                                                                             0.000
                                            NOR
                                                         0
      cs nor3n03c
                                03c
                                      >
 1
                                                         0
                                                                     12
                                                                           0
                                                                              0.000
                                                    12
                                                             0.000
                                            NOR
      cs_nor2n12c
                                12c
                                      >
 1
                                                                          0
                                                                             0.000
                                            NOR
                                                    3
                                                         0
                                                            0.000
                                                                     3
                                04c
 1
      cs_nor2n04c
                                      > .
                                                                     12
                                                                           0
                                                                              0.000
                                                    12
                                                         0
                                                             0.000
                                            NOR
 1
      cs_nor3n10c
                                10c
                                      >
                                                                     7
                                                                             0.000
                                                            0.000
                                                                          0
      cs_nor2n09c
                                                    7
                                                         0
                                09c
                                            NOR
 1
                                      >
                                                                    178
                                                                              0.000
                                                    2
                                                         0
                                                            0.000
                                                                           0
                                            NOT
89
      cs_invvn01c
                                01c
                                      >
                                                                             0.000
                                                        0
                                                            0.000
                                                                    24
                                                                          0
                                                    6
 4
      cs_invvn11c
                               11c
                                      >
                                           NOT
                                                                             0.000
                                                                    24
                                                                          0
                                           NOT
                                                    4
                                                        0
                                                            0.000
 6
      cs_invvn10c
                               10c
                                      >
                                                                              0.000
                                12c
                                            NOT
                                                    6
                                                         0
                                                            0.000
                                                                    132
                                                                           0
 22
                                      >
      cs_invvn12c
                                                                          0
                                                                             0.000
                                            NOT
                                                    4
                                                        0
                                                            0.000
                                                                    28
 7
      cs invvn09c
                               09c
                                      >
                                                    2
                                                            0.000
                                                                          0
                                                                              0.000
                                                         0
                                                                    56
 28
      cs_invvn07c
                                07c
                                      >
                                            NOT
                                                                              0.000
                                                   10
                                                         0
                                                            0.000
                                                                     40
                                                                          0
                                15c
                                            NOT
      cs invvn15c
 4
                                      >
                                                                              0.000
                                                    2
                                                         0
                                                            0.000
                                                                    22
                                                                          0
                                            NOT
 11
      cs invvn06c
                                06c
                                      >
                                                                              0.000
                                                    2
                                                                    24
                                                                          0
                                05c
                                            NOT
                                                         0
                                                            0.000
      cs invvn05c
                                      >
 12
                                13c
                                            NOT
                                                    8
                                                        0
                                                            0.000
                                                                    40
                                                                          0
                                                                             0.000
      cs_invvn13c
 5
                                      >
                                                                              0.000
                                            NOT
                                                   10
                                                         0
                                                            0.000
                                                                     10
                                                                           0
      cs invvn14b
                                14b
                                      >
 1
                                                        0
                                                            0.000
                                                                          0
                                                                             0.000
                               08c
                                            NOT
                                                    4
                                                                    16
                                      >
 4
      cs_invvn08c
                                                    2
                                                        0
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
                                            NOT
                               02c
 6
      cs_invvn02c
                                      >
                                                        0
                                                                     8
                                                                         0
                                                                             0.000
                                                            0.000
                                14c
                                            NOT
                                                    8
 1
      cs invvn14c
                                      >
                                                                             0.000
                                                                     6
                                                                         0
                                04c
                                      >
                                            NOT
                                                    2
                                                        0
                                                            0.000
 3
      cs_invvn04c
                                            NOT
                                                   25
                                                         0
                                                            0.000
                                                                     25
                                                                          0
                                                                              0.000
                                19c
 1
      cs_invvn19c
                                      >
                                                            0.000
                                                                     28
                                                                          0
                                                                              0.000
                                            NOT
                                                   14
                                16c
                                                         0
 2
      cs_invvn16c
                                      >
                                                                     28
                                                                              0.000
                                                         0
                                                             0.000
                                                                           0
                                 10c
                                       >
                                             OAI
                                                   14
 2
      cs oa21n10c
                                                                             0.000
                                                         0
                                                            0.000
                                                                     6
                                                                          0
                                                    6
 1
      cs oa22n03c
                                 03c
                                       >
                                             OAI
                                                                    550
                                                                           0
                                                                              0.000
                                                             0.000
 22
                                07c
                                            REG
                                                   25
                                                         0
      cl_invvn07c
                                      >
                                                             0.000
                                                                    750
                                                                           0
                                                                               0.000
                                07d
                                            REG
                                                   25
                                                         0
 30
       cl_invvn07d
                                      >
```

```
18
    cl_nnd2n07c
                           07c
                                     REG
                                           26
                                                   0.000 468
                                                 0
                                                                0.000
    cl_ao22n07c
8
                          07c
                                >
                                     REG
                                           33
                                                0
                                                   0.000
                                                          264
                                                                0.000
2
    cl_nnd3n07c
                          07c
                                >
                                     REG
                                           29
                                                0
                                                   0.000
                                                          58
                                                               0
                                                                  0.000
1
    cl_nor2n06c
                          06c
                               >
                                     REG
                                           26
                                                0
                                                   0.000
                                                          26
                                                               0
                                                                  0.000
1
    cl_ao21n07c
                          07c
                                     REG
                                           30
                                                          30
                                                0
                                                   0.000
                                                               0
                                                                  0.000
1
    cl_oa21n07c
                          07c
                                     REG
                                           30
                                                          30
                                                0
                                                   0.000
                                                               0
                                                                  0.000
1
    cb_mode_block
                                > SEQUENTIAL
                                                70
                                                     0.000
                                                               70
                                                                    0.000
    cb_clk_32_1
6
                              > SEQUENTIAL
                                              80
                                                   0 0.000 480
                                                                  0.000
1
    cs_xbn2n01b
                                     XNOR
                           01b
                                             8
                                                 0
                                                    0.000
                                                            8
                                                                0.000
                                >
    cs_xbo2n01d
1
                           01d
                                     XOR
                                                   0.000
                                                           8
                                            8
                                                0
                                                               0
                                                                  0.000
```

```
# of
Levels Output
        1
  1
        55
              50* plus *****
 2
        1
 3
        8
 4
        1
 10
 11
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 2
       20
 3
        1
 4
        5
 5
        3
 6
        10
 7
        3
 9
        1
 10
         6
 12
         1
         2
 13
 14
         4
 15
        10
 16
        3
 17
        14
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net								
	# of Fanout Nets							
ranou								
1	945	900* plus ************************************						
2	101	100* plus *						
3	41	********						
4	16	****						
5	8	*****						
6	11	******						
7	2	**						
8	4	***						
13	3	********						
14	16	*						
15	1							
[End o	[End of measure]							
[measure]: Execution time was 0.6 seconds.								
Prim	ary Inp	<idcdsuc> has:  outs = 122  utouts = 73</idcdsuc>						

The model <idcdsuc> I</idcdsuc>	nas:
Primary Inputs =	122
Primary Outputs =	73
Primary BIDIs =	0 .
Signals =	1148
Gate Count =	927
Connections =	1764
Master REG Bits =	83
Slave REG Bits =	<b>83</b> .
Internal Area =	4533
External Area =	0
Gates/Connects =	0.525510
Fanout Count =	1764
Average Fanout =	1.536585
Avg Tech Box Size =	4.889968
Tech Box Size Stddev =	0.010696
Power =	0.000000
***R-E-A-L***S-T-A-T-I-S-	T-I-C-S***
TEXE OTATIO	

#### Real signals 773 Real boxes 552 1389 Real connections = 2162 Real LSTs 8.211957 Real ICells/box 3.916667 Real LSTs/box 1.400362 =

Real nets/box Cell Total Each Cell

Type C	nt Boxname	Powe	r Level	Fund	ction	Int	Ext	Power	Int	Ext	Power
7	cs_ao22n03c	03c	>					42			
4	cs_ao12n03c	03c	>	AOI	4	0	0.000	16	0	0.000	
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000	

```
cs_ao12n04c
 1
                               04c
                                           AOI
                                     >
                                                  4
                                                       0
                                                          0.000
                                                                   4
                                                                       0
                                                                          0.000
180
      BRKPT
                                                  0
                                                                       0
                                   >
                                        BRKPT
                                                      0
                                                          0.000
                                                                  0
                                                                          0.000
195
      IOPAD
                                   >
                                       IOPAD
                                                 0
                                                      0
                                                         0.000
                                                                  0
                                                                      0
                                                                          0.000
164
      cs_nnd2n02c
                                02c
                                            NAND
                                                     3
                                                             0.000
                                                                     492
                                                                           0
                                                                               0.000
                                      >
                                                          0
                                                            0.000
 1
     cs_nnd2n10c
                                10c
                                           NAND
                                                    8
                                                         0
                                                                     8
                                                                            0.000
                                     >
24
      cs_nnd3n02c
                                02c
                                           NAND
                                                     4
                                                         0
                                                            0.000
                                                                     96
                                                                          0
                                                                             0.000
                                      >
 2
     cs_nnd2n05c
                               05c
                                                    4
                                           NAND
                                                         0
                                                            0.000
                                                                     8
                                                                         0
                                                                            0.000
                                     >
 5
     cs_nnd4n03c
                               03c
                                           NAND
                                                    5
                                                         0
                                                            0.000
                                                                    25
                                                                             0.000
                                     >
                                                                          0
 1
     cs nnd2n13c
                               13c
                                           NAND
                                                         0
                                                            0.000
                                     >
                                                    15
                                                                    15
                                                                          0
                                                                             0.000
     cs_nnd2n04c
 3
                               04c
                                           NAND
                                                    3
                                     >
                                                         0
                                                            0.000
                                                                     9
                                                                         0
                                                                            0.000
     cs nnd3n07c
                               07c
                                           NAND
 1
                                     >
                                                    6
                                                         0
                                                            0.000
                                                                     6
                                                                         0
                                                                            0.000
 1
     cs_nnd2n14e
                                14e
                                      >
                                           NAND
                                                    19
                                                         0
                                                            0.000
                                                                     19
                                                                          0
                                                                             0.000
 2
     cs nnd2n03c
                               03c
                                     >
                                           NAND
                                                    3
                                                         0
                                                            0.000
                                                                     6
                                                                         0
                                                                            0.000
 3
     cs_nnd2n07c
                               07c
                                     >
                                           NAND
                                                    4
                                                         0
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
 2
     cs_nnd2n11c
                               11c
                                     >
                                           NAND
                                                         0
                                                            0.000
                                                                     22
                                                                          0
                                                                             0.000
                                                    11
 1
     cs nnd2n14b
                               14b
                                           NAND
                                                    20
                                                         0
                                                             0.000
                                                                     20
                                                                          0
                                                                              0.000
                                      >
 1
     cs_nnd3n12c
                               12c
                                           NAND
                                                   22
                                                         0
                                                            0.000
                                                                     22
                                                                          0
                                                                             0.000
                                     >
 1
     cs_nnd4n06c
                               06c
                                                         0
                                     >
                                           NAND
                                                    8
                                                            0.000
                                                                     8
                                                                         0
                                                                            0.000
 6
     cs nnd2n14c
                               14c
                                           NAND
                                                   19
                                                            0.000
                                     >
                                                         0
                                                                    114
                                                                           0
                                                                              0.000
                               10c
                                           NAND
                                                            0.000
                                                                    20
 1
     cs nnd4n10c
                                                   20
                                                         0
                                                                             0.000
                                     >
                                                                          0
     cs_nnd2n06c
 1
                               06c
                                           NAND
                                     >
                                                    4
                                                         0
                                                            0.000
                                                                     4
                                                                         0
                                                                            0.000
     cs nnd3n05c
                               05c
                                           NAND
                                                    6
                                                            0.000
 1
                                     >
                                                         0
                                                                     6
                                                                         0
                                                                            0.000
     cs_nnd2n12c
                                                   12
                               12c
                                           NAND
                                                         0
 1
                                     >
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
     cs_nnd3n10c
 1
                               10c
                                     >
                                           NAND
                                                   12
                                                         0
                                                            0.000
                                                                     12
                                                                          0
                                                                             0.000
10
                               02c
                                           NOR
                                                        0
                                                           0.000
      cs_nor2n02c
                                     >
                                                   3
                                                                   30
                                                                         0
                                                                            0.000
 1
                               03c
                                           NOR
                                                   4
                                                       0
                                                           0.000
                                                                           0.000
     cs_nor3n03c
                                     >
                                                                   4
                                                                        0
     cs_nor2n12c
                               12c
                                           NOR
                                                  12
                                                        0
                                                                    12
                                                                         0.000
1,
                                     >
                                                           0.000
 1
     cs nor2n04c
                               04c
                                           NOR
                                                   3
                                                       0
                                                           0.000
                                                                   3
                                                                        0
                                                                           0.000
                                     >
- 1
     cs_nor3n10c
                               10c
                                           NOR
                                                  12
                                                        0
                                                           0.000
                                     >
                                                                   12
                                                                         0
                                                                           0.000
 1
     cs_nor2n09c
                               09c
                                     >
                                           NOR
                                                   7
                                                       0
                                                           0.000
                                                                   7
                                                                        0
                                                                           0.000
89
      cs_invvn01c
                               01c
                                     >
                                           NOT
                                                   2
                                                       0
                                                          0.000
                                                                  178
                                                                         0
                                                                            0.000
4
     cs invvn11c
                              11c
                                     >
                                          NOT
                                                  6
                                                       0
                                                          0.000
                                                                  24
                                                                        0
                                                                           0.000
6
     cs_invvn10c
                              10c
                                          NOT
                                                  4
                                                       0
                                                          0.000
                                                                  24
                                                                           0.000
                                     >
                                                                        0
22
      cs invvn12c
                               12c
                                           NOT
                                                   6
                                                       0
                                                          0.000
                                                                  132
                                                                         0
                                                                            0.000
                                     >
7
     cs invvn09c
                              09c
                                          NOT
                                                  4
                                                       0
                                                          0.000
                                                                  28
                                                                        0
                                                                           0.000
                                    >
28
      cs_invvn07c
                               07c
                                           NOT
                                                   2
                                                       0
                                                         . 0.000
                                                                        0
                                     >
                                                                   56
                                                                           0.000
4
     cs_invvn15c
                                                  10
                              15c
                                     >
                                          NOT
                                                       0
                                                          0.000
                                                                   40
                                                                        0
                                                                            0.000
11
      cs invvn06c
                               06c
                                     >
                                           NOT
                                                   2
                                                       0
                                                          0.000
                                                                   22
                                                                        0
                                                                           0.000
12
      cs_invvn05c
                               05c
                                     >
                                           NOT
                                                   2
                                                       0
                                                          0.000
                                                                   24
                                                                        0
                                                                            0.000
5
     cs_invvn13c
                                                  8
                              13c
                                     >
                                          NOT
                                                       0
                                                          0.000
                                                                  40
                                                                        0
                                                                           0.000
 1
     cs invvn14b
                              14b
                                          NOT
                                                  10
                                                       0
                                                          0.000
                                     >
                                                                   10
                                                                        0
                                                                            0.000
 4
     cs_invvn08c
                              08c
                                                  4
                                          NOT
                                                       0
                                                          0.000
                                                                  16
                                                                        0
                                    >
                                                                           0.000
 6
     cs_invvn02c
                              02c
                                                  2
                                    >
                                          NOT
                                                       0
                                                          0.000
                                                                  12
                                                                        0
                                                                           0.000
     cs invvn14c
                              14c
                                          NOT
                                                  8
                                                          0.000
 1
                                    >
                                                       0
                                                                   8
                                                                       0
                                                                           0.000
 3
                              04c
                                          NOT
                                                  2
                                                          0.000
     cs_invvn04c
                                                       0
                                                                   6
                                                                       0
                                                                           0.000
                                    >
 1
     cs invvn19c
                              19c
                                          NOT
                                                 25
                                                                   25
                                     >
                                                       0
                                                          0.000
                                                                        0
                                                                           0.000
2
     cs invvn16c
                                          NOT
                                                          0.000
                              16c
                                    >
                                                 14
                                                       0
                                                                   28
                                                                        0
                                                                            0.000
 2
                                                 14
     cs_oa21n10c
                               10c
                                           OAI
                                                       0
                                                          0.000
                                                                   28
                                                                        0
                                     >
                                                                            0.000
     cs_oa22n03c
 1
                               03c
                                     >
                                           OAI
                                                  6
                                                       0
                                                          0.000
                                                                   6
                                                                       0
                                                                           0.000
22
      cl invvn07c
                                          REG
                                                 25
                                                          0.000
                              07c
                                    >
                                                       0
                                                                  550
                                                                         0
                                                                            0.000
30
      cl_invvn07d
                              07d
                                     >
                                          REG
                                                  25
                                                       0
                                                           0.000
                                                                  750
                                                                         0
                                                                            0.000
18
      cl_nnd2n07c
                                                  26
                               07c
                                     >
                                           REG
                                                        0
                                                           0.000
                                                                   468
                                                                          0
                                                                             0.000
8
     cl_ao22n07c
                                                  33
                                                           0.000
                              07c
                                     >
                                           REG
                                                       0
                                                                  264
                                                                         0
                                                                             0.000
 2
     cl_nnd3n07c
                              07c
                                          REG
                                                  29
                                                       0
                                                           0.000
                                                                   58
                                                                         0
                                                                            0.000
                                     >
     cl_nor2n06c
                              06c
                                          REG
                                                 26
                                                          0.000
                                                                   26
                                                                        0
                                                                           0.000
```

```
0.000
                          07c
                                    REG
                                          30
                                                0
                                                   0.000
                                                          30
                                                               0
   cl_ao21n07c
                               >
1
                                    REG
                                          30
                                                0
                                                  0.000
                                                          30
                                                               0.000
                          07c
                               >
   cl_oa21n07c
1
                                                     0.000
                                                              70
                                                                    0.000
                                               70
                               > SEQUENTIAL
1
   cb_mode_block
                                                                  0.000
   cb_clk_32_1
                              > SEQUENTIAL
                                             80
                                                     0.000
                                                            480
6
                                                           8
                                                                 0.000
                                    XNOR
                                             8
                                                 0
                                                   0.000
                                                               0
    cs_xbn2n01b
                          01b
1
                                                                 0.000
                                            8
                                                0
                                                   0.000
                                                          8
                                                               0
                          01d
                                >
                                     XOR
1
    cs_xbo2n01d
```

### # of Levels Output 50\* plus \*\*\*\*\*

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 2
        20
 3
        1
 4
        5.
 5
        3
 6
        10
  7
        3
 9
        1
 10
         6
 12
         1
         2
 13
         4
 14
 15
         10
 16
         3
 17
         14
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

# of

```
Fanout Nets
  1
       945
              900* plus ***
  2
              100* plus *
       101
  3
       41
  4
        16
  5
        8
  6
        11
  7
        2
 8
        4
 13
        3
 14
        16
 15
        1
[End of measure]
[measure]: Execution time was 0.6 seconds.
       > quick tcte(SCORE(ALL),NO VIOLATIONS)
>>]: [quick]:( tcte(SCORE(ALL),NO_VIOLATIONS) );
-1993.41 Avg: -212.60
[BD-500000]: tcte CMVC version 1.6 compiled on Apr 13 1999 at 18:26:19
-1993.41 Avg: -212.60
maximum area for proto box IDCDSUC is 4533.
[quick]: Number of boxes to process is 927.
[quick]: Number of boxes processed is 0.
-1993.41 Avg: -208.85
[BD-502200]: Combined 4 gates.
[tcte]: Execution time was 0.2 seconds.
      > measure
The model <IDCDSUC> has:
 Primary Inputs
                              122
 Primary Outputs
                                73
 Primary BIDIs
                               0
 Signals
                           1144
 Gate Count
                              923
 Connections
                              1760
 Master REG Bits
                                83
 Slave REG Bits
                               83
 Internal Area
                             4525
External Area
                               0
Gates/Connects
                             0.524432
Fanout Count
                              1760
Average Fanout
                             1.538462
Avg Tech Box Size
                              4.902492
Tech Box Size Stddev =
                               0.010763
Power
                         0.000000
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
Real signals
                             769
Real boxes
                             548
Real connections
                               1385
Real LSTs
                             2154
Real ICells/box
                           8.257299
```

Real LSTs/box 3.930657 1.403285 Real nets/box Total Cell Cell Each Power Level Function Int Ext Power Int Ext Power Type Cnt Boxname 42 0 0.000 **AOI** 0 0.000 6 03c 7 cs\_ao22n03c > 16 0 0.000 **AOI** 4 0 0.000 03c > 4 cs ao12n03c 0.000 18 0 18 0 0.000 10c > AOI cs\_ao22n10c 1 0.000 4 0.000 4 0 04c AOI 0 cs ao12n04c 1 0.000 **BRKPT** 0 0 0.000 n 0 **BRKPT** 180 0 0 0.000 **IOPAD** 0-0 0.000 **IOPAD** > 195 492 0 0.000 02c **NAND** 3 0.000 O cs nnd2n02c > 164 8 0.000 0.000 0 10c **NAND** 8 0 cs nnd2n10c > 1 0.000 96 0 02c NAND 4 0 0.000 24 cs\_nnd3n02c > 0.000 8 0 0.000 NAND 4 0 05c 2 cs nnd2n05c > 0 0.000 5 0 0.000 25 03c NAND cs\_nnd4n03c > 5 15 0 0.000 15 0 0.000 13c NAND cs\_nnd2n13c > 1 0 0.000 9 0 0.000 NAND 3 cs nnd2n04c 04c > 3 6 0 0.000 0 0.000 cs\_nnd3n07c 07c > NAND 6 1 0.000 **NAND** 19 0 0.000 19 0 14e > 1 cs\_nnd2n14e 0.000 **NAND** 3 0 0.000 6 0 03c 2 cs\_nnd2n03c 0 0.000 0 0.000 12 07c NAND 4 > 3 cs nnd2n07c 0.000 0.000 22 0 NAND 11 0 11c 2 cs nnd2n11c > 0.000 20 0 0.000 20 0 **NAND** 14b 1 cs nnd2n14b 0.000 0.000 22 0 22 0 NAND cs\_nnd3n12c 12c > 1 0 0.000 NAND 0 0.000 8 06c 8 cs\_nnd4n06c > 1 0.000 0 0:000 19 0 114 NAND cs nnd2n14c 14c > 6 20 0 0.000 0 0.000 20 cs nnd4n10c 10c > NAND 1 0 0.000 **NAND** 0 0.000 4 06c > 4 1 cs\_nnd2n06c 0.000 6 0 0.000 **NAND** 6 0 cs nnd3n05c 05c > 1 12 0 0.000 0 0.000 cs\_nnd2n12c 12c > NAND 12 1 12 0 0.000 10c > NAND 12 0 0.000 cs\_nnd3n10c 1 NOR 0 0.000 02c 3 0 0.000 30 cs\_nor2n02c > 10 4 0 0.000 03c NOR 4 0 0.000 > cs\_nor3n03c 1 12c NOR 12 0.000 12 0 0.000 cs nor2n12c > 1 0 0.000 NOR 3 0 0.000 3 cs\_nor2n04c 04c > 1 12 0.000 **NOR** 12 0 0.000 0 10c cs nor3n10c > 1 NOR 7 0 0.000 7 0 0.000 09c > cs\_nor2n09c 1 2 0 0.000 178 0 0.000 NOT 01c 89 cs invvn01c > 0.000 24 0 0.000 6 0 11c NOT cs invvn11c > 4 0 0.000 4 0 0.000 24 10c > NOT 6 cs\_invvn10c 0 0.000 6 0 0.000 132 NOT 12c > 22 cs invvn12c 0. 0.000 0.000 28 0 cs\_invvn09c 09c > NOT 4 7 0 2 0 0.000 48 0.000 07c > NOT 24 cs\_invvn07c 0 0.000 0 0.000 40 15c NOT 10 4 cs invvn15c > 0.000 0 0.000 22 0 06c NOT 2 cs\_invvn06c > 11 0 0.000 24 0 0.000 05c NOT 2 12 cs\_invvn05c > 0.000 40 0 0.000 0 13c > NOT 8 5 cs invvn13c 0.000 0.000 10 0 14b > NOT 10 0 cs invvn14b 1 0.000 0 0.000 08c NOT 4 0 16 4 cs invvn08c > 0 0.000 2 0 0.000 12 02c > NOT 6 cs invvn02c NOT 8 0 0.000 8 0 0.000 14c > 1 cs\_invvn14c 2 0.000 6 0 0.000 0 3 cs invvn04c 04c > NOT 25 0 0.000 25 0 0.000 19c > NOT cs\_invvn19c 1

```
2
    cs_invvn16c
                           16c
                                      NOT
                                             14
                                                  0
                                                     0.000
                                                             28
                                                                  0
                                                                     0.000
2
    cs_oa21n10c
                            10c
                                       OAL
                                             14
                                                  0
                                                     0.000
                                                             28
                                                                  0.000
1
    cs_oa22n03c
                            03c
                                       OAI
                                              6
                                                  0
                                                     0.000
                                                             6
                                                                 0.000
22
     cl_invvn07c
                           07c
                                      REG
                                             25
                                 >
                                                  0
                                                     0.000
                                                            550
                                                                  0.000
30
     cl_invvn07d
                           07d
                                      REG
                                             25
                                 >
                                                  0
                                                     0.000
                                                            750
                                                                      0.000
                                                                  0
18
     cl_nnd2n07c
                            07c
                                             26
                                       REG
                                                      0.000
                                                            468
                                                                   0
                                                                      0.000
8
    cl_ao22n07c
                            07c
                                 >
                                       REG
                                             33
                                                      0.000
                                                  0
                                                            264
                                                                   0.000
2
    cl_nnd3n07c
                            07c
                                 >
                                       REG
                                             29
                                                  0
                                                      0.000
                                                             58
                                                                  0
                                                                     0.000
1
    cl_nor2n06c
                           06c
                                 >
                                      REG
                                             26
                                                  0
                                                     0.000
                                                             26
                                                                  0
                                                                     0.000
1
    cl_ao21n07c
                            07c
                                 >
                                       REG
                                             30
                                                  0
                                                     0.000
                                                             30
                                                                  0
                                                                     0.000
1
    cl_oa21n07c
                            07c
                                       REG
                                             30
                                                  0
                                                     0.000
                                                             30
                                                                  0
                                                                     0.000
    cb_mode_block
1
                                 > SEQUENTIAL
                                                  70
                                                        0.000
                                                                  70
                                                                       0.000
6
    cb_clk_32 1
                                > SEQUENTIAL
                                                80
                                                     0 0.000 480
                                                                     0.000
1
    cs_xbn2n01b
                            01b
                                       XNOR
                                                   0
                                 >
                                               8
                                                              8
                                                                  0
                                                      0.000
                                                                     0.000
1
    cs_xbo2n01d
                            01d
                                       XOR:
                                                                     0.000
                                              8
                                                   0
                                                      0.000
                                                              8
                                                                  0
```

```
# of
Levels Output
         1
        55
 1
              50* plus **
 2
        1
 3
        8
 4
        1
 10
 11
         1.
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 2
       20
 3
        1
 4
        5
 5
        3
 6
       10
 7
        3
 9
        1
10
        6
12
        1
13
        2
14
        4
15
        10
16
        3
17
        14
```

The Histogram Of Fanin vs. Box

```
# of
Fanin Ops
```

```
382
              350* plus *****
 1
 2
      203
              200* plus ***
 3
       37
       16
The Histogram Of Fanout vs. Net
   # of
Fanout Nets
       943
              900* plus **
 1
       100
              100* plus
 2
 3
       41
 4
       16
 5
        7
 6
       11
 7
        2
 8
        4
        3
 13
 14
        16
 20
         1
[End of measure]
[measure]: Execution time was 0.6 seconds.
        > tc_parm CAP_LIM(200)
> tc_parm CAP_LIM(100)
       > fanmatch ESTIMATED, SORT, ONE_LEVEL
>>]: ltorbox( dfanmatch(ESTIMATED,SORT,ONE_LEVEL) );
[BD-500000]: fanmatch CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32
setting ESTIMATED option.
setting SORT option.
setting ONE_LEVEL option.
-1993.41 Avg: -208.85
[BD-500300]: 137 pins on 66 gates swapped.
-1978.06 Avg: -206.71
[fanmatch]: Execution time was 1.4 seconds.
       > measure
 The model <IDCDSUC> has:
                               122
 Primary Inputs
 Primary Outputs
                                 73
                                0
 Primary BIDIs
                            1144
 Signals
                               923
 Gate Count
                               1760
 Connections
 Master REG Bits
                                 83
                                 83
 Slave REG Bits
                              4525
 Internal Area
 External Area
                                0
                              0.524432
  Gates/Connects
 Fanout Count
                               1760
  Average Fanout
                              1.538462
```

Avg Tech Box Size = 4.902492 Tech Box Size Stddev = 0.010763 Power 0.000000 \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\* Real signals = 769 Real boxes 548 Real connections 1385 Real LSTs 2154 Real ICells/box 8.257299 = Real LSTs/box 3.930657 Real nets/box 1.403285 Cell Total Each Cell Type Cnt Boxname Power Level Function Int Ext Power Int Ext Power 7 cs\_ao22n03c 03c AOI 6 0 0.000 42 0 0.000 > 4 cs\_ao12n03c 03c AOI 4 0 0.000 16 0.000 > 0 1 cs\_ao22n10c 10c 18 0 AOI 0.000 18 0 0.000 1 cs\_ao12n04c 04c AOI 0.000 4 0 4 0 0.000 180 **BRKPT BRKPT** 0 0 0.000 0 0 0.000 > 195 **IOPAD** IOPAD 0 0 0.000 0 0 0.000 164 cs nnd2n02c 02c **NAND** 3 0 0.000 492 0.000 1 cs\_nnd2n10c 10c NAND 8 0.000 8 > 0 0 0.000 24 cs nnd3n02c 02c NAND 4 0 0.000 96 0. 0.000 2 cs nnd2n05c 05c > NAND 4 0 0.000 8 0 0.000 5 cs nnd4n03c 03c > NAND 5 0.000 25 0 0 0.000 1 cs\_nnd2n13c 13c **NAND** 0 > 15 0.000 15 0 0.000 3 cs\_nnd2n04c 04c > **NAND** 3 0 0.000 9 0 0.000 cs\_nnd3n07c 1 07c **NAND** 6 > 0 0.000 6 0 0.000 1 cs\_nnd2n14e 14e **NAND** 19 0 > 0.000 19 0 0.000 2 cs\_nnd2n03c 03c NAND 3 0.000 0 6 0 0.000 3 cs nnd2n07c 07c > NAND 4 0.000 0 12 0 0.000 2 cs\_nnd2n11c 11c NAND 0 > 11 0.000 22 0 0.000 1 cs\_nnd2n14b 14b > NAND 20 0 0.000 20 0 0.000 cs nnd3n12c 12c 0.000 > NAND 22 0 0.000 22 0 cs\_nnd4n06c 06c 1 > NAND 8 0 0.000 8 0 0.000 6 cs nnd2n14c 14c > NAND 19 0 0.000 114 0 0.000 1 cs nnd4n10c 10c > NAND 20 0 0.000 20 0 0.000 1 cs\_nnd2n06c 06c > **NAND** 4 0 0.000 4 0 0.000 1 cs\_nnd3n05c 05c > NAND 6 0 0.000 6 0 0.000 1 cs\_nnd2n12c 12c > **NAND** 12 0 0.000 12 0 0.000 1 cs\_nnd3n10c 10c > **NAND** 12 0 0.000 12 0 0.000 10 cs\_nor2n02c 02c NOR 0 > 3 0.000 30 0 0.000 1 cs\_nor3n03c 03c NOR 4 > 0 0.000 4 0.000 0 1 cs\_nor2n12c 12c NOR 12 0 0.000 12 > 0 0.000 1 cs\_nor2n04c 04c NOR 3 > 0 0.000 3 0 0.000 12 1 cs\_nor3n10c 10c **NOR** > 0 0.000 12 0.000 0 1 cs nor2n09c 09c **NOR** 7 0 0.000 > 7 0.000 89 2 cs\_invvn01c 01c > NOT 0 0.000 178 0.000 4 cs invvn11c NOT 6 0.000 11c > 0 24 0 0.000 6 cs invvn10c 10c NOT > 4 0 0.000 24 0 0.000 22 cs\_invvn12c 12c > NOT 6 0 0.000 132 0 0.000 7 cs invvn09c 09c NOT 4 0 0.000 28 > 0 0.000

2

0

0.000

48

0

0.000

NOT

07c

24

cs\_invvn07c

```
0.000
                                                       0.000
                                                                    0
                                       NOT
                                               10
                                                    0
                                                               40
                            15c
                                  >
4
    cs_invvn15c
                                        NOT
                                               2
                                                    0
                                                       0.000
                                                               22
                                                                    0
                                                                       0.000
                             06c
                                  >
11
     cs_invvn06c
                                               2
                                                    0
                                                       0.000
                                                               24
                                                                    0
                                                                       0.000
                                        NOT
     cs invvn05c
                             05c
12
                                  >
                                                                       0.000
                                                   0
                                                      0.000
                                                              40
                                                                    0
                            13c
                                  >
                                       NOT
                                               8
    cs_invvn13c
5
                                                       0.000
                                                               10
                                                                    0
                                                                      0.000
                            14b
                                        NOT
                                               10
                                                    0
    cs_invvn14b
                                  >
1
                                                                       0.000
                                       NOT
                                               4
                                                   0
                                                       0.000
                                                              16
                                                                    0
                            08c
4
    cs_invvn08c
                                  >
                                                                       0.000
                                       NOT
                                               2
                                                   0
                                                       0.000
                                                              12
                                                                    0
                            02c
6
    cs invvn02c
                                  >
                                                       0.000
                                                                      0.000
                                               8
                                                   0
                                                               8
                                                                   0
                                        NOT
    cs_invvn14c
                            14c
                                  >
1
                                                                   0.000
                                               2
                                                      0.000
                                                               6
                                                   0
                            04c
                                  >
                                        NOT
3
    cs_invvn04c
                                                                    0
                                                                       0.000
                                                    0
                                                       0.000
                                                               25
                            19c
                                  >
                                        NOT
                                               25
1
    cs invvn19c
                                                               28
                                                                       0.000
                                                       0.000
                                                                    0
                                        NOT
                                               14
                                                    0
                            16c
                                  >
2
    cs_invvn16c
                                                               28
                                                                    0.000
                                         OAI
                                               14
                                                    0
                                                       0.000
                             10c
                                  >
2
    cs_oa21n10c
                                         OAI
                                               6
                                                    0
                                                       0.000
                                                               6
                                                                   0.000
                             03c
1
    cs oa22n03c
                                  >
                                               25
                                                    0
                                                       0.000
                                                              550
                                                                     0
                                                                        0.000
                            07c
                                        REG
22
     cl_invvn07c
                                  >
                                                                        0.000
                                                              750
                            07d
                                        REG
                                               25
                                                    0
                                                       0.000
                                                                     0
                                  >
30
     cl_invvn07d
                                                               468
                                                                         0.000
                                         REG
                                               26
                                                     0
                                                       0.000
                                                                      0
                             07c
18
     cl_nnd2n07c
                                  >
                                                        0.000
                                                               264
                                                                        0.000
                                                                     0
                             07c
                                        REG
                                               33
                                                    0
    cl ao22n07c
                                  >
8
                                                                        0.000
                                               29
                                                    0
                                                        0.000
                                                               58
                                                                     0
                             07c
                                        REG
2
    cl nnd3n07c
                                   >
                                                                        0.000
                                                       0.000
                                                               26
                                                                    0
                                               26
                                                    0
                            06c
                                        REG
1
    cl nor2n06c
                                                                     0
                                                                        0.000
                                                               30
                                                     0
                                                       0.000
                             07c
                                  >
                                        REG
                                               30
1
    cl_ao21n07c
                                                                     0
                                                                        0.000
                                               30
                                                     0
                                                        0.000
                                                               30
                                   >
                                        REG
    cl oa21n07c
                             07c
1
                                                          0.000
                                                                     70
                                                                          0.000
                                  > SEQUENTIAL
                                                    70
    cb mode_block
1
                                                       0 0.000 480
                                                                        0.000
                                                  80
                                 > SEQUENTIAL
6
    cb_clk_32_1
                                                                 8
                                                                     0
                                                                        0.000
                                        XNOR
                                                 8
                                                      0
                                                         0.000
                             01b
                                   >
1
     cs_xbn2n01b
                                                                        0.000
                                                     0.000
                                                                8
                                                                     0
    cs_xbo2n01d
                             01d
                                         XOR
                                                8
1
```

```
# of
Levels Output
 0
       1
              50* plus
        55
  1
 2
        1
  3
        8
  4
        1
 10
         3
 11
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
        20
 2
 3
        1
 4
        5
              ****
 5
              ***
        3
 6
        10
 7
        3
 9
        1
 10
         6
 12
         1
```

```
13
         2
  14
         4
  15
        10
  16
         3
 17
        14
The Histogram Of Fanin vs. Box
    # of
Fanin
         Ops
  1
       382
              350* plus ****
  2
       203
              200* plus ***
  3
        37
  4
        16
The Histogram Of Fanout vs. Net
    # of
Fanout Nets
       943
  1
              900* plus
  2
       100
              100* plus
  3
       41
  4
       .16
  5
  8
        3
 13
 14
        16
[End of measure]
[measure]: Execution time was 0.7 seconds.
       > treematch ESTIMATED, TWO_LEVEL, NO_VIOLATIONS
>>]: ltorbox( dtreematch(ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
[BD-500000]: treematch CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1978.06 Avg: -206.71
[BD-500301]: 5 pins on 2 gates swapped.
-1978.02 Avg: -210.98
[treematch]: Execution time was 0.2 seconds.
      > measure
The model <IDCDSUC> has:
Primary Inputs
                              122
Primary Outputs
                               73
Primary BIDIs
                               0
Signals
                           1144
```

923

**Gate Count** 

```
Connections
                               83
Master REG Bits
                              83
Slave REG Bits
                            4525
Internal Area
                              0
External Area
                            0.524432
Gates/Connects
                             1760
Fanout Count
                            1.538462
Average Fanout
                             4.902492
Ava Tech Box Size
                              0.010763
Tech Box Size Stddev =
                        0.000000
Power
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
                            769
Real signals
                =
                            548
Real boxes
                              1385
Real connections
                            2154
Real LSTs
                          8.257299
Real ICells/box
                           3.930657
Real LSTs/box
                           1.403285
 Real nets/box
 Cell
               Total
                Cell
 Each
                                                        Int Ext Power
                                                                         Int Ext
                                                                                   Power
Type Cnt Boxname
                                Power Level Function
                                                        0...
                                                           0.000
                                                                   42
                                                                         0
                                                                            0.000
                                03c
                                            AOI
                                                   6
  7
                                     · >
      cs ao22n03c
                                                        0
                                                           0.000
                                                                    16
                                                                         0
                                                                            0.000
                                03c
                                             AOI
                                                   4
      cs ao12n03c
                                       >
  4
                                                            0.000
                                                                    18
                                                                          0
                                                                            0.000
                                                   18
                                                        0
                                 1.0c
                                             AOI
  1
      cs ao22n10c
                                      .>
                                                                    4
                                                   4
                                                        0
                                                           0.000
                                                                         0
                                                                            0.000
                                 04c
                                             AOI
  1
      cs_ao12n04c
                                         BRKPT
                                                           0.000
                                                                    0
                                                                        0
                                                                            0.000
                                                   0
                                                        0
 180
       BRKPT
                                                                       0
                                                                           0.000
                                                       0
                                                          0.000
                                                                   0
                                        IOPAD
                                                  0
 195
       IOPAD
                                    >
                                                                      492
                                                              0.000
                                                                             0.000
                                             NAND
                                                      3
                                                           0
                                 02c
 164
        cs nnd2n02c
                                        >
                                                                      8
                                                                          0
                                                                              0.000
                                            NAND
                                                     8
                                                          0
                                                             0.000
  1
      cs nnd2n10c
                                 10c
                                       >
                                                                           0
                                                                              0.000
                                                          0
                                                             0.000
                                                                      96
                                            NAND
 24
       cs_nnd3n02c
                                 02c
                                       >
                                                      4
                                                                              0.000
                                                                          0
                                            NAND
                                                     4
                                                          0
                                                             0.000
                                                                      8
  2
       cs_nnd2n05c
                                 05c
                                       >
                                                                     25
                                                                           0
                                                                              0.000
                                                     5
                                                          0
                                                             0.000
  5
       cs nnd4n03c
                                 03c
                                       >
                                            NAND
                                                                           0
                                                                              0.000
                                                          0
                                                             0.000
                                                                      15
  1
      cs_nnd2n13c
                                 13c
                                       >
                                            NAND
                                                     15
                                            NAND
                                                     3
                                                          0
                                                             0.000
                                                                      9
                                                                          0
                                                                              0.000
                                 04c
                                       >
  3
       cs_nnd2n04c
                                            NAND
                                                     6
                                                          0
                                                             0.000
                                                                      6
                                                                          0
                                                                              0.000
                                 07c
       cs_nnd3n07c
                                       >
  1
                                                              0.000
                                                                      19
                                                                            0
                                                                               0.000
                                 14e
                                            NAND
                                                     19
                                                           0
  1
       cs nnd2n14e
                                       >
                                                                          0
                                                                              0.000
                                 03c
                                            NAND
                                                     3
                                                          0
                                                             0.000
                                                                      6
  2
       cs nnd2n03c
                                       >
                                                                           0
                                                                              0.000
                                            NAND
                                                     4
                                                          0
                                                             0.000
                                                                     12
                                 07c
  3
       cs nnd2n07c
                                       >
                                                                               0.000
                                                     11
                                                          0
                                                              0.000
                                                                      22
                                                                            0
                                 11c
                                            NAND
  2
       cs nnd2n11c
                                       >
                                                     20
                                                           0
                                                              0.000
                                                                      20
                                                                            0
                                                                               0.000
                                 14b
                                            NAND
                                       >
  1
       cs_nnd2n14b
                                                     22
                                                          0
                                                              0.000
                                                                      22
                                                                            0.000
                                            NAND
                                 12c
  1
       cs nnd3n12c
                                       >
                                                                      8
                                                                           0
                                                                             0.000
                                                          0
                                                             0.000
                                 06c
                                            NAND
                                                     8
  1
       cs_nnd4n06c
                                       >
                                                                            0.000
                                                          0
                                                              0.000
                                                                     114
                                 14c
                                            NAND
                                                     19
  6
       cs_nnd2n14c
                                       >
                                                                      20
                                                                               0.000
                                                              0.000
                                                                            0
                                 10c
                                            NAND
                                                     20
                                                           0
       cs_nnd4n10c
  1
                                                                              0.000
                                 06c
                                            NAND
                                                     4
                                                          0
                                                             0.000
                                                                      4
                                                                           0
                                       >
  1
       cs_nnd2n06c
                                            NAND
                                                     6
                                                          0
                                                             0.000
                                                                      6
                                                                           0
                                                                              0.000
                                 05c
  1
       cs_nnd3n05c
                                       >
                                                                      12
                                                                            0
                                                                               0.000
                                                              0.000
                                                     12
                                                           0
  1
       cs_nnd2n12c
                                 12c
                                       >
                                            NAND
                                                                      12
                                                                               0.000
                                            NAND
                                                     12
                                                           0
                                                              0.000
                                                                            0
       cs nnd3n10c
                                 10c
                                       >
  1
                                                                     30
                                                                           0
                                                                              0.000
                                                     3
                                                         0
                                                            0.000
                                 02c
                                             NOR
  10
       cs nor2n02c
                                       >
                                                                             0.000
                                                                     4
                                03c
                                            NOR
                                                    4
                                                         0
                                                            0.000
                                                                          0
       cs_nor3n03c
                                       >
  1
                                                                     12
                                                                           0
                                            NOR
                                                    12
                                                         0
                                                             0.000
                                                                              0.000
                                 12c
  1
       cs_nor2n12c
                                       >
                                                    3
                                                            0.000
                                                                     3
                                                                          0
                                                                             0.000
                                            NOR
                                                         0
  1
       cs nor2n04c
                               · 04c
                                      >
                                                    12
                                                                     12
                                                                           0
                                                                              0.000
                                            NOR
                                                         0
                                                             0.000
       cs_nor3n10c
                                 10c
```

1760

```
1
     cs nor2n09c
                             09c
                                   >
                                         NOR
                                                 7
                                                      0
                                                        0.000
                                                                 7
                                                                      0.000
89
     cs_invvn01c
                             01c
                                   >
                                         NOT
                                                 2
                                                     0
                                                        0.000
                                                                178
                                                                       0
                                                                          0.000
4
     cs invvn11c
                             11c
                                   >
                                         NOT
                                                 6
                                                     0
                                                        0.000
                                                                24
                                                                         0.000
                                                                     0
6
     cs_invvn10c
                             10c
                                   >
                                         NOT
                                                 4
                                                        0.000
                                                                24
                                                     0
                                                                         0.000
                                                                     0
22
     cs_invvn12c
                             12c
                                   >
                                         NOT
                                                 6
                                                     0
                                                        0.000
                                                                132
                                                                          0.000
                                                                      0
7
     cs_invvn09c
                             09c
                                         NOT
                                                 4
                                                        0.000
                                                                28
                                   >
                                                     0
                                                                         0.000
                                                                     0
24
     cs_invvn07c
                                                 2
                             07c
                                         NOT
                                                     0
                                    >
                                                        0.000
                                                                48
                                                                      0
                                                                         0.000
4
     cs_invvn15c
                             15c
                                         NOT
                                                10
                                                        0.000
                                   >
                                                     0
                                                                40
                                                                      0
                                                                         0.000
11
     cs invvn06c
                             06c
                                         NOT
                                                 2
                                                        0.000
                                   >
                                                                22
                                                     0
                                                                      0
                                                                         0.000
12
                                                 2
     cs_invvn05c
                             05c
                                         NOT
                                                        0.000
                                   >
                                                     0
                                                                24
                                                                      0
                                                                         0.000
5
     cs_invvn13c
                             13c
                                   >
                                         NOT
                                                8
                                                     0
                                                        0.000
                                                                40
                                                                     0
                                                                         0.000
1
     cs_invvn14b
                             14b
                                   >
                                         NOT
                                                10
                                                     0
                                                        0.000
                                                                10
                                                                      0
                                                                         0.000
4
     cs_invvn08c
                             08c
                                   >
                                         NOT
                                                4
                                                     0
                                                        0.000
                                                                16
                                                                     0
                                                                         0.000
6
     cs_invvn02c
                             02c
                                   >
                                         NOT
                                                2
                                                     0
                                                        0.000
                                                                12
                                                                     0
                                                                         0.000
1
     cs_invvn14c
                             14c
                                         NOT
                                                8
                                                     0
                                                        0.000
                                                                     0
                                   >
                                                                8
                                                                        0.000
3
     cs_invvn04c
                             04c
                                         NOT
                                                2
                                                     0
                                                        0.000
                                                                     0
                                   >
                                                                6
                                                                        0.000
1
     cs_invvn19c
                             19c
                                         NOT
                                                25
                                                     0
                                                        0.000
                                                                25
                                   >
                                                                      0
                                                                         0.000
2
     cs_invvn16c
                             16c
                                         NOT
                                                14
                                                     0
                                                        0.000
                                                                28
                                                                      0
                                                                         0.000
2
     cs_oa21n10c
                              10c
                                          OAI
                                                14
                                                        0.000
                                   >
                                                     0
                                                                28
                                                                      0
                                                                         0.000
1
     cs_oa22n03c
                              03c
                                          OAI
                                                6
                                    >
                                                        0.000
                                                                        0.000
                                                     0
                                                                6
                                                                     0
22
     cl invvn07c
                             07c
                                         REG
                                                25
                                                        0.000
                                                     0
                                                                550
                                                                      0
                                                                          0.000
30
     cl invvn07d
                             07d
                                         REG
                                                25
                                                        0.000
                                   >
                                                     0
                                                                750
                                                                       0
                                                                          0.000
18
     cl_nnd2n07c
                              07c
                                         REG
                                                26
                                   >
                                                      0
                                                         0.000
                                                                468
                                                                       0
                                                                          0.000
8
    cl_ao22n07c
                             07c
                                   >
                                         REG
                                                33
                                                      0
                                                         0.000
                                                                264
                                                                       0
                                                                         0.000
2
    cl nnd3n07c
                             07c
                                         REG
                                                29
                                                         0.000
                                   >
                                                      0
                                                                 58
                                                                      0
                                                                         0.000
    cl_nor2n06c
1
                             06c
                                         REG
                                                26
                                                     0
                                                        0.000
                                                                26
                                                                      0
                                                                         0.000
1
    cl_ao21n07c
                             07c
                                   >
                                         REG
                                               - 30
                                                      0
                                                        0.000
                                                                 30
                                                                      0
                                                                          0.000
1
    cl_oa21n07c
                             07c
                                   >
                                         REG
                                                30
                                                        0.000
                                                                 30
                                                      0
                                                                      0
                                                                         0.000
1
    cb_mode_block
                               -A
                                    > SEQUENTIAL
                                                     70
                                                           0.000
                                                                      70
                                                                            0.000
6
    cb_clk_32_1
                                  > SEQUENTIAL
                                                   80
                                                           0.000
                                                                   480
                                                                          0
                                                                            0.000
1
    cs_xbn2n01b
                              01b
                                    >
                                         XNOR
                                                  8
                                                      0
                                                          0.000
                                                                  8
                                                                       0
                                                                          0.000
1
     cs_xbo2n01d
                              01d
                                    >
                                         XOR
                                                 8
                                                     -0
                                                         0.000
                                                                 8
                                                                      0
                                                                         0.000
```

```
# of
Levels Output
 0
        1
 1
        55
              50* plus *****
 2
         1
 3
        8
 4
         1
 10
         3
 11
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
5
5
       3
6
       10
7
       3
9
       1
        6
10
12
13
        2
14
        4
       10
15
16
        3
17
       14
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
Fanout Nets
             900* plus ********
      943
             100* plus
 2
       100
 3
       41
 4
       16
 5
       7
 6
       11
        2
 7
 8
        4
        3
 13
 14
        16
 20
        1
```

# [End of measure]

# of

```
[synsasname]: Execution time was 0.0 seconds.
[restore_pin_keywords]: deleted 0 nets and pins
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1146 signals, 923 usage boxes and 1760 connections.
[
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
      > measure
The model <IDCDSUC> has:
 Primary Inputs
                             122
 Primary Outputs
                               73
 Primary BIDIs
                              0
 Signals
                          1146
 Gate Count
                            923
 Connections
                            1760
 Master REG Bits
                               83
 Slave REG Bits
                              83
 Internal Area
                            4525
 External Area
                              0
 Gates/Connects
                            0.524432
 Fanout Count
                             1760
 Average Fanout
                            1.535777
 Avg Tech Box Size =
                            4:902492
 Tech Box Size Stddev =
                              0.010763
 Power
                        0.000000
 **R-E-A-L***S-T-A-T-I-S-T-I-C-S***
 Real signals
                            771
 Real boxes
                            548
 Real connections
                              1385
 Real LSTs
                            2156
 Real ICells/box =
                          8.257299
 Real LSTs/box
                           3.934307
 Real nets/box
                          1.406934
 Cell
               Total
 Each
                Cell
Type Cnt Boxname
                                Power Level Function
                                                       Int Ext Power
                                                                        Int Ext Power
      cs_ao22n03c
                                                          0.000
                                03c
                                            AOI
                                                       0
                                                                  42
                                                                           0.000
  4
      cs_ao12n03c
                                03c
                                            AOI
                                                   4
                                                       0
                                                          0.000
                                                                           0.000
                                                                  16
                                                                        0
                                                  18
  1
      cs_ao22n10c
                                10c
                                            AOI
                                                       0
                                                          0.000
                                      >
                                                                   18
                                                                        0
                                                                           0.000
  1
      cs ao12n04c
                                04c
                                            AOI
                                                  4
                                                          0.000
                                      >
                                                       0
                                                                   4
                                                                       0
                                                                          0.000
       BRKPT
 180
                                        BRKPT
                                                  0
                                                       0
                                                          0.000
                                                                       0
                                                                          0.000
                                                                  0
       IOPAD
 195
                                        IOPAD
                                                 0
                                                      0
                                                         0.000
                                                                  0
                                                                      0
                                                                         0.000
                                   >
       cs_nnd2n02c
 164
                                 02c
                                            NAND
                                                     3
                                                             0.000
                                                                    492
                                                          0
                                                                           0
                                                                              0.000
                                                                            0.000
  1
      cs nnd2n10c
                                10c
                                           NAND
                                                    8
                                                            0.000
                                      >
                                                         0
                                                                    8
                                                                         0
 24
       cs_nnd3n02c
                               02c
                                           NAND
                                                    4
                                                         0
                                                            0.000
                                      >
                                                                    96
                                                                          0
                                                                             0.000
 2
      cs_nnd2n05c
                                05c
                                           NAND
                                                    4
                                                         0
                                      >
                                                            0.000
                                                                    8
                                                                         0
                                                                           0.000
  5
      cs nnd4n03c
                                03c
                                           NAND
                                                    5
                                                            0.000
                                                                    25
                                      >
                                                         0
                                                                         0
                                                                             0.000
  1
      cs_nnd2n13c
                                           NAND
                                                    15
                                13c
                                      >
                                                         0
                                                            0.000
                                                                    15
                                                                          0
                                                                             0.000
  3
      cs_nnd2n04c
                                04c
                                           NAND
                                                    3
                                                            0.000
                                                                    9
                                                                            0.000
```

```
NAND
                                                        0
                                                           0.000
                                                                    6
                                                                         0
                                                                            0.000
                               07c
                                                   6
1
    cs_nnd3n07c
                                     >
                               14e
                                          NAND
                                                   19
                                                         0
                                                            0.000
                                                                    19
                                                                          0
                                                                             0.000
    cs_nnd2n14e
                                     >
1
                                          NAND
                                                   3
                                                        0
                                                           0.000
                                                                    6
                                                                         0
                                                                            0.000
                               03c
                                     >
2
    cs_nnd2n03c
                                                           0.000
                                                                    12
                                                                             0.000
                               07c
                                     >
                                          NAND
                                                   4
                                                        0
                                                                         0
    cs nnd2n07c
3
                                          NAND
                                                   11
                                                         0
                                                            0.000
                                                                    22
                                                                          0
                                                                             0.000
2
                               11c
    cs_nnd2n11c
                                     >
                                                            0.000
                                                   20
                                                         0
                                                                    20
                                                                          0
                                                                             0.000
                               14b
                                          NAND
    cs nnd2n14b
                                     >
1
                                                            0.000
                                                                    22
                                                                          0
                                                                             0.000
                                          NAND
                                                   22
                                                         0
                               12c
                                     >
    cs_nnd3n12c
1
                                                           0.000
                                                                         0
                                                                            0.000
                                          NAND
                                                   8
                                                        0
                                                                    8
                               06c
                                     >
1
    cs_nnd4n06c
                                                                          0
                                                                             0.000
                                                        0
                                                            0.000
                                                                    114
                                          NAND
                                                   19
6
    cs_nnd2n14c
                               14c
                                     >
                                                                    20
                                                                          0
                                                                             0.000
                                                   20
                                                         0
                                                            0.000
                               10c
                                     >
                                          NAND
1
     cs_nnd4n10c
                                                                         0
                                                                            0.000
                                                   4
                                                        0
                                                           0.000
                                                                    4
                               06c
                                          NAND
1
     cs nnd2n06c
                                     >
                                                        0
                                                           0.000
                                                                    6
                                                                         0
                                                                            0.000
                               05c
                                          NAND
                                                    6
1
     cs_nnd3n05c
                                     >
                                                         0
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
                               12c
                                          NAND
                                                   12
                                     >
1
     cs nnd2n12c
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
                                                   12
                                                         0
                               10c
                                     >
                                          NAND
1
     cs nnd3n10c
                                                                            0.000
                                                           0.000
                                                                         0
                               02c
                                     >
                                           NOR
                                                   3
                                                       0
                                                                   30
10
     cs_nor2n02c
                                                          0.000
                                                                   4
                                                                           0.000
                              03c
                                          NOR
                                                  4
                                                       0
                                                                        0
1
     cs nor3n03c
                                    >
                                                                   12
                                                                         0
                                                                            0.000
                                                  12
                                                       0
                                                           0.000
                               12c
                                    >
                                          NOR
     cs_nor2n12c
1
                                          NOR
                                                  3
                                                       0
                                                          0.000
                                                                   3
                                                                        0
                                                                           0.000
                              04c
                                    >
1
     cs_nor2n04c
                                                           0.000
                                                  12
                                                       0
                                                                   12
                                                                         0
                                                                            0.000
                                          NOR
     cs nor3n10c
                               10c
                                     >
1
                                                  7
                                                          0.000
                                                                   7
                                                                        0
                                                                           0.000
                                                       0
     cs_nor2n09c
                              09c
                                     >
                                          NOR
1
                                                          0.000
                                                                  178
                                                                            0.000
                              01c
                                          NOT
                                                  2
                                                       0
                                                                         0
                                     >
89
     cs_invvn01c
                                                                           0.000
                                          NOT
                                                  6
                                                      0
                                                          0.000
                                                                  24
                                                                        0
                              11c
4
     cs invvn11c
                                    >
                                                                           0.000
                                                  4
                                                      0
                                                          0.000
                                                                  24
                                                                        0
                              10c
                                          NOT
6
     cs_invvn10c
                                    >
                                                                            0.000
                                          NOT
                                                  6
                                                       0
                                                          0.000
                                                                  132
                                                                         0
                               12c
22
                                     >
     cs_invvn12c
                                                          0.000
                                                                  28
                                                                           0.000
                                                  4
                                                      0
                                                                        0
                                          NOT
7
                              09c
     cs_invvn09c
                                    >
                                                                  48
                                                                            0.000
                                                  2
                                                          0.000
                                                                        0
                                          NOT
                                                       0
                               07c
                                     >
24
     cs_invvn07c
                                                          0.000
                                                                            0.000
                                          NOT
                                                 10
                                                       0
                                                                  40
                                                                        0
                              15c
4
     cs invvn15c
                                    >
                                                          0.000
                                                                        0
                                                                           0.000
                                          NOT
                                                  2
                                                       0
                                                                  22
11
     cs invvn06c
                               06c
                                   · >
                                                                  24
                                                                        0
                                                                            0.000
                                                  2
                                                       0
                                                          0.000
                                           NOT
12
     cs invvn05c
                               05c
                                   . >
                                                                  40
                                                                        0
                                                                           0.000
                                          NOT
                                                  8
                                                       0
                                                          0.000
     cs_invvn13c
                              13c
                                    >
5
                                                          0.000
                                                                        0
                                                                            0.000
                                          NOT
                                                  10
                                                       0
                                                                   10
1
     cs_invvn14b
                              14b
                                    >
                                                          0.000 -
                                                                           0.000
                                          NOT
                                                       0
                                                                  16
                                                                        0
4
     cs invvn08c
                              08c
                                    >
                                                  4.
                                                  2
                                                                        0
                                                                           0.000
     cs_invvn02c
                              02c
                                    >
                                          NOT
                                                       0
                                                          0.000
                                                                  12
6
                                                          0.000
                                                                       0
                                                                           0.000
                              14c
                                          NOT
                                                  8
                                                       0
                                                                   8
1
     cs_invvn14c
                                    >
                                                                       0
                                                                           0.000
                              04c
                                          NOT
                                                  2
                                                       0
                                                          0.000
                                                                   6
3
     cs invvn04c
                                    >
                              19c
                                    >
                                          NOT
                                                 25
                                                       0
                                                          0.000
                                                                   25
                                                                        0
                                                                            0.000
1
     cs_invvn19c
                                                          0.000
                                                                            0.000
                                          NOT
                                                 14
                                                       0
                                                                   28
                                                                        0
                              16c
                                    >
2
     cs_invvn16c
                                                                   28
                                                                            0.000
                                           OAI
                                                  14
                                                       0
                                                          0.000
                                                                         0
                               10c
                                     >
2
     cs_oa21n10c
                                           OAI
                                                  6
                                                       0
                                                          0.000
                                                                   6
                                                                       0
                                                                           0.000
                               03c
1
     cs oa22n03c
                                     >
                                          REG
                                                  25
                                                       0
                                                          0.000
                                                                  550
                                                                         0
                                                                            0.000
                              07c
22
     cl invvn07c
                                    >
                                                       0
                                                           0.000
                                                                  750
                                                                             0.000
                                                  25
                                                                         0
                              07d
                                     >
                                          REG
30
     cl_invvn07d
                                                                             0.000
                                           REG
                                                  26
                                                        0
                                                           0.000
                                                                   468
                                                                          0
                               07c
                                     >
     cl nnd2n07c
18
                                                                             0.000
                                                  33
                                                        0
                                                           0.000
                                                                   264
                                                                         0
                                           REG
                               07c
8
     cl ao22n07c
                                     >
                                                                            0.000
                                                                   58
                                                                         0
                                                  29
                                                        0
                                                           0.000
2
     cl_nnd3n07c
                               07c
                                     >
                                           REG
                                                  26
                                                       0
                                                           0.000
                                                                   26
                                                                         0
                                                                            0.000
                              06c
                                    >
                                          REG
1
     cl_nor2n06c
                                                  30
                                                        0
                                                           0.000
                                                                   30
                                                                         0
                                                                            0.000
                               07c
                                           REG
1
     cl ao21n07c
                                                  30
                                                        0
                                                           0.000
                                                                   30
                                                                         0
                                                                            0.000
                               07c
                                           REG
1
     cl_oa21n07c
                                                                0.000
                                                                         70
                                                                               0
                                                                                  0.000
                                     > SEQUENTIAL
                                                       70
                                                             0
     cb_mode_block
1
                                                                     480
                                                                             0
                                                                                0.000
                                                     80
                                                           0
                                                              0.000
     cb_clk_32_1
                                   > SEQUENTIAL
6
                                                                             0.000
                                                            0.000
                                                                     8
                                                                          0
                               01b
                                           XNOR
                                                    8
                                                         0
1
     cs_xbn2n01b
                                     >
                                                                    8
                                                                         0
                                                                            0.000
                                           XOR
                                                   8
                                                        0
                                                           0.000
                               01d
 1
     cs xbo2n01d
```

Levels	Outp	out
0	1	*
1	55	50* plus *****
2	·1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
    2
0
1
   943
       2
   100
       100* plus
3
    41
4
    16
5
6
    11
```

```
8
 13
 14
 20
        1
[End of measure]
[measure]: Execution time was 0.6 seconds.
      > write end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 21:59:11 1999
Part: IDCDSUC
                                    EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                 Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                              Max. Endpoints: 3
Sort Field: Slack
                       Abbreviation Comparison/Description
 Cause of Slack
                                   Slack due to a point downstream on path
                        SIkCont
 Slack Continuation
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
                         RAT
                                        ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
                                    ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                         ClkGSet
 Clock Gating Setup
ARRIVAL TIME + ADJUST )
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 Clock Gating Hold
                        ClkGHld
ARRIVAL TIME + ADJUST )
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 Clock Tree Pulse Width
                          CIKTPW
TRAILING EDGE)
                             ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 Setup
                    Setup
ADJUST)
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                   Hold
 Hold
ADJUST)
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                       EndOfC
 EndOfCycle
ADJUST)
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        CIkPW
 ClockPulseWidth
TRAILING EDGE)
                                  ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
                        ClkSep
 ClockSeparation
ARRIVAL TIME + ADJUST )
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                    ALTest
 Loop
CLOCK + ADJUST )
                                  Slack discontinuity due to failed test
                        ATLimit
 Arrival Time Limiting
                                                                     Delay/ Failed Test/
                                  LimitedAT/
  Num/
                                             AT Slack Slew CL FO Cell
                                                                             P Func T.Adi
                                  E Phase
  Test PinName
NetName
                                             2977 -1978 3847 1011 1 PO
                                                                                       0
                                   R C3+R
    1 dcd_succ_last_t1
dcd_succ_last_t1
                                                                     0
                                     999
RAT
                                              2977 -1978 3847 1011 1 IOPAD
                                                                                   IOPAD
                                    R C3+R
----> BOX714/OUT
```

0 dcd\_succ\_last\_t1

	> BOX714/IN	R C3+R 2977 -1978 3847 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1&0	
	> C167/y	R C3+R 2977 -1978 3847 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	5 00 D 4445 4070 55 400 4 3 3 400
	> C167/a	F C3+R 1115 -1978 55 139 4 cs_invvn 01c NOT
	1862 N675	E.CO. D. 1115 1070 FF 100 4 as mades 145 NAND
	>{a} C2738/y 0 N675	F C3+R 1115 -1978 55 139 4 cs_nnd2n 14b NAND
	> C2738/b	R C3+R 1084 -1978 90 159 3 cs_nnd2n 14b NAND
	31 N1692	11 00 FT 1004 -1370 30 133 3 CS_HIId2H 14D 14AI4D
	>{b} C2725rwr/y	R C3+R 1084 -1978 90 159 3 cs_nnd2n 14c NAND
•	0 N1692	
	> C2725rwr/a	F C3+R 1035 -1978 93 168 2 cs_nnd2n 14c NAND
	49 N1479	_
	>{c} C2721rwr/y	F C3+R 1035 -1978 93 168 2 cs_nnd3n 12c NAND
	0 N1479	
	> C2721rwr/c	R C3+R 975 -1978 179 95 2 cs_nnd3n 12c NAND
	59 N1497	D CO.D. 075 4070 '470 05 0 0 40 NOD
	>{d} C2709rwr/y 0 N1497	R C3+R 975 -1978 179 95 2 cs_nor3n 10c NOR
	> C2709rwr/a	F C3+R 899 -1978 50 53 1 cs_nor3n 10c NOR
	76 N1986	1 00111 033 1070 30 30 1 03_1101011 100 NO11
e single i	>{e} C2677rwr_0/y	F C3+R 899 -1978 50 53 1 cs_nnd2n 12c NAND
	0 N1986	and the commence of the commen
* * * = + * *	> C2677rwr_0/b	R C3+R 872 -1978 74 88 2 cs_nnd2n 12c NAND
	27 N1094	
· .	>{f} C2909/y	R C3+R 872 -1978 74 88 2 cs_nnd2n 14c NAND
	0 N1094 > C2909/a	F C3+R 835 -1978 80 108 1 cs_nnd2n 14c NAND
	37 dcd_mcr41_blk&0	TO THE COTTEN TO SO TO TO THE STREET THE STR
	> BOX615/OUT	F C3+R 835 -1978 80 108 1 IOPAD IOPAD
: '	0 dcd_mcr41_blk&0	
	> BOX615/IN	F_C3+R 835 -1978 80 108 1 IOPAD IOPAD 0
_	dcd_mcr41_blk	AWARE A.
		F C3+R 835 -1978 80 108 1 Pl 0
	dcd_mcr41_blk	
		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
	2 dcd_succ_last_t1	F C3+R 2574 -1575 2362 1011 1 PO 0
	dcd_succ_last_t1	1 00111 2014 1010 2002 1011 11 0
	RAT	999 0
	> BOX714/OUT	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1	
	0 dcd_succ_last_t1> BOX714/IN	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y	
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT R C3+R 1138 -1575 92 139 4 cs_invvn 01c NOT
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1436 N675	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1436 N675>{a} C2738/y 0 N675> C2738/a	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT R C3+R 1138 -1575 92 139 4 cs_invvn 01c NOT
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1436 N675> {a} C2738/y 0 N675> C2738/a 44 last_cycle	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD  F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT  R C3+R 1138 -1575 92 139 4 cs_invvn 01c NOT  R C3+R 1138 -1575 92 139 4 cs_nnd2n 14b NAND  F C3+R 1094 -1575 65 108 1 cs_nnd2n 14b NAND
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1436 N675>{a} C2738/y 0 N675> C2738/a	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT R C3+R 1138 -1575 92 139 4 cs_invvn 01c NOT R C3+R 1138 -1575 92 139 4 cs_nnd2n 14b NAND

> 0240770	1100/11 100/ 10/0 00 12 / 2 00
37 N1587	R C3+R 1057 -1575 69 124 2 cs_invvn 14b NOT
> C1952/y 0 N1587	N 05+N 1057 -1075 05 124 2 65_NVIII 145 NOT
> C1952/a	F C3+R 1016 -1575 80 139 2 cs_invvn 14b NOT
41 num_dcd_cyl&0(1)	_
> BOX679/OUT	F C3+R 1016 -1575 80 139 2 IOPAD IOPAD
0 num_dcd_cyl&0(1)	
> BOX679/IN	F C3+R 1016 -1575 80 139 2 IOPAD IOPAD 0
num_dcd_cyl(1)	
> num_dcd_cyl(1)	F C3+R 1016 -1575 80 139 2 Pl 0
num_dcd_cyl(1)	
2 local milli +2 rog n lot 0/2	F C3+R 2818 -1499 48 31 1 cl_invvn 07c SRL
3 local_milli_t2.reg_n.lat_0/a 41 N2054	F C3+H 2010 -1499 40 01 1 CI_IIVVII 070 0112
Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	1 00 100 00 <u>200 ( / 0 _ / / 0 )</u>
> C3011/y	F C3+R 2818 -1499 48 31 1 cs_invvn 07c NOT 0
N2054	
> C3011/a	R C3+R 2781 -1499 466 92 3 cs_invvn 07c NOT
37 N73	
>{a} C2794/y	R C3+R 2781 -1499 466 92 3 cs_ao12n 03c AOI
0 N73	
	F C3+R 2540 -1499 115 18 1 cs_ao12n 03c AOI
241 N1866	
>{b} C2555/y	F C3+R 2540 -1499 115 18 1 cs_ao12n 03c AOI
0 N1866	- D OO D
> C2555/b	R C3+R 2431 -1499 3912 1044 3 cs_ao12n 03c AOI
109 iu_reset_op_c_t1&0	R C3+R 2431 -1499 3912 1044 3 cs_nnd2n 02c NAND
>{c} C2393/y 0 iu_reset_op_c_t1&0	N COTH 2401 -1499 0312 1044 0 03_IIId2II 02010110
> C2393/a	F C3+R 474 -1499 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6	
> gbfocell_6/y	F C3+R 474 -1499 78 137 3 cs_invvn 09c NOT 0
gbfonet_6	
> gbfocell_6/a	R C3+R 410 -1499 217 43 1 cs_invvn 09c NOT
64 N2031	
>{d} C2162/y	R C3+R 410 -1499 217 43 1 cs_nnd3n 02c NAND
0 N2031	
> C2162/b	F C3+R 303 -1499 57 49 3 cs_nnd3n 02c NAND
107 exc_cond_q	F 00 D 000 4400 F7 40 0 d incom 07d CDI
> exc_cond.reg_n.lat_0/l2_out_	n F C3+R 303 -1499 57 49 3 cl_invvn 07d SRL
0 exc_cond_q	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
> exc_cond.reg_n.lat_0/c2	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
143 slow_mode.c2_4> slow_mode.clockblock_3/c2	R C3+ 160 N/C 60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4	11 00T 100 100 00 200 17 00_0M_02_1 20D
U 310W_ITIOUE.UZ_4	

R C3+R 1057 -1575 69 124 2 cs\_nnd2n 14e NAND

----> C2487/b

<sup>&</sup>gt; get\_default\_delay\_synlimit

<sup>&</sup>gt; tc\_parm OFFSET(0)

<sup>&</sup>gt; tc\_parm WEIGHTED\_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...

<sup>[</sup>tc\_parm]: [set\_benefit\_per\_unit\_cost]: unit cost is 4.000000 [tc\_parm]: [set\_benefit\_per\_unit\_cost]: benefit\_units is 0.000172

```
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > quick texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WO...
>>1: [quick]:(
texpand(SCORE(ALL), PUSH, SORT_PINS, NO PRIMITIVES, WORST, SIMILAR, VIEW (TRULE BASE AU
TOGEN), NO VIOLATIONS));
-1978.02 Avg: -210.98
[BD-500000]: texpand CMVC version 1.13.1.9 compiled on Apr 13 1999 at 18:26:58
[texpand]: setting SCORE option to ALL.
[texpand]: setting PUSH option.
[texpand]: setting SORT_PINS option.
[texpand]: setting NO_PRIMITIVES option.
[texpand]: setting WORST option.
[texpand]: setting SIMILAR option.
[texpand]: explicit VIEWs used.
[texpand]: setting NO_VIOLATIONS option.
-1978.02 Avg: -210.98
[texpand]: TRULE view TRULE_BASE_AUTOGEN was found.
maximum area for proto box IDCDSUC is 4525
Rel 0.5 Compiled on Apr 13 1999 at 18:30:09.
-1978.02 Avg: -210.98
Selected 401 critical boxes of 923 total.
[quick]: Number of boxes to process is 401.
[quick]: Number of boxes processed is 0.
[pattern_util]: CMVC version 1.19 compiled on Apr 1 1999 at 05:05:05.
[BD-80000]: pattern CMVC version 1.21.1.1 compiled on Apr 8 1999 at 05:25:52
-1978.02 Avg: -206.57
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected [texpand]: Execution time was 0.6 seconds. [BD-502600]: 11 gates checked and 1 expanded.
         > get_default_delay_synlimit
          > tc_parm OFFSET(0)
        > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > quick {texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, W...
>>]: [quick]:( texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WORST_
,VIEW(TRULE_BASE_AUTOGEN) NO_VIOLATIONS) );
-1978.02 Avg: -206.57
[texpand]: setting SCORE option to ALL.
[texpand]: setting PUSH option.
[texpand]: setting SORT_PINS option.
[texpand]: setting NO_PRIMITIVES option.
[texpand]: setting WORST option.
[texpand]: explicit VIEWs used.
[texpand]: setting NO_VIOLATIONS option.
```

```
-1978.02 Avg: -206.57
[texpand]: TRULE view TRULE_BASE_AUTOGEN was found.
maximum area for proto box IDCDSUC is 4525
-1978.02 Avg: -206.57
Selected 400 critical boxes of 922 total.
[quick]: Number of boxes to process is 400.
[quick]: Number of boxes processed is 0.
-1978.02 Avg: -206.57
 Pattern hint flag is inactive
 [cleanup]: 0 boxes disconnected
 [texpand]: Execution time was 0.4 seconds.
 [BD-502600]: 10 gates checked and 0 expanded.
         > get default delay synlimit
          > tc parm OFFSET(0)
        > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
 [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
 [tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
 [tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
 [tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
 [tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > quick {texpand(SCORE(ALL),PUSH,SORT_PINS,NO_PRIMITIVES,W...
 >>]: [quick]:(
texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WORST, SIMILAR, VIEW(TRULE_AND_OR
              ,NO_VIOLATIONS) );
 AUTOGEN)
-1978.02 Avg: -206.57
 [texpand]: setting SCORE option to ALL.
 [texpand]: setting PUSH option.
 [texpand]: setting SORT_PINS option.
 [texpand]: setting NO_PRIMITIVES option.
 [texpand]: setting WORST option.
 [texpand]: setting SIMILAR option.
 [texpand]: explicit VIEWs used.
 [texpand]: setting NO_VIOLATIONS option.
 -1978.02 Avg: -206.57
 [texpand]: TRULE view TRULE_AND_OR_AUTOGEN was found.
 maximum area for proto box IDCDSUC is 4525
 -1978.02 Avg: -206.57
 Selected 400 critical boxes of 922 total.
 [quick]: Number of boxes to process is 400.
 [quick]: Number of boxes processed is 0.
 -1978.02 Avg: -206.57
 Pattern hint flag is inactive
 [cleanup]: 0 boxes disconnected
 [texpand]: Execution time was 0.0 seconds.
 [BD-502600]: 0 gates checked and 0 expanded.
         > get_default_delay_synlimit
           > tc parm OFFSET(0)
         > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
 [tc parm]: [set benefit per unit_cost]: unit cost is 4.000000
 [tc parm]: [set benefit_per_unit_cost]: benefit_units is 0.000172
 [tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
 [tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
```

```
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
       > quick {texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, W...
>>]: [quick]:( texpand(SCORE(ALL), PUSH, SORT_PINS, NO_PRIMITIVES, WORST
,VIEW(TRULE_AND_OR_AUTOGEN) ,NO_VIOLATIONS));
-1978.02 Avg: -206.57
[texpand]: setting SCORE option to ALL.
[texpand]: setting PUSH option.
[texpand]: setting SORT_PINS option.
[texpand]: setting NO_PRIMITIVES option.
[texpand]: setting WORST option.
[texpand]: explicit VIEWs used.
[texpand]: setting NO_VIOLATIONS option.
-1978.02 Avg: -206.57
[texpand]: TRULE view TRULE_AND_OR_AUTOGEN was found.
maximum area for proto box IDCDSUC is 4525
-1978.02 Avg: -206.57
Selected 400 critical boxes of 922 total.
[quick]: Number of boxes to process is 400.
[quick]: Number of boxes processed is 0.
-1978.02 Avg: -206.57
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[texpand]: Execution time was 0.0 seconds.
[BD-502600]: 0 gates checked and 0 expanded.
                                          > get_default_delay_synlimit
  > tc_parm OFFSET(0)
       > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc parm]: [set benefit per unit cost]: benefit units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
       > quick tmerge(SCORE(ALL),ORD2,SORT_PINS,NO_VIOLATIONS)
>>]: [quick]:( tmerge(SCORE(ALL),ORD2,SORT_PINS,NO_VIOLATIONS) );
-1978.02 Avg: -206.57
[tmerge]: Compiled on Mar 31 1999 at 11:35:37.
[tmerge]: setting SCORE option to ALL.
[tmerge]: setting ORD2 option.
[tmerge]: setting SORT_PINS option.
[tmerge]: setting NO_VIOLATIONS option.
-1978.02 Avg: -206.57
maximum area for proto box IDCDSUC is 4525
-1978.02 Avg: -206.57
Selected 400 critical boxes of 922 total.
[quick]: Number of boxes to process is 400.
[quick]: Number of boxes processed is 0.
-1978.02 Avg: -206.57
[tmerge]: applied 0 times
      > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
```

Sun Apr 18 21:59:14 1999

Part: IDCDSUC

Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack

Num/

**Test PinName** 

Abbreviation Comparison/Description

Slack due to a point downstream on path Slack Continuation SlkCont ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) **RAT** Required Arrival Time ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL Asserted Required Arrival Time AssrtRAT TIME) ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK Clock Gating Setup ClkGSet ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK CIKGHId Clock Gating Hold ARRIVAL TIME + ADJUST ) ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK Clock Tree Pulse Width **CIKTPW** TRAILING EDGE) ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + Setup Setup ADJUST) ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + Hold Hold ADJUST) ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + **EndOfC** EndOfCycle ADJUST) ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK **CIkPW** ClockPulseWidth TRAILING EDGE) ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ClkSep ClockSeparation ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM Loop **ALTest** CLOCK + ADJUST ) Slack discontinuity due to failed test Arrival Time Limiting \_ATLimit

NetName	
	R C3+R 2977 -1978 3847 1011 1 PO 0
1 dcd_succ_last_t1	R C3+R 2977 -1978 3847 1011 1 PO 0
dcd_succ_last_t1	
RAT	999 0
> BOX714/OUT	R C3+R 2977 -1978 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1	
> BOX714/IN `	R C3+R 2977 -1978 3847 1011 1 IOPAD IOPAD '
0 dcd_succ_last_t1&0	
> C167/y	R C3+R 2977 -1978 3847 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0	
> C167/a	F C3+R 1115 -1978 55 139 4 cs_invvn 01c NOT
1862 N675	
>{a} C2738/y	F C3+R 1115 -1978 55 139 4 cs_nnd2n 14b NAND
0 N675	
> C2738/b	R C3+R 1084 -1978 90 159 3 cs_nnd2n 14b NAND
31 N1692	
>{b} C2725rwr/y	R C3+R 1084 -1978 90 159 3 cs_nnd2n 14c NAND
0 N1692	
0 111002	

AT Slack Slew CL FO Cell

LimitedAT/

E Phase

Delay/ Failed Test/

P Func T.Adj

> C2725rwr/a 49 N1479	F C3+R	1035 -1978	93	168 2 cs_nnd2n	14c NAND
>{c} C2721rwr/y 0 N1479	FC3+R	1035 -1978	93	168 2 cs_nnd3r	12c NAND
> C2721rwr/c 59 N1497	R C3+R	975 -1978	179	95 2 cs_nnd3n	12c NAND
>{d} C2709rwr/y 0 N1497	R C3+R	975 -1978	179	95 2 cs_nor3n	10c NOR
> C2709rwr/a 76 N1986	F C3+R	899 -1978	50	53 1 cs_nor3n	10c NOR
>{e} C2677rwr_0/y 0 N1986	F C3+R	899 -1978	50	53 1 cs_nnd2r	12c NAND
> C2677rwr_0/b 27 N1094	R C3+R	872 -1978	74	88 2 cs_nnd2n	12c NAND
>{f} C2909/y 0 N1094	R C3+R	872 -1978	74	88 2 cs_nnd2n	14c NAND
> C2909/a 37 dcd_mcr41_blk&0	F C3+R	835 -1978	80 1	08 1 cs_nnd2n	14c NAND
> BOX615/OUT 0 dcd_mcr41_blk&0	F C3+R	835 -1978	80	108 1 IOPAD	IOPAD
	F C3+R	835 -1978	80	108 1 IOPAD	IOPAD 0
> dcd_mcr41_blk dcd_mcr41_blk	F C3+R	•	: : :	108 1 PI	0

2 dcd\_succ\_last\_t1 F C3+R 2574 1575 2362 1011 1 PO dcd\_succ\_last\_t1 RAT 999 ----> BOX714/OUT FC3+R 2574 -1575 2362 1011 1 IOPAD IOPAD 0 dcd\_succ\_last\_t1 ----> BOX714/IN FC3+R 2574 -1575 2362 1011 1 IOPAD IOPAD 0 dcd\_succ\_last\_t1&0 ----> C167/y FC3+R 2574 -1575 2362 1011 1 cs\_invvn 01c NOT 0 dcd\_succ\_last\_t1&0 ----> C167/a RC3+R 1138 -1575 92 139 4 cs\_invvn 01c NOT 1436 N675 ---->{a} C2738/y R C3+R 1138 -1575 139 4 cs\_nnd2n 14b NAND 0 N675 ----> C2738/a FC3+R 1094 -1575 65 108 1 cs\_nnd2n 14b NAND 44 last\_cycle ---->{b} C2487/y FC3+R 1094 -1575 108 1 cs nnd2n 14e NAND 0 last cycle ----> C2487/b R C3+R 1057 -1575 124 2 cs\_nnd2n 14e NAND 37 N1587 ----> C1952/v RC3+R 1057 -1575 69 124 2 cs\_invvn 14b NOT 0 N1587 ----> C1952/a FC3+R 1016 -1575 80 139 2 cs\_invvn 14b NOT 41 num\_dcd\_cyl&0(1) ----> BOX679/OUT FC3+R 1016 -1575 80 139 2 IOPAD **IOPAD** 0 num\_dcd\_cyl&0(1) ----> BOX679/IN FC3+R 1016 -1575 139 2 IOPAD **IOPAD** 0 num\_dcd\_cyl(1) ----> num\_dcd\_cyl(1) FC3+R 1016 -1575 80 139 2 PI 0 num\_dcd\_cyl(1)

 3 iu_reset_op_c_t1	R C3+R	2431 -1432 3912 1011 1 PO 0
iu_reset_op_c_t1		_
RAT	999	
> BOX716/OUT	R C3+F	R 2431 -1432 3912 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1		
> BOX716/IN	R C3+R	2431 -1432 3912 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	<b>5</b> 00 5	0.404 4.400 0040 4044 0 mmd0m 00m NAND
>{a} C2393/y	R C3+R	2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	- 00 D	474 4400 70 407 0 as said 00 000 NAND
> C2393/a	F C3+R	474 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6	5 00 D	474 -1432 78 137 3 cs invvn 09c NOT 0
> gbfocell_6/y	F C3+R	474 -1432 78 137 3 cs_invvn 09c NOT 0
gbfonet_6	D 00 - D	440 4400 047 40 4 on income 000 NOT
> gbfocell_6/a	R C3+R	410 -1432 217 43 1 cs_invvn 09c NOT
64 N2031	D CO. D	410 -1432 217 43 1 cs_nnd3n 02c NAND
>{b} C2162/y	R C3+R	410 -1432 217 43 1 CS_IIIQSII 02C IVAND
0 N2031	F C3+R	303 -1432 57 49 3 cs_nnd3n 02c NAND
> C2162/b	r Co+n	303 -1432 37 49 3 CS_IIIId311 02C 14A14D
107 exc_cond_q> exc_cond.reg_n.lat_0/l2_out_	n . E (	C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
		00411 000 -1402 37 43 0 01_IIIVVII 074 011E
0 exc_cond_q > exc_cond.reg_n.lat_0/c2	B C3	3+ 160 N/C 60 239 14 cl_invvn 07d SRL
143 slow_mode.c2_4	11 00	77 700 140 00 200 110 <u>-</u>
> slow_mode.clockblock_3/c2	R	C3+ 160 N/C 60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4		·
O GION_INGGOIOL_ I		The second secon

## > measure

The model <IDCDSUC> has: 122 **Primary Inputs Primary Outputs** 73 0 **Primary BIDIs** Signals 1145 **Gate Count** 922 1759 Connections 83 Master REG Bits Slave REG Bits 83 4525 Internal Area 0 External Area Gates/Connects 0.524161 **Fanout Count** 1759 Average Fanout 1.536245 Avg Tech Box Size 4.907809 0.010780 Tech Box Size Stddev = Power 0.000000

\*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\*

 Real signals
 =
 770

 Real boxes
 =
 547

 Real connections
 =
 1384

 Real LSTs
 =
 2154

 Real ICells/box
 =
 8.272395

Real LSTs/box 3.937843 Real nets/box 1.407678 Cell Total Each Cell Type Cnt Boxname Power Level Function Int Ext Power Int Ext Power 7 cs ao22n03c 03c AOI 6 0 0.000 42 0 0.000 3 cs ao12n03c 03c AOI 4 0 0.000 12 0 0.000 > 1 cs ao22n10c 10c AOI 0.000 > 18 0 18 0 0.000 1 cs ao12n04c 04c AOI 4 0 0.000 4 0 0.000 180 BRKPT > **BRKPT** 0 0 0.000 0 0 0.000 195 **IOPAD** > **IOPAD** 0 0 0.000 0 0 0.000 164 cs nnd2n02c 02c > **NAND** 3 0 0.000 492 0 0.000 1 cs\_nnd2n10c 10c **NAND** 8 0 0.000 8 0 0.000 > 24 02c **NAND** cs\_nnd3n02c 4 0 0.000 96 0 0.000 > 2 cs\_nnd2n05c 05c NAND 4 0 0.000 8 0 0.000 > 5 cs nnd4n03c 03c **NAND** 5 25 0 0.000 0 0.000 1 cs nnd2n13c 13c NAND 15 0 0.000 15 0.000 0 3 cs nnd2n04c 04c NAND 3 0.000 0 9 0 0.000 1 cs\_nnd3n07c 07c NAND 6 0 0.000 6 0.000 > 0 1 cs nnd2n14e 14e NAND 19 0 0.000 19 0 0.000 > 2 cs\_nnd2n03c 03cNAND 3 0 0.000 6 0 0.000 > 3 cs\_nnd2n07c 07c NAND 4 0 0.000 12 0. 0.000 > 2 cs nnd2n11c 11c NAND 11 0 0.000 22 0 0.000 > 1 cs nnd2n14b 14b **NAND** 20 0 0.000 20 > 0 0.000 1 cs\_nnd3n12c 12c NAND 22 22 > 0 0.000 0 0.000 cs\_nnd4n06c 1 06c - NAND 8 0 0.000 8 0 0.000 6 cs\_nnd2n14c :14c > NAND 19 0 0.000 114 0 0.000 1 20 cs\_nnd4n10c -10c . NAND: 0 0.000 20 0 0.000 1 cs nnd2n06c 06c NAND 4 0 0.000 4 0.000 1 cs nnd3n05c 05c NAND 6 0 0.000 6 0 0.000 > 1 cs nnd2n12c 12c NAND 12 0 0.000 0.000 > 12 0 1 cs\_nnd3n10c 10c ---> NAND 12 0 0.000 12 0.000 2 cs nnd2f03c 03c NAND 4 0.000 > 0 8 0 0.000 10 cs\_nor2n02c 02c NOR 3 0 0.000 30 > 0 0.000 0 1 cs\_nor3n03c 03c > NOR 4 0.000 4 0 0.000 1 cs nor2n12c 12c > NOR 12 0 0.000 12 0 0.000 1 cs\_nor2n04c 04c > NOR 3 0 0.000 3 0 0.000 1 12 12 cs\_nor3n10c 10c > NOR 0 0.000 0.000 1 cs\_nor2n09c 09c > NOR 7 0 0.000 7 0 0.000 89 cs\_invvn01c 01c NOT 2 0 0.000 178 0.000 > 0 4 cs\_invvn11c 11c NOT 6 0 0.000 24 0 0.000 > 6 cs\_invvn10c 10c NOT 4 0 0.000 24 0 0.000 > 22 NOT 0.000 cs\_invvn12c 12c 6 0 132 0.000 > 0 7 cs\_invvn09c 09c NOT 4 0.000 28 0 0 0.000 > 21 2 cs\_invvn07c 07c NOT 0 0.000 42 0 0.000 > 4 cs invvn15c 15c NOT 10 0 0.000 40 0 0.000 > 11 cs\_invvn06c 06c NOT 2 22 > 0 0.000 0 0.000 2 12 cs\_invvn05c 05c > NOT 0 0.000 24 0 0.000 5 cs\_invvn13c 13c > NOT 8 0 0.000 40 0 0.000 1 cs\_invvn14b NOT 14b > 10 0 0.000 10 0 0.000 4 cs\_invvn08c 08c > NOT 4 0 0.000 16 0 0.000 6 cs invvn02c 02c > NOT 2 0 0.000 12 0 0.000 1 cs\_invvn14c 14c NOT 8 0 0.000 8 > 0 0.000 3 cs\_invvn04c 04c NOT 2 0.000 0.000 6 0

```
0.000
                                                             25
                                                                     0.000
                                       NOT
                                             25
                                                   0
                                                                  0
                           19c
                                 >
1
    cs_invvn19c
                                       NOT
                                             14
                                                  0
                                                      0.000
                                                             28
                                                                  0
                                                                     0.000
                           16c
2
    cs_invvn16c
                                 >
                                                                 0.000
                                                     0.000
                                                             2
                                              2
                                       NOT
                                                  0
    cs_invvn03c
                           03c
1
                                                             28
                                                                      0.000
                                                      0.000
                                                                   0
                            10c
                                       OAI
                                             14
                                                   0
2
    cs_oa21n10c
                                                     0.000
                                                             6
                                                                  0.000
                                       OAI
                                              6
                                                  0
                            03c
    cs_oa22n03c
1
                                                                      0.000
                                             25
                                                   0
                                                      0.000
                                                             550
                                                                   0
                           07c
                                       REG
     cl_invvn07c
                                 >
22
                                                                      0.000
                                              25
                                                   0
                                                      0.000
                                                             750
                                                                   0
                                       REG
                            07d
30
     cl invvn07d
                                 >
                                                             468
                                                                      0.000
                                              26
                                                      0.000
                                                                    0
                                                   0
                            07c
                                       REG
     cl_nnd2n07c
18
                                                                   0.000
                                                             264
                                                   0
                                                      0.000
                            07c
                                  >
                                       REG
                                              33
    cl_ao22n07c
8
                                                                      0.000
                                              29
                                                   0
                                                      0.000
                                                              58
                                                                   0
                            07c
                                       REG
2
    cl_nnd3n07c
                                  >
                                                                      0.000
                                                      0.000
                                                             26
                                                                   0
                                       REG
                                             26
                                                   0
    cl_nor2n06c
                            06c
                                 >
1
                                                                   0
                                                                      0.000
                                       REG
                                              30
                                                   0
                                                      0.000
                                                              30
                            07c
1
    cl ao21n07c
                                              30
                                                   0
                                                      0.000
                                                              30
                                                                   0
                                                                      0.000
                                       REG
    cl_oa21n07c
                            07c
1
                                                                        0.000
                                                        0.000
                                                                   70
                                  > SEQUENTIAL
                                                   70
    cb_mode_block
1
                                                               480
                                                                      0.000
                                > SEQUENTIAL
                                                80
                                                      0
                                                         0.000
    cb_clk_32_1
6
                                                               8
                                                                    0
                                                                      0.000
                                                8
                                                    0
                                                       0.000
                                       XNOR
                             01b
1
    cs_xbn2n01b
                                                      0.000
                                                                   0
                                                                      0.000
                                               8
                                                   0
                                                               8
                                        XOR
                             01d
     cs_xbo2n01d
1
```

```
# of
Levels Output
 0
        1
        55
  1
  2
        1
  3
        8
  4
        1
         3
 10
 1Ï
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
  0
        7
  2
        20
  3
         1
         5
  4
  5
         3
  6
        10
  7
         3
  9
         1
 10
         6
 12
         1
 13
         2
         4
 14
         10
 15
 16
         3
         14
 17
```

The Histogram Of Fanin vs. Box

```
# of
Fanin
         Ops
               350* plus *****
 1
       380
 2
       205
               200* plus *****
 3
        36
 4
        16
```

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
     2
 0
         942
 1
 2
    100
         100* plus
 3
     41
 4
     16
 5
     7
 6
     11
 7
     2
 8
13
     3
14
20
```

### [End of measure]

[fantom]: Execution time was 0.0 seconds.

[BD-500701]: Added 0 inverters.

```
[measure]: Execution time was 0.6 seconds.
       > critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...
critical(
repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS), fantom(LIMITED), faninv(LIMITED));
-1978.02 Avg: -206.57
maximum area for proto box IDCDSUC is 4525
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
[BD-500000]: clone CMVC version 1.20 compiled on Apr 13 1999 at 18:21:21
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
[BD-500000]: fantom CMVC version 1.54 compiled on Apr 13 1999 at 18:23:22
[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
-1978.02 Avg: -206.57
ArrayNum: 9 ArrayMax: 922
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.3 seconds.
[BD-500700]: Added 0 buffers.
```

```
[faninv]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 36 times and applied 0 of them.
      > nextbox synexpand(XPANDVIEW)
>>]: nextbox( synexpand(XPANDVIEW) );
[restore_pin_keywords]: restored 0 keywords
>>1: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[restore_pin_keywords]: deleted 0 nets and pins
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1145 signals, 922 usage boxes and 1759 connections.
>>1: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
       > measure
 The model <IDCDSUC> has:
 Primary Inputs
                              122
 Primary Outputs
                               73
 Primary BIDIs
                               0
 Signals
                           1145
 Gate Count
                             922
 Connections
                             1759
 Master REG Bits
                                83
                               83
 Slave REG Bits
 Internal Area
                            4525
 External Area
                               0
                            0.524161
 Gates/Connects
 Fanout Count
                             1759
 Average Fanout
                            1.536245
                             4.907809
 Avg Tech Box Size =
 Tech Box Size Stddev =
                              0.010780
 Power
                         0.000000
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
 Real signals
                             770
                             547
 Real boxes
 Real connections
                               1384
 Real LSTs
                            2154
 Real ICells/box
                           8.272395
                            3.937843
 Real LSTs/box
                           1.407678
 Real nets/box
 Cell
               Total
 Each
                 Cell
                                                                          Int Ext Power
                                 Power Level Function
                                                        Int Ext Power
Type Cnt Boxname
                                                                    42
                                                        0
                                                            0.000
                                                                         0
                                                                             0.000
  7
                                 03c
                                             AOI
                                                    6
       cs_ao22n03c
                                             AOI
                                                    4
                                                        0
                                                            0.000
                                                                    12
                                                                         0
                                                                             0.000
                                 03c
  3
       cs ao12n03c
                                                   18
                                                         0
                                                            0.000
                                                                    18
                                                                          0
                                                                             0.000
                                 10c
                                             AOI
   1
       cs_ao22n10c
                                      >
```

```
1
     cs_ao12n04c
                               04c
                                           AOI
                                                       0
                                                          0.000
                                                  4
                                                                   4
                                                                       0
                                                                          0.000
180
      BRKPT
                                        BRKPT
                                                  0
                                                      0
                                                          0.000
                                                                  0
                                                                       0
                                                                          0.000
                                   >
195
      IOPAD
                                       IOPAD
                                                 0
                                                      0
                                                         0.000
                                                                 0
                                                                      0
                                  >
                                                                         0.000
164
                                02c
                                                     3
      cs nnd2n02c
                                            NAND
                                                                    492
                                      >
                                                          0
                                                             0.000
                                                                           0
                                                                              0.000
 1
     cs nnd2n10c
                               10c
                                           NAND
                                     >
                                                    8
                                                        0
                                                            0.000
                                                                    8
                                                                         0
                                                                            0.000
24
                                02c
      cs_nnd3n02c
                                      >
                                           NAND
                                                    4
                                                         0
                                                            0.000
                                                                    96
                                                                          0
                                                                             0.000
2
     cs_nnd2n05c
                               05c
                                     >
                                           NAND
                                                    4
                                                        0
                                                            0.000
                                                                    8
                                                                         0
                                                                            0.000
 5
     cs nnd4n03c
                               03c
                                     >
                                           NAND
                                                    5
                                                        0
                                                            0.000
                                                                    25
                                                                         0
                                                                             0.000
 1
     cs_nnd2n13c
                               13c
                                           NAND
                                                    15
                                                         0
                                     >
                                                            0.000
                                                                    15
                                                                          0
                                                                             0.000
 3
     cs_nnd2n04c
                               04c
                                           NAND
                                                            0.000
                                     >
                                                    3
                                                        0
                                                                    9
                                                                         0
                                                                            0.000
     cs_nnd3n07c
                               07c
                                           NAND
 1
                                     >
                                                    6
                                                            0.000
                                                        0
                                                                    6
                                                                         0
                                                                            0.000
     cs_nnd2n14e
 1
                               14e
                                     >
                                           NAND
                                                    19
                                                         0
                                                            0.000
                                                                    19
                                                                        ...0....0.00
 2
     cs nnd2n03c
                               03c
                                     >
                                           NAND
                                                    3
                                                        0
                                                            0.000
                                                                            0.000
                                                                    6
                                                                         0
 3
     cs_nnd2n07c
                               07c
                                           NAND
                                                    4
                                     >
                                                        0
                                                            0.000
                                                                    12
                                                                         0
                                                                             0.000
 2
     cs_nnd2n11c
                               11c
                                     >
                                           NAND
                                                   11
                                                         0
                                                            0.000
                                                                    22
                                                                          0
                                                                             0.000
 1
     cs nnd2n14b
                               14b
                                     >
                                           NAND
                                                    20
                                                         0
                                                            0.000
                                                                    20
                                                                          0
                                                                             0.000
 1
     cs_nnd3n12c
                               12c
                                           NAND
                                                   22
                                                         0
                                                                    22
                                     >
                                                            0.000
                                                                          0
                                                                             0.000
 1
     cs nnd4n06c
                               06c
                                     >
                                           NAND
                                                    8
                                                            0.000
                                                        0
                                                                    8
                                                                         0
                                                                            0.000
 6
     cs_nnd2n14c
                               14c
                                           NAND
                                                   19
                                                         0
                                     >
                                                            0.000
                                                                    114
                                                                           0
                                                                             0.000
 1
     cs_nnd4n10c
                               10c
                                     >
                                           NAND
                                                   20
                                                         0
                                                            0.000
                                                                    20
                                                                          0
                                                                             0.000
     cs_nnd2n06c
                               06c
                                     >
                                           NAND
                                                    4
                                                        0
                                                            0.000
                                                                    4
                                                                         0
                                                                            0.000
 1
     cs_nnd3n05c
                               05c
                                     >
                                           NAND
                                                    6
                                                        0
                                                           0.000
                                                                         0
                                                                            0.000
                                                                    6
 1
     cs nnd2n12c
                               12c
                                           NAND
                                                         0
                                     >
                                                   12
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
 1
     cs nnd3n10c
                               10c
                                          NAND
                                                         0
                                                            0.000
                                     >
                                                   12
                                                                    12
                                                                          0
                                                                             0.000
                               03c
2
     cs_nnd2f03c
                                          NAND
                                                   4
                                                        0
                                                           0.000
                                                                        0
                                                                           0.000
                                    >
                                                                    8
10
     cs_nor2n02c
                               02c
                                           NOR
                                                   3
                                                        0
                                                           0.000
                                                                   30
                                     >
                                                                         0
                                                                            0.000
 1
     cs_nor3n03c
                               03c
                                     >
                                           NOR
                                                   4.
                                                       0.000
                                                                           0.000
                                                                   4
                                                                        0.
1
     cs nor2n12c
                               12c
                                     >
                                           NOR
                                                  12
                                                        0.000
                                                                   12
                                                                         0
                                                                            0.000
 1.
     cs_nor2n04c
                               04c
                                           NOR
                                                  3
                                                       0
                                                           0.000
                                                                   3
                                                                        0
                                                                           0.000
                                     >
1.
     cs_nor3n10c
                               10c
                                           NOR
                                                  12
                                                       0
                                                           0.000
                                                                   12
                                                                         0
                                                                            0.000
                                     >
1
     cs_nor2n09c
                               09c
                                     >
                                           NOR
                                                   7
                                                       0
                                                          0.000
                                                                   7
                                                                        0
                                                                           0.000
89
                                                 - 2
                                                                  178 -
     cs_invvn01c
                               01c
                                           NOT
                                                       0
                                                          0.000
                                     >
                                                                        0.000
4
     cs_invvn11c
                              11c
                                          NOT
                                                  6
                                                      Õ
                                                          0.000
                                                                  24
                                                                           0.000
                                    >
                                                                       0
6
     cs invvn10c
                                          NOT
                                                  4
                                                          0.000
                              10c
                                    >
                                                      0
                                                                  24
                                                                           0.000
                                                                       0
22
     cs_invvn12c
                                          NOT
                                                  6
                                                          0.000
                               12c
                                                       0
                                                                  132
                                                                        0
                                                                            0.000
                                     .>
7
     cs_invvn09c
                                          NOT
                                                      0
                              09c
                                    >
                                                  4
                                                          0.000
                                                                  28
                                                                        0
                                                                           0.000
21
                                                          0.000
      cs_invvn07c
                               07c
                                           NOT
                                                  2
                                     >
                                                       0
                                                                  42
                                                                        0
                                                                           0.000
4
     cs_invvn15c
                              15c
                                          NOT
                                                 10
                                                       0
                                                          0.000
                                                                  40
                                                                        0
                                    >
                                                                           0.000
11
     cs_invvn06c
                               06c
                                           NOT
                                                  2
                                                       0
                                                          0.000
                                     >
                                                                  22
                                                                        0
                                                                           0.000
12
     cs invvn05c
                               05c
                                           NOT
                                                  2
                                                       0
                                                          0.000
                                                                  24
                                     >
                                                                        0
                                                                           0.000
5
     cs invvn13c
                              13c
                                          NOT
                                                  8
                                                      0
                                                          0.000
                                    >
                                                                  40
                                                                       0
                                                                           0.000
1
     cs_invvn14b
                              14b
                                    >
                                          NOT
                                                  10
                                                       0
                                                          0.000
                                                                  10
                                                                        0
                                                                           0.000
4
                                                                           0.000
     cs_invvn08c
                              08c
                                    >
                                          NOT
                                                  4
                                                      0
                                                          0.000
                                                                  16
                                                                       0
6
     cs invvn02c
                              02c
                                          NOT
                                                  2
                                                      0
                                                          0.000
                                    >
                                                                  12
                                                                       0
                                                                           0.000
1
     cs_invvn14c
                              14c
                                    >
                                          NOT
                                                  8
                                                      0
                                                          0.000
                                                                  8
                                                                       0
                                                                          0.000
3
     cs_invvn04c
                              04c
                                    >
                                          NOT
                                                  2
                                                      0
                                                          0.000
                                                                  6
                                                                       0
                                                                          0.000
1
     cs_invvn19c
                              19c
                                    >
                                          NOT
                                                 25
                                                       0
                                                          0.000
                                                                  25
                                                                        0
                                                                           0.000
2
     cs_invvn16c
                              16c
                                          NOT
                                                 14
                                                          0.000
                                                                  28
                                    >
                                                       0
                                                                        0
                                                                           0.000
1
     cs_invvn03c
                              03c
                                          NOT
                                                  2
                                                      0
                                                          0.000
                                    >
                                                                  2
                                                                       0
                                                                          0.000
2
     cs_oa21n10c
                               10c
                                           OAI
                                                 14
                                                       0
                                                          0.000
                                                                  28
                                     >
                                                                        0
                                                                           0.000
1
     cs_oa22n03c
                               03c
                                           OAI
                                                  6
                                     >
                                                      0
                                                          0.000
                                                                  6
                                                                       0
                                                                          0.000
22
     cl invvn07c
                              07c
                                          REG
                                                 25
                                                          0.000
                                                                  550
                                    >
                                                       0
                                                                        0
                                                                            0.000
30
     cl invvn07d
                              07d
                                          REG
                                                 25
                                                          0.000
                                                                  750
                                    >
                                                       0
                                                                         0
                                                                            0.000
     cl_nnd2n07c
                                                  26
18
                               07c
                                     >
                                           REG
                                                        0
                                                           0.000
                                                                  468
                                                                         0
                                                                             0.000
8
     cl ao22n07c
                              07c
                                    >
                                          REG
                                                  33
                                                       0
                                                           0.000
                                                                  264
                                                                            0.000
                                                                         0
```

```
0.000
                         07c
                                    REG
                                          29
                                               0
                                                 0.000
                                                         58
   cl_nnd3n07c
2
                         06c
                                   REG
                                          26
                                               0
                                                  0.000
                                                         26
                                                              0
                                                                 0.000
    cl_nor2n06c
                              >
1
                                          30
                                               0
                                                  0.000
                                                         30
                                                              0
                                                                 0.000
                                    REG
                         07c
1
   cl_ao21n07c
                                                                 0.000
                                                         30
                                          30
                                               0
                                                  0.000
                                                              0
   cl_oa21n07c
                          07c
                                    REG
1
                                                                   0.000
                                                    0.000
                                                              70
                               > SEQUENTIAL
                                               70
    cb_mode_block
1
                                                                 0.000
                             > SEQUENTIAL
                                            80
                                                  0 0.000 480
    cb_clk_32_1
6
                                                0.000
                                                          8
                                                              0.000
                                    XNOR
                                            8
                          01b
    cs xbn2n01b
1
                                                  0.000
                                                          8
                                                              0
                                                                0.000
                                    XOR
                                           8
                                               0
    cs_xbo2n01d
                          01d
1
```

```
# of
Levels Output
        1
  0
              50* plus *****
        55
  1
 2
        1
        8
 3
 4
         1
 10
         3
         1
 11
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 3
        1
        5
.. 4
        3
 5
        10
 6
        3
 7
 9
        1
 10
         6
 12
         1
         2
 13
 14
         4
 15
        10
         3
 16
 17
        14
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
 0
       2
 1
      942
            200* plus
 2
      100
            100* plus
 3
      41
 4
       16
 5
       7
 6
       11
 7
       2
 8
       4
 13
       3
 14
       16
20
        1
[End of measure]
[measure]: Execution time was 0.6 seconds.
      > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end point report..92476.
[ET-0019]: <End....New Endpoint Report.
Sun Apr 18 21:59:18 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                    EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                 Max. Slack: 1,13427E+38
Sort Field: Slack
                              Max. Endpoints: 3
 Cause of Slack
                       Abbreviation Comparison/Description
 Slack Continuation
                        SlkCont
                                   Slack due to a point downstream on path
 Required Arrival Time
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                         RAT
 Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
 Clock Gating Setup
                        ClkGSet
                                   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                        ClkGHld
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                          CIKTPW
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
Setup
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
ADJUST)
Hold
                   Hold
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST )
                      EndOfC
 EndOfCycle
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST)
                        CIkPW
ClockPulseWidth
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
 ClockSeparation
                        ClkSep
                                  ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
Loop
                   ALTest
CLOCK + ADJUST )
 Arrival Time Limiting
                        ATLimit
                                  Slack discontinuity due to failed test
```

Num/ Test PinName NetName	LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
	R C3+R 2977 -1978 3847 1011 1 PO 0 999 0 R C3+R 2977 -1978 3847 1011 1 IOPAD IOPAD
> BOX714/IN 0 dcd_succ_last_t1&0	R C3+R 2977 -1978 3847 1011 1 IOPAD IOPAD
> C167/y 0 dcd_succ_last_t1&0	R C3+R 2977 -1978 3847 1011 1 cs_invvn 01c NOT
> C167/a 1862 N675	F C3+R 1115 -1978 55 139 4 cs_invvn 01c NOT
>{a} C2738/y 0 N675	F C3+R 1115 -1978 55 139 4 cs_nnd2n 14b NAND
> C2738/b 31 N1692	R C3+R 1084 -1978 90 159 3 cs_nnd2n 14b NAND
>{b} C2725rwr/y 0 N1692	R C3+R 1084 -1978 90 159 3 cs_nnd2n 14c NAND
> C2725rwr/a 49 N1479	F C3+R 1035 -1978 93 168 2 cs_nnd2n 14c NAND
>{c} C2721rwr/y_ 0 N1479	F C3+R 1035 -1978 93 168 2 cs_nnd3n 12c NAND
> C2721rwr/c 59 N1497	R C3+R -975 -1978 179 95 2 cs_nnd3n 12c NAND
>{d} C2709rwr/y 0 N1497	R C3+R 975 -1978 179 95 2 cs_nor3n 10c NOR
> C2709rwr/a 76 N1986	F C3+R 899 -1978 50 53 1 cs_nor3n 10c NOR
>{e} C2677rwr_0/y 0 N1986	F C3+R 899 -1978 50 53 1 cs_nnd2n 12c NAND
> C2677rwr_0/b 27 N1094	R C3+R 872 -1978 74 88 2 cs_nnd2n 12c NAND
>{f} C2909/y 0 N1094	R C3+R 872 -1978 74 88 2 cs_nnd2n 14c NAND  F C3+R 835 -1978 80 108 1 cs_nnd2n 14c NAND
> C2909/a 37 dcd_mcr41_blk&0 > BOX615/OUT	F C3+R 835 -1978 80 108 1 IOPAD IOPAD
0 dcd_mcr41_blk&0 > BOX615/IN	F C3+R 835 -1978 80 108 1 IOPAD IOPAD 0
> BOX613/114 dcd_mcr41_blk > dcd_mcr41_blk dcd_mcr41_blk	F C3+R 835 -1978 80 108 1 PI 0
	F C3+R 2574 -1575 2362 1011 1 PO 0
RAT > BOX714/OUT	999 0 F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1> BOX714/lN 0 dcd_succ_last_t1&0	F C3+R 2574 -1575 2362 1011 1 IOPAD IOPAD

> C167/y	F C3+R 2574 -1575 2362 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0	D.00 D. 1100 1000
> C167/a 1436 N675	R C3+R 1138 -1575 92 139 4 cs_invvn 01c NOT
>{a} C2738/y	R C3+R 1138 -1575 92 139 4 cs_nnd2n 14b NAND
0 N675	11 00+11 1130 -1375 92 139 4 CS_IIIUZII 140 IVAIND
> C2738/a	F C3+R 1094 -1575 65 108 1 cs_nnd2n 14b NAND
44 last_cycle	
>{b} C2487/y	F C3+R 1094 -1575 65 108 1 cs_nnd2n 14e NAND
0 last_cycle	B.00 B. 10-5 17-5 10-10-10-10-10-10-10-10-10-10-10-10-10-1
> C2487/b 37 N1587	R C3+R 1057 -1575 69 124 2 cs_nnd2n 14e NAND
> C1952/y	R C3+R 1057 -1575 69 124 2 cs_invvn 14b NOT
0 N1587	11 00111 1007 1070 00 124 2 05_HIVWH 14D NO!
> C1952/a	F C3+R 1016 -1575 80 139 2 cs_invvn 14b NOT
41 num_dcd_cyl&0(1)	_
> BOX679/OUT	F C3+R 1016 -1575 80 139 2 IOPAD IOPAD
0 num_dcd_cyl&0(1)	F.00 D 4040 4F7F 00 400 0 10D4D 10D4D
> BOX679/IN num_dcd_cyl(1)	F C3+R 1016 -1575 80 139 2 IOPAD IOPAD 0
> num_dcd_cyl(1)	F C3+R 1016 -1575 80 139 2 PI 0
num_dcd_cyl(1)	7 00111 1010 1070 00 100 211
*	R C3+R 2431 -1432 3912 1011 1 PO 0
iu_reset_op_c_t1	R C3+R 2431 -1432 3912 1011 1 PO 0
RAT	999
> BOX716/OUT	999 R C3+R 2431 -1432 3912 1011 1 IOPAD JOPAD
0 iu_reset_op_c_t1	
> BOX716/IN	R C3+R 2431 -1432 3912 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
>{a} C2393/y 0 iu_reset_op_c_t1&0	H_C3+H
> C2393/a	F C3+R 474 -1432 78 137 3 cs nnd2n 02c NAND
1958 gbfonet_6	
> gbfocell_6/y	F C3+R 474 -1432 78 137 3 cs_nnd2n 02c NAND F C3+R 474 -1432 78 137 3 cs_invvn 09c NOT 0
gbfonet_6	D.00 D. 440 4400 047 40 4
> gbfocell_6/a 64 N2031	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
>{b} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
0 N2031	110 1102 217 10 105_1111doi1 02017/1110
> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
107 exc_cond_q	
> exc_cond.reg_n.lat_0/l2_out_	n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
0 exc_cond_q > exc_cond.reg_n.lat_0/c2	R C3+ 160 N/C 60 239 14 cl_invvn 07d SRL
143 slow_mode.c2_4	11 001 100 100 00 200 14 G_HIVVII U/U SAL
> slow_mode.clockblock_3/c2	R C3+ 160 N/C 60 239 14 cb_clk_32_1 LCB
0 slow_mode.c2_4	

[

```
>>]: Itorbox( dfanmatch(ACTUAL,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1978.02 Avg: -206.57
[BD-500300]: 70 pins on 32 gates swapped.
-1977.33 Avg: -205.40
[fanmatch]: Execution time was 3.6 seconds.
       > get_default_delay_synlimit
        > tc parm OFFSET(0)
       > tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1) ...
[tc parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
       > reset critical slack limit
-1977.33 Avg: -205.40
resetting the current slack to -1977.3279
       > repower paths FUZZY(0.02)
initial slack is -1977
after repower paths slack is -1977
        > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS) , repowe...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL), INC, NO_VIOLATIONS, REPOWER_GROUP(BETA)));
-1977.33 Avg: -200.64
maximum area for proto box IDCDSUC is 4595
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1977.33 Avg: -200.64
ArrayNum: 9 ArrayMax: 922
-1967.14 Avg: -200.49
ArrayNum: 6 ArrayMax: 922
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 0.4 seconds.
[BD-500026]: repower was applied 1 times.
Irepowerl: Execution time was 0.4 seconds.
[BD-502000]: Called transforms 24 times and applied 1 of them.
        > compare critical slack_limit
-1967.14 Avg: -200.49
comparing new slack -1967.1356 to saved slack -1957.5546
       > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 21:59:41 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                      EDA EinsTimer EndPoint Report
```

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999

Min. Slack: -1.13427E+38

Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description Slack Continuation SlkCont Slack due to a point downstream on path Required Arrival Time RAT ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL TIME) Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ARRIVAL TIME + ADJUST ) Clock Gating Hold ClkGHld ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK ARRIVAL TIME + ADJUST ) Clock Tree Pulse Width CIKTPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE ) Setup Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + ADJUST) Hold Hold ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + ADJUST) EndOfCycle EndOfC ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + ADJUST) ClockPulseWidth ClkPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK TRAILING EDGE) ClockSeparation ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ClkSep ARRIVAL TIME + ADJUST ) ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM Loop CLOCK + ADJUST ) Arrival Time Limiting ATLimit Slack discontinuity due to failed test Num/ LimitedAT/ Delay/ Failed Test/ Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj NetName 1 dcd\_succ\_last\_t1 R C3+R 2966 -1967 3847 1011 1 PO dcd\_succ\_last\_t1 RAT 999 0 ---> BOX714/OUT R C3+R 2966 -1967 3847 1011 1 IOPAD **JOPAD** 0 dcd\_succ last t1 ----> BOX714/IN R C3+R 2966 -1967 3847 1011 1 IOPAD IOPAD : 0 dcd\_succ\_last\_t1&0 ----> C167/y R C3+R 2966 -1967 3847 1011 1 cs\_invvn 01c NOT 0 dcd\_succ\_last t1&0 ----> C167/a FC3+R 1104 -1967 55 139 4 cs\_invvn 01c NOT 1862 N675 ---->{a} C2738/y FC3+R 1104 -1967 55 139 4 cs\_nnd2n 14b NAND 0 N675 ----> C2738/a R C3+R 1075 -1967 71 108 1 cs\_nnd2n 14b NAND 29 last\_cycle ---->{b} C2487/v R C3+R 1075 -1967 71 108 1 cs\_nnd2n 14e NAND 0 last\_cycle ----> C2487/b FC3+R 1044 -1967 41 124 2 cs\_nnd2n 14e NAND 31 N1587 ----> C1952/y FC3+R 1044 -1967 41 124 2 cs\_invvn 14b NOT 0 N1587 ----> C1952/a R C3+R 1024 -1967 80 139 2 cs\_invvn 14b NOT

20 num_dcd_cyl&0(1)> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+R 1024 -1967 80 139 2 IOPAD IOPAD  R C3+R 1024 -1967 80 139 2 IOPAD IOPAD 0  R C3+R 1024 -1967 80 139 2 PI 0
2 dcd_succ_last_t1 dcd_succ_last_t1 RAT	F C3+R 2616 -1617 2362 1011 1 PO 0
> BOX714/OUT 0 dcd_succ_last_t1 > BOX714/IN	F C3+R 2616 -1617 2362 1011 1 IOPAD IOPAD F C3+R 2616 -1617 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&0> C167/y	F C3+R 2616 -1617 2362 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0 > C167/a 1436 N675	R C3+R 1180 -1617 92 139 4 cs_invvn 01c NOT
>{a} C2738/y 0 N675	R C3+R 1180 -1617 92 139 4 cs_nnd2n 14b NAND
> C2738/b 52 N1692	F C3+R 1128 -1617 63 159 3 cs_nnd2n 14b NAND
>{b} C2725rwr/y 0 N1692	F C3+R 1128 -1617 63 159 3 cs_nnd2n 14c NAND
> C2725rwr/a 42 N1479	R C3+R 1086 -1617 134 167 2 cs_nnd2n 14c NAND
>{c} C2721rwr/y 0 N1479	R C3+R 1086 -1617 134 167 2 cs_nnd3n 12c NAND
> C2721rwr/c	F C3+R 994 -1617 125 95 2 cs_nnd3n 12c NAND
>{d} C2709rwr/y 0 N1497	F C3+R 994 -1617 125 95 2 cs_nor3n 10e NOR
> C2709rwr/c 96 N1781	R C3+R 898 -1617 137 68 2 cs_nor3n 10e NOR
>{e} C2885/y 0 N1781	R C3+R 898 -1617 137 68 2 cs_nnd4n 10c NAND
> C2885/d 73 N1997	F C3+R 825 -1617 44 50 1 cs_nnd4n 10c NAND
>{f} C2886/y 0 N1997	F C3+R 825 -1617 44 50 1 cs_nnd2n 14c NAND
> C2886/a 23 op_serialize&0	R C3+R 802 -1617 80 124 2 cs_nnd2n 14c NAND
> BOX638/OUT 0 op_serialize&0	R C3+R 802 -1617 80 124 2 IOPAD IOPAD
> BOX638/IN op_serialize	R C3+R 802 -1617 80 124 2 IOPAD IOPAD 0
> op_serialize op_serialize	R C3+R 802 -1617 80 124 2 Pl 0
3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT	R C3+R 2431 -1432 3912 1011 1 PO 0 999 0

```
----> BOX716/OUT
                                   R C3+R
                                            2431 -1432 3912 1011 1 IOPAD
                                                                                IOPAD
0 iu_reset_op_c_t1
---> BOX716/IN
                                 R C3+R
                                           2431 -1432 3912 1044 3 IOPAD
                                                                              IOPAD
0 iu_reset op c t1&0
---->{a} C2393/v
                                R C3+R
                                         2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a
                               F C3+R
                                          473 -1432
                                                      78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6
----> gbfocell_6/y
                                FC3+R
                                          473 -1432
                                                      78 137 3 cs_invvn 09c NOT
                                                                                      0
gbfonet_6
----> gbfocell_6/a
                                R C3+R
                                          410 -1432
                                                      217
                                                           43 1 cs invvn 09c NOT
64 N2031
---->{b} C2162/v
                                          410 -1432
                                R C3+R
                                                      217
                                                            43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b
                               FC3+R
                                          303 -1432
                                                      57 49 3 cs_nnd3n 02c NAND
107 rcvrv reset a
----> rcvry_reset.reg_n.lat_0/l2_out_n
                                      FC3+R
                                                303 -1432
                                                             57 49 3 cl_invvn 07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2
                                    R C3+
                                              160 N/C
                                                         60 222 13 cl_invvn 07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2
                                     R C3+
                                               160
                                                   N/C
                                                           60 222 13 cb clk 32 1 LCB
0 slow mode.c2 1
  > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000 [tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
> has_dual_rail_children NAND
      . > has_dual_rail_children NOR
        > nextbox findtt(TWO_LEVEL,BOX(2),LIMITED)
>>]: nextbox( findtt(TWO_LEVEL,BOX(2),LIMITED) );
[BD-500000]: findtt CMVC version 1.17 compiled on Apr 13 1999 at 18:23:54
[create_table_from_view]: No table generated for def cl_scan view EQNVIEW.
limit search to two levels.
number of boxes covered by each pattern; 2.
limit search to offset.
[BD-502100]: Found 35 patterns.
[findtt]: Execution time was 0.1 seconds.
        > nextbox findtt(TWO_LEVEL,BOX(3),LIMITED)
>>]: nextbox( findtt(TWO_LEVEL,BOX(3),LIMITED) );
[create_table_from_view]: No table generated for def cl_scan view EQNVIEW.
limit search to two levels.
number of boxes covered by each pattern: 3.
limit search to offset.
[BD-502100]: Found 0 patterns.
[findtt]: Execution time was 0.0 seconds.
        > nextbox tkern
>>]: nextbox( tkern );
```

```
[tkern]: (W) No AND def - tkern will not apply.
[tkern]: generated patterns for 0 nets
          > get_default_delay_synlimit
           > tc_parm OFFSET(0)
         > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
         > nextbox powerize
>>]: nextbox( powerize );
[BD-80000]: powerize CMVC version 1.9 compiled on Apr 8 1999 at 05:26:08
[BD-85000]: Changed power level of 35 patterns, added 0 patterns.
         > quick trecover(SCORE(ALL), RE_POWER, INC, SORT_PINS, NO1FAN,...
>>]: [quick]:( trecover(SCORE(ALL),RE_POWER,INC,SORT_PINS,NO1FAN,NO_VIOLATIONS) );
-1967.14 Avg: -200.49
[trecover]: Compiled on Apr 13 1999 at 18:27:36.
[trecover]: setting SCORE option to ALL.
[trecover]: setting RE_POWER option.
[trecover]: setting INC mode.
[trecover]: setting SORT_PINS option.
[trecover]: setting NO1FAN option.
[trecover]: setting NO_VIOLATIONS option.
-1967.14 Avg: -200.49
maximum area for proto box IDCDSUC is 4599
-1967.14 Avg: -200.49
Selected 398 critical boxes of 922 total.
[quick]: Number of boxes to process is 398.
[quick]: Number of boxes processed is 0.
-1967.14 Avg: -189.91
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[trecover]: 309 boxes checked 3 recovered
[trecover]: Execution time was 2.2 seconds.
       > measure
 The model <IDCDSUC> has:
 Primary Inputs
                              122
 Primary Outputs
                                73
 Primary BIDIs
                               0
                           1141
 Signals
 Gate Count
                              918
                              1756
 Connections
 Master REG Bits
                                83
                                83
 Slave REG Bits
                             4603
 Internal Area
 External Area
                               0
                             0.522779
 Gates/Connects
 Fanout Count
                              1756
```

Average Fanout

1.539001

Tech Box Size Stddev = 0.010883 0.000000 Power \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\* Real signals = 766 Real boxes 543 Real connections 1381 Real LSTs 2147 Real ICells/box 8.476980 Real LSTs/box 3.953959 Real nets/box 1.410681 Cell Total Each Cell Type Cnt Boxname Power Level Function Int Ext Power Int Ext Power 7 cs\_ao22n03c 03c **AOI** 6 0 0.000 42 0 0.000 2 cs\_ao12n03c 03c > **AOI** 4 0 0.000 8 0 0.000 cs\_ao12n10c 10c **AOI** 12 0 0.000 12 > 0 0.000 1 cs\_ao22n10c 10c 18 > AOI 0 0.000 18 0 0.000 1 cs\_ao12n04c 04c **AOI** 4 0 0.000 4 0 0.000 180 **BRKPT BRKPT** 0 0 0.000 0 0 0.000 > 195 **IOPAD** -IOPAD 0 0 0.000 ..> 0 0-0.000 .. > 160 cs nnd2n02c 02c NAND 480 3. 0 0.000 0.000 1 cs\_nnd2n10c 10c NAND 8 0 0.000 8 0.: 0.000 > 2 cs\_nnd2n12c 12c 12 NAND 0 0.000 24 > -0 0.000 21 cs\_nnd3n02c 02c > NAND 4 0 0.000 ...84 0 0.000... 2 cs\_nnd2n09c. 09c ..> NAND 7... 0 0.000 14 0 0.000 3 cs\_nnd2n03c 03c NAND 3 9 0 > 0 0.000 0.000 5 cs\_nnd4n03c 03c > NAND 5 ...0 0.000 25 0 0.000 2 cs\_nnd2n11c 11c **NAND** 0 22 > 11 0.000 0 0.000 : 7 cs\_nnd2n14c 14c **NAND** 19 0 133 > 0.000 : 0 0.000 3 cs\_nnd2n08c 08c **NAND** 7 0 0.000 > 21 0 0.000 1 0.000 cs\_nnd3n07c 07c **NAND** > 6 0 6 0 0.000 1 cs\_nnd2n14e 14e > NAND 0 0.000 0 19 19 0.000 1 cs nnd2n04c 04c > NAND 3 0:000 0-3 0 0.000 2 cs nnd2n07c 07c **NAND** 4 0.000 > 0 8 0 0.000 1 cs\_nnd2n14b 14b > NAND 20 0 0.000 20 0 0.000 1 cs\_nnd3n12c 0.000 12c > NAND 22 0 0.000 22 0 2 cs nnd4n10c 10c > NAND 20 0 0.000 40 0 0.000 2 cs\_nnd3n05c 05c > NAND 6 0 0.000 12 0 0.000 1 cs\_nnd2n05c 05c > NAND 4 0 0.000 4 0 0.000 1 cs\_nnd3n10c 10c > NAND 12 0 0.000 12 0.000 cs\_nnd2f03c 1 03c NAND 4 0 4 > 0.000 0 0.000 1 cs\_nnd3z07c 07c NAND 10 0.000 10 > 0 0.000 0 2 cs\_nnd4v06c 06c > NAND 8 0 0.000 16 0 0.000 10 cs\_nor2n02c 02c NOR 3 0 0.000 > 30 0 0.000 1 cs\_nor3n03c 03c NOR 4 0 > 0.000 4 0 0.000 1 cs nor2n12c 12c NOR 12 0 0.000 12 > 0.000 1 cs\_nor2n04c 04c NOR 3 0 > 0.000 3 0 0.000 1 cs nor3n10e 10e NOR 16 0.000 > 0 16 0 0.000 1 cs\_nor2n11c 11 11c > NOR 0 0.000 11 0 0.000 88 cs\_invvn01c 01c > NOT 2 0 0.000 176 0 0.000 4 cs\_invvn11c NOT 11c > 6 0 0.000 24 0.000 6 cs\_invvn10c 10c NOT 4 0 > 0.000 24 0.000 21 cs\_invvn12c 12c NOT 6 0 0.000 126 0 0.000

Avg Tech Box Size =

5.014161

```
0.000
                                                   0
                                                      0.000
                                                             24
                                                                   0
                                       NOT
                                              4
    cs_invvn09c
                            09c
6
                                 >
                                               2
                                       NOT
                                                   0
                                                      0.000
                                                             44
                                                                   0
                                                                      0.000
                            07c
     cs_invvn07c
                                  >
22
                                              10
                                                   0
                                                      0.000
                                                              40
                                                                   0
                                                                      0.000
                                       NOT
    cs_invvn15c
                            15c
4
                                 >
                                              2
                                                                      0.000
                                                   0
                                                      0.000
                                                             16
                                                                   0
                            06c
                                 >
                                       NOT
8
    cs_invvn06c
                                               2
                                                      0.000
                                                              24
                                                                   0
                                                                      0.000
                            05c
                                  >
                                       NOT
                                                   0
12
     cs_invvn05c
                                                             48
                                                                   0
                                                                      0.000
                                       NOT
                                              8
                                                   0
                                                      0.000
                            13c
6
    cs_invvn13c
                                 >
                                                                   0
                                                                      0.000
                                       NOT
                                              10
                                                   0
                                                      0.000
                                                              10
                            14b
1
    cs_invvn14b
                                  >
                                                                      0.000
                                              4
                                                   0
                                                      0.000
                                                             20
                                                                   0
                                       NOT
5
    cs invvn08c
                            08c
                                  >
                                                                      0.000
                                              2
                                                             12
                                                                   0
                                                   0
                                                      0.000
    cs_invvn02c
                            02c
                                 >
                                       NOT
6
                                                                      0.000
                                       NOT
                                                   0
                                                      0.000
                                                             24
                                                                   0
                            14c
                                              8
3
    cs invvn14c
                                 >
                                                                  0
                                                                     0.000
                                              2
                                                   0
                                                      0.000
                                                              6
    cs_invvn04c
                                       NOT
3
                            04c
                                  >
                                                              25
                                                                   0.
                                                                      0.000...
                                       NOT
                                              25
                                                   0
                                                      0.000
                            19c
1
    cs_invvn19c
                                  >
                                       NOT
                                              14
                                                   0
                                                      0.000
                                                              28
                                                                   0
                                                                      0.000
2
    cs invvn16c
                            16c
                                                                   0.000
                                              14
                                                   0
                                                      0.000
                                                              28
                             10c
                                        OAI
2
    cs_oa21n10c
                                  >
                                                              6
                                                                  0.000
                             03c
                                  >
                                        OAI
                                              6
                                                   0
                                                      0.000
1
     cs_oa22n03c
                                                      0.000
                                                              550
                                                                    0
                                                                       0.000
                                       REG
                                              25
                                                   0
     cl_invvn07c
                            07c
22
                                                      0.000
                                                              750
                                                                    0.000
                                              25
                                                    0
                            07d
                                       REG
     cl_invvn07d
                                  >
30
                                                                     0.000
                                        REG
                                              26
                                                    0
                                                       0.000
                                                              468
                             07c
18
     cl nnd2n07c
                                  >
                                                                      0.000
                                              33
                                                       0.000
                                                              264
                                                                    0
                                                    0
                            07c
                                        REG
8
    cl ao22n07c
                                                                    0.000
                                                       0.000
                                                              58
                                              29
                                                    0
                            07c
                                        REG
2
    cl_nnd3n07c
                                  >
                                                              26
                                                                   0
                                                                       0.000
                                       REG
                                              26
                                                   0
                                                      0.000
                            06c
     cl_nor2n06c
                                  >
1
                                                       0.000
                                                              30
                                                                    0
                                                                       0.000
                                                    0
                                        REG
                                              30
     cl ao21n07c
                            07c
                                  >
1
                                                                       0.000
                                                       0.000
                                                              30
                                                                    0
                                              30
                                                    0
     cl_oa21n07c
                            07c
                                        REG
1
                                                                    70
                                                                         0.000
                                  > SEQUENTIAL
                                                   70
                                                         0.000
     cb_mode_block
                                                                       0.000
                                 > SEQUENTIAL 80
                                                         0.000 480
     cb clk_32_1
                                                      0
6
                                                8
                                                       0.000
                                                                8
                                                                    0
                                                                       0.000
     cs_xbn2n01b
                             01b
                                   >
                                        XNOR
                                                     0
 1
                             01d >
                                        XOR 8
                                                    0.000
                                                                       0.000
     cs_xbo2n01d
```

```
# of
Levels Output
  0
         1
              50* plus *****
        55
  1
  2
         1
  3
         8
  4
         1
 10
         3
 11
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 2
        20
 3
        1
        5
 4
 5
        3
 6
        10
 7
        3
 9
        1
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
   2
1
   938
      99
   17
5
   7
6
   11
7
   3
8
   3
13
    3
14
   16
20
    1
```

## [End of measure]

```
[measure]: Execution time was 0.6 seconds.
```

> critical repower(SCORE(ALL),INC,NO\_VIOLATIONS),clone(SCO...

critical(

repower(SCORE(ALL),INC,NO\_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE\_POWER,INC,NO\_VIOLATIONS),fantom(LIMITED),faninv(LIMITED));

-1967.14 Avg: -189.91

maximum area for proto box IDCDSUC is 4603

repower: setting SCORE option to ALL.

repower: setting INC mode.

repower: setting NO\_VIOLATIONS option.

setting SCORE option to ALL.

setting ACTUAL option.

setting RE\_POWER option.

setting INC mode.

setting NO\_VIOLATIONS option.

fantom: Found 152 valid buffers or inverters.

[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.

```
[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
-1967.14 Avg: -189.91
ArrayNum: 6 ArrayMax: 918
-1963.71 Avg: -189.33
ArrayNum: 9 ArrayMax: 918
IBD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.2 seconds.
[BD-500700]: Added 0 buffers.
[fantom]: Execution time was 0.0 seconds.
[BD-500701]: Added 1 inverters.
[faninv]: Execution time was 2.0 seconds.
[BD-502000]: Called transforms 48 times and applied 1 of them.
       > nextbox synexpand(XPANDVIEW)
>>1: nextbox( synexpand(XPANDVIEW) );
[restore_pin_keywords]: restored 0 keywords
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[restore_pin_keywords]: deleted 0 nets and pins
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                 The model has 1142 signals, 919 usage boxes and 1757 connections.
>>1: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
       > measure
 The model <IDCDSUC> has:
                               122
  Primary Inputs
  Primary Outputs
                                73
                                0
  Primary BIDIs
  Signals
                            1142
                              919
  Gate Count
                              1757
  Connections
  Master REG Bits
                                 83
  Slave REG Bits
                                83
                             4623
  Internal Area
  External Area
                                0
                              0.523051
  Gates/Connects
  Fanout Count
                              1757
  Average Fanout
                             1.538529
                              5.030468
  Avg Tech Box Size =
                                0.010896
  Tech Box Size Stddev =
  Power
                          0.000000
 ***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
                              767
  Real signals
```

Real boxes 544 Real connections 1382 Real LSTs 2149 Real ICells/box 8.498162 = Real LSTs/box 3.950368 Real nets/box = 1.409926 Cell Total Each Cell Type Cnt Boxname Power Level Function Int Ext Power Int Ext 7 cs\_ao22n03c 03c AOI 6 42 0 0.000 0 0.000 > 2 cs\_ao12n03c 03c AOI 4 0 0.000 8 0. > 0.000 cs ao12n10c 1 10c **AOI** 12 0 0.000 > 12 0 0.000 cs\_ao22n10c 1 10c AOI 18 0 0.000 > 18 0 0.000 1 cs\_ao12n04c 04c > AOI 4 0 0.000 4 0 0.000 180 **BRKPT BRKPT** 0 0 0.000 0 0 > 0.000 195 **IOPAD IOPAD** 0 > 0 0.000 0 0 0.000 160 cs nnd2n02c 02c **NAND** > 3 0 0.000 480 0.000 0 1 cs\_nnd2n10c 10c **NAND** 8 0 0.000 8 0.000 > 0 2 cs\_nnd2n12c 12c NAND 12 0 0.000 24 0.000 0 21 cs\_nnd3n02c 02c > **NAND** 4 0 0.000 84 0 0.000 2 cs\_nnd2n09c 09c **NAND** 7 > 0 0.000 14 0 0.000 3 cs nnd2n03c 03c > NAND 3. 0 0.000 9 0.000 0 5 cs nnd4n03c 03c > NAND 5 0 0.000 25 0 0.000 2 cs\_nnd2n11c 11c NAND 11 0 0.000 22 0 0.000 7 cs\_nnd2n14c 14c > NAND 19 0 0.000 133 0 0.000 3 cs\_nnd2n08c -08c NAND <u>.</u> .7.. > 0 0.000 21 0.000 1 cs nnd3n07c 07c > **NAND** 6 0 0.0000 0.000 6 1 cs\_nnd2n14e 14e NAND 0 > 19 0.000 19 0 0.000 1 cs\_nnd2n04c 04c **NAND** 3 0 > 0.000 3 0 0.000 2 cs\_nnd2n07c 07c NAND 4 0 0.000 > 8 0 0.000 1 cs\_nnd2n14b 14b > NAND 20 0 0.000 20 0 0.000 1 cs\_nnd3n12c 12c **NAND** 22 0 0.000 > 22 0 0.000 2 cs nnd4n10c 10c **NAND** 20 > 0 0.000 40 0 0.000 2 cs\_nnd3n05c 05c **NAND** > 0 6 0.000 12 0 0.000 1 cs\_nnd2n05c 05c > NAND 4 0 0.000 4 0 0.000 1 cs\_nnd3n10c 10c NAND 12 0 0.000 12 > 0 0.000 1 cs\_nnd2f03c 03c NAND 0 > 4 0.000 4 0 0.000 1 cs\_nnd3z07c 10 07c > NAND 0 0.000 10 0 0.000 2 cs nnd4v06c 06c NAND > 8 0 0.000 16 0 0.000 10 cs nor2n02c 02c NOR 0.000 > 3 0 30 0 0.000 1 cs\_nor3n03c 03c > NOR 4 0 0.000 4 0 0.000 1 cs\_nor2n12c 12c > NOR 12 0 0.000 12 0 0.000 1 cs nor2n04c 04c > NOR 3 0 0.000 3 0 0.000 1 cs\_nor3n10e 10e > NOR 16 0 0.000 16 0.000 0 1 cs\_nor2n11c 11c > NOR 11 0 0.000 11 0.000 0 88 cs\_invvn01c 01c NOT 2 > 0 0.000 176 0 0.000 4 cs\_invvn11c 11c NOT 6 0 0.000 24 > 0 0.000 6 cs\_invvn10c 10c NOT > 4 0 0.000 24 0 0.000 21 cs\_invvn12c 12c NOT 6 0 0.000 > 126 0 0.000 6 cs\_invvn09c 09c 0 NOT 4 0.000 24 0.000 > 0 22 cs invvn07c 07c 2 > NOT 0 0.000 44 0 0.000 4 cs invvn15c 15c NOT 0 > 10 0.000 40 0 0.000 8 cs\_invvn06c 06c > NOT 2 0 0.000 16 0 0.000 12 cs invvn05c 05c NOT 2 0 0.000 24 0 0.000

```
NOT
                                              8
                                                  0
                                                     0.000
                                                             48
                                                                  0
                                                                     0.000
                           13c
6
    cs_invvn13c
                                 >
                                       NOT
                                             28
                                                  0
                                                     0.000
                                                             28
                                                                  0
                                                                     0.000
                           19b
1
    cs invvv19b
                                 >
                                                             20
                                                                  0
                                                                     0.000
                                              4
                                                  0
                                                     0.000
                                      NOT
5
    cs_invvn08c
                           08c
                                 >
                                                                  0
                                                                     0.000
                           02c
                                 >
                                       NOT
                                              2
                                                  0
                                                     0.000
                                                             12
6
    cs_invvn02c
                                                                     0.000
                                      NOT
                                              8
                                                  0
                                                     0.000
                                                             24
                                                                  0
                           14c
3
    cs_invvn14c
                                 >
                                              2
                                                     0.000
                                                             6
                                                                 0
                                                                    0.000
    cs_invvn04c
                                       NOT
                                                  0
3
                           04c
                                 >
                                             25
                                                     0.000
                                                             25
                                                                  0
                                                                     0.000
                                       NOT
                                                  0
                           19c
1
    cs invvn19c
                                 >
                                                     0.000
                                                             28
                                                                  0.000
                                                  0
                           16c
                                 >
                                       NOT
                                             14
2
    cs_invvn16c
                                              2
                                                             2
                                                                  0
                                                                    0.000
                           01e
                                 >
                                       NOT
                                                  0
                                                     0.000
1
    cs_invvn01e
                                                     0.000
                                                             28
                                                                   0.000
                                       OAI
                                             14
                                                  0
                                  >
2
    cs_oa21n10c
                            10c
                                                                    0.000
                                              6
                                                  0
                                                     0.000
                                                             6
                                                                  0
                            03c
                                       OAL
1
    cs_oa22n03c
                                  >
                                             25
                                                  0
                                                      0.000
                                                             550
                                                                   0
                                                                      0.000
                           07c
                                       REG
     cl_invvn07c
22
                                 >
                                                   0
                                                      0.000
                                                             750
                                                                   0
                                                                      0.000
                                              25
     cl invvn07d
                           07d
                                       REG
30
                                                                      0.000
                            07c
                                       REG
                                              26
                                                   0
                                                      0.000
                                                             468
                                                                    0
     cl_nnd2n07c
18
                                                                   0
                            07c
                                       REG
                                              33
                                                   0
                                                      0.000
                                                             264
                                                                       0.000
    cl_ao22n07c
                                 >
8
                                                                      0.000
                                              29
                                                      0.000
                                                              58
                                                                   0
                                       REG
                                                   0
2
    cl nnd3n07c
                            07c
                                 >
                                                                      0.000
                                                                   0
                                       REG
                                             26
                                                   0
                                                      0.000
                                                             26
                           06c
                                 >
1
    cl_nor2n06c
                                                      0.000
                                                              30
                                                                   0
                                                                      0.000
                                              30
                                                   0
                                       REG
1
    cl_ao21n07c
                            07c
                                 >
                                                      0.000
                                                              30
                                                                   0
                                                                      0.000
                                              30
                                                   0
1
    cl_oa21n07c
                            07c
                                 >
                                       REG
                                                                        0.000
                                                                   70
                                                        0.000
                                 > SEQUENTIAL
                                                   70
    cb_mode_block
1
                                                      0 0.000 480
                                                                      0.000
                                > SEQUENTIAL 80
6
    cb_clk_32_1
                                                      0.000
                                                               8
                                                                   0.000
                                                    0
                             01b
                                       XNOR
                                                8
1
    cs_xbn2n01b
                                  >
                                                 .. 0 ..0.000
                                                               8
                                                                   0.000
                             01d
                                        XOR
                                               8
    cs_xbo2n01d
                                  >
```

```
# of
Levels Output
0
 1
        55
              50* plus
 2
        1.
 3
        8
 4
        1
 10
         3
 11
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
        7
 0
 2
        20
  3
        1
  4
        5
  5
        3
  6
        10
  7
         3
  9
         1
 10
         6
 12
         1
 13
         2
 14
         7
```

```
15
        7
 16
        3
 17
        14
The Histogram Of Fanin vs. Box
   # of
Fanin
        Ops
  1
       379
              350* plus *****
 2
       202
             200* plus **
  3
       35
  4
       18
The Histogram Of Fanout vs. Net
   # of
Fanout Nets
 0
       2
 1
       940
 2
       97
 3
       42
       17
       11
 13
        3
 14
       16
 20
[End of measure]
[measure]: Execution time was 0.6 seconds.
      > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 21:59:52 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                       EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                   Max. Slack: 1.13427E+38
Sort Field: Slack
                                Max. Endpoints: 3
Cause of Slack
                        Abbreviation Comparison/Description
Slack Continuation
                         SIkCont
                                    Slack due to a point downstream on path
Required Arrival Time
                          RAT
                                     ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
Asserted Required Arrival Time AssrtRAT
                                          ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
Clock Gating Setup
                          ClkGSet
                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold
                         CIkGHId
                                     ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
```

```
ARRIVAL TIME + ADJUST )
                        CIKTPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
Clock Tree Pulse Width
TRAILING EDGE)
                           ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                  Setup
Setup
ADJUST )
                          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                  Hold
Hold
ADJUST )
                               ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                    EndOfC
 EndOfCycle
ADJUST)
                                ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                      CIkPW
ClockPulseWidth
TRAILING EDGE)
                                ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
                      ClkSep
 ClockSeparation
ARRIVAL TIME + ADJUST )
                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                  ALTest
 Loop
CLOCK + ADJUST)
                                Slack discontinuity due to failed test
 Arrival Time Limiting
                      ATLimit
                                                                Delay/ Failed Test/
                                LimitedAT/
  Num/
                                         AT Slack Slew CL FO Cell
                                                                       P Func T.Adi
                               E Phase
 Test PinName
NetName
                                          2963 -1964 3847 1011 1 PO
                                R C3+R
   1 dcd_succ_last_t1
dcd_succ_last_t1
                            RAT
                                          2963 -1964 3847 1011 1 IOPAD
                                 RC3+R
----> BOX714/OUT
0 dcd succ_last_t1
                            R C3+R 2963 -1964 3847 1011 1 IOPAD IOPAD
----> BOX714/IN
0 dcd_succ_last_t1&0
                             R C3+R 2963 -1964 3847 1011 1 cs_invvn 01c NOT
----> C167/y
0 dcd succ_last_t1&0
                                                    55 139 4 cs_invvn 01c NOT
                                       1101 -1964
                              FC3+R
----> C167/a
1862 N675
                                                     55 139 4 cs_nnd2n 14b NAND
                              F C3+R
                                        1101 -1964
---->{a} C2738/y
0 N675
                                                     90 159 3 cs_nnd2n 14b NAND
                                        1069 -1964
                              R C3+R
----> C2738/b
31 N1692
                                                         159 3 cs_nnd2n 14c NAND
                                RC3+R
                                         1069 -1964
---->{b} C2725rwr/y
0 N1692
                                                      93 167 2 cs_nnd2n 14c NAND
                                         1020 -1964
                               FC3+R
----> C2725rwr/a
49 N1479
                                                      93
                                                         167 2 cs nnd3n 12c NAND
                                FC3+R
                                         1020 -1964
---->{c} C2721rwr/y
0 N1479
                                                     157 95 2 cs_nnd3n 12c NAND
                               R C3+R
                                         962 -1964
----> C2721rwr/c
58 N1497
                                                           95 2 cs_nor3n 10e NOR
                                          962 -1964
                                                     157
                                R C3+R
---->{d} C2709rwr/y
0 N1497
                                         899 -1964
                                                     50 54 1 cs nor3n 10e NOR
                                FC3+R
----> C2709rwr/a
64 N1986
                                                           54 1 cs_nnd2n 12c NAND
                                 FC3+R
                                           899 -1964
                                                       50
---->{e} C2677rwr_0/y
0 N1986
                                                      75
                                                           89 2 cs_nnd2n 12c NAND
                                R C3+R
                                          872 -1964
----> C2677rwr 0/a
26 N1094
                                                    75 89 2 cs_nnd2n 14c NAND
                               R C3+R
                                         872 -1964
---->{f} C2909/y
0 N1094
```

C2909/a	F C3+R 835 -1964 80 108 1 cs_nnd2n 14c NAND
cd_mcr41_blk&0 BOX615/OUT d_mcr41_blk&0	F C3+R 835 -1964 80 108 1 IOPAD IOPAD
BOX615/IN mcr41_blk	F C3+R 835 -1964 80 108 1 IOPAD IOPAD 0
dcd_mcr41_blk mcr41_blk	F C3+R 835 -1964 80 108 1 PI 0
2 dcd_succ_last_t1	F C3+R 2616 -1617 2362 1011 1 PO 0
succ_last_t1	
DOV714/OLIT	999 0 F C3+R 2616 -1617 2362 1011 1 IOPAD IOPAD
BOX714/OUT d_succ_last_t1	F C3+R 2616 -1617 2362 1011 1 IOPAD IOPAD
BOX714/IN	F C3+R 2616 -1617 2362 1011 1 IOPAD IOPAD
d_succ_last_t1&0	TOTAL ZOTO TOTAL ZOOZ TOTAL TOTAL
C167/y	F C3+R 2616 -1617 2362 1011 1 cs_invvn 01c NOT
d_succ_last_t1&0	
C167/a	R C3+R 1180 -1617 92 139 4 cs_invvn 01c NOT
N675	
(a) C2738/y	R C3+R 1180 -1617 92 139 4 cs_nnd2n 14b NAND
675 - C2729/b	F C3+R 1128 -1617 63 159 3 cs_nnd2n 14b NAND
C2738/b 11692	F C3+H 1128 -1017 03 139 3 CS_HHUZH 140 NAND
(b) C2725rwr/y	F C3+R 1128 -1617 63 159 3 cs_nnd2n 14c NAND
1692	
	R C3+R 1086 -1617 134 167 2 cs_nnd2n 14c NAND
<b>\1479</b>	
(c) C2721rwr/y	R C3+R 1086 -1617 134 167 2 cs_nnd3n 12c NAND
1479	E CO. D
C2721rwr/c 11497	F C3+R 994 -1617 125 95 2 cs_nnd3n 12c NAND
[d] C2709rwr/y	F C3+R 994 -1617 125 95 2 cs_nor3n 10e NOR
1497	1 00111 001 1017 120 00 2 00_1101011 100 NOTE
C2709rwr/c	R C3+R 898 -1617 137 68 2 cs_nor3n 10e NOR
l1781	
(e) C2885/y	R C3+R 898 -1617 137 68 2 cs_nnd4n 10c NAND
1781	E CO. D
C2885/d 11997	F C3+R 825 -1617 44 50 1 cs_nnd4n 10c NAND
	F C3+R 825 -1617 44 50 1 cs nnd2n 14c NAND
	1 00111 020 1017 44 00 1 00_1110211 140 14/14D
C2886/a	R C3+R 802 -1617 80 124 2 cs_nnd2n 14c NAND
p_serialize&0	
BOX638/OUT	R C3+R 802 -1617 80 124 2 IOPAD IOPAD
	D.O. D
	R C3+R 802 -1617 80 124 2 IOPAD IOPAD 0
	B C3+B 802 -1617 80 124 2 DI 0
• —	11 OUTH OUZ -1017 OU 124 2 PI U
(f) C2886/y 1997 C2886/a p_serialize&0 BOX638/OUT p_serialize&0 BOX638/IN erialize op_serialize erialize	R C3+R 802 -1617 80 124 2 IOPAD IOPAI R C3+R 802 -1617 80 124 2 IOPAD IOPAD R C3+R 802 -1617 80 124 2 PI 0

```
999
RAT
                                                                            IOPAD
                                          2431 -1432 3912 1011 1 IOPAD
                                 R C3+R
----> BOX716/OUT
0 iu_reset_op_c_t1
                                        2431 -1432 3912 1044 3 IOPAD
                                                                           IOPAD
                               R C3+R
---> BOX716/IN
0 iu_reset_op_c_t1&0
                                        2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
                              RC3+R
---->{a} C2393/y
0 iu reset_op_c_t1&0
                                                   78 137 3 cs_nnd2n 02c NAND
                                       473 -1432
                              FC3+R
----> C2393/a
1958 gbfonet_6
                                                                                  0
                                                    78 137 3 cs_invvn 09c NOT
                              FC3+R
                                        473 -1432
----> qbfocell_6/y
qbfonet_6
                                        410 -1432
                                                    217
                                                        43 1 cs invvn 09c NOT
                              R C3+R
----> gbfocell_6/a
64 N2031
                                                    217 43 1 cs_nnd3n 02c NAND
                              R C3+R
                                        410 -1432
---->{b} C2162/y
0 N2031
                                                    57 49 3 cs_nnd3n 02c NAND
                                        303 -1432
                              FC3+R
----> C2162/b
107 rcvry_reset_q
                                                          57 49 3 cl_invvn 07d SRL
                                              303 -1432
----> rcvry_reset.reg_n.lat_0/l2_out_n
                                    FC3+R
0 rcvry_reset_q
                                                       60 222 13 cl_invvn 07d SRL
----> rcvry_reset.reg_n.lat_0/c2 R C3+
                                            160
                                                 N/C
143 slow_mode.c2_1
                                             160 N/C 60 222 13 cb_clk_32_1 LCB
----> slow_mode.clockblock/c2
                                   R C3+
0 slow_mode.c2_1
_____
<u>...</u>
  > treematch {ACTUAL ,TWO_LEVEL,NO_VIOLATIONS}
->>]: ltorbox( dtreematch(ACTUAL ,TWO_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1963.71 Avg: -189.33
[BD-500301]: 8 pins on 3 gates swapped.
[treematch]: Execution time was 0.9 seconds.
>>]: Itorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1963.69 Avg: -190.04
[BD-500300]: 25 pins on 11 gates swapped.
-1963.71 Avg: -189.83
[fanmatch]: Execution time was 3.7 seconds.
       > get_default_delay_synlimit
```

[tc\_parm]: [set\_benefit\_per\_unit\_cost]: unit cost is 4.000000 [tc\_parm]: [set\_benefit\_per\_unit\_cost]: benefit\_units is 0.000172 [tc\_parm]: [set\_benefit\_per\_unit\_cost]: benefit is 1.000000 [tc\_parm]: [set\_benefit\_per\_unit\_cost]: weight is 4.000000

> tc parm {WEIGHTED\_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),W...

> reset\_critical\_slack\_limit

> tc\_parm OFFSET(0)

```
-1963.71 Avg: -189.83
resetting the current slack to -1963.7057
       > repower_paths FUZZY(0.02)
initial slack is -1964
after repower paths slack is -1964
       > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS), repower...
critical( repower(SCORE(ALL),INC.NO VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1963.71 Avg: -189.46
maximum area for proto box IDCDSUC is 4648
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1963.71 Avg: -189.46
ArrayNum: 9 ArrayMax: 919
-1956.14 Avg: -188.82
ArrayNum: 9 ArrayMax: 919
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
IBD-5000261: repower was applied 2 times.
[repower]: Execution time was 0.6 seconds.
[BD-500026]: repower was applied 2 times.
[repower]: Execution time was 0.6 seconds.
[BD-502000]: Called transforms 32 times and applied 2 of them.
        > compare_critical_slack_limit
3 Avg: -188.47
-1955.13 Avg: -188.47
comparing new slack -1955.1339 to saved slack -1944.0686
        > syntrace
          > write_end_point_report -points 10
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:00:16 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                      EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                   Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
Sort Field: Slack
                                Max. Endpoints: 10
 Cause of Slack
                        Abbreviation Comparison/Description
                         SlkCont
                                    Slack due to a point downstream on path
 Slack Continuation
                          RAT
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
                                         ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 Clock Gating Setup
                          ClkGSet
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                                     ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                         ClkGHld
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                           CIKTPW
                                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
                               ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 Setup
                     Setup
```

	ADJUST ) Hold	Hold (DA	ATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
	ADJUST ) EndOfCycle	EndOfC	( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
	ADJUST) ClockPulseWidth	CIkPW	( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
	TRAILING EDGE ) ClockSeparation	ClkSep	( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
	ARRIVAL TIME + ADJ	UST) ALTest ([	DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
	CLOCK + ADJUST ) Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test
	Num/ Test PinName		LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
	NetName		
	1 dcd_succ_last_t dcd_succ_last_t1	:1	R C3+R 2954 -1955 3847 1011 1 PO 0
	RAT> BOX714/OUT		999 R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1> BOX714/IN		R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
-	0 dcd_succ_last_t1&0		R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	)	F C3+R 1092 -1955 55 139 4 cs_invvn 01c NOT-
- · · · · · · · · · · · · · · · · · · ·	1862 N675 >{a} C2738/y		F C3+R 1092 -1955 55 139 4.cs_nnd2n 14b NAND
: -	0 N675 > C2738/a		R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
	29 last_cycle >{b} C2487/y	÷	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND
	0 last_cycle > C2487/b	·	F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
	29 N1587 > C1952/y N1587		F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
	> C1952/a 10 num_dcd_cyl&0(1	١	R C3+R 1024 -1955 80 319 1 cs_invvv 19b NOT
	> BOX679/OUT 0 num_dcd_cyl&0(1)	,	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
	> BOX679/IN		R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
	num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)		R C3+R 1024 -1955 80 319 1 PI 0
	2 dcd_succ_last_		F C3+R 2644 -1645 2362 1011 1 PO 0
	dcd_succ_last_t1 RAT		999 0
	O dcd_succ_last_t1> BOX714/IN		F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD

	0 dcd_succ_last_t1&0	
	> C167/y	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	
	> C167/a	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
	1436 N675	
	>{a} C2738/y	R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
	0 N675	
	> C2738/b	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
	56 N1692	E 00. D 4450 4045 70 450 0 10 44 110 D
	>{b} C2725rwr/y 0 N1692	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND
	> C2725rwr/a	R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND
	56 N1479	11 05+11 1097 -1045 146 100 2 CS_11110211 146 146 140D
	>{c} C2721rwr/y	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
	0 N1479	11 30111 1001 1040 140 100 2 03_11110011 12D 14A11D
	> C2721rwr/c	F C3+R 994 -1645 125 95 2 cs_nnd3n 12b NAND
	102 N1497	
	>{d} C2709rwr/y	F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
	0 N1497	
	> C2709rwr/c	R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR
	96 N1781	
		R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
	0 N1781	5 00 D
	> C2885/d	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
**************************************	73 N1997 >{f} C2886/y	EC2.D 995 1645 44 50 1 ap madon 44 NAND
	0 N1997	F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
	> C2886/a	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
	23 op_serialize&0	TOTAL TOTAL TOTAL TO THE TENT OF THE TANKE
	> BOX638/OUT	R C3+R 802 -1645 80 124-2 IOPAD IOPAD
	0 op serialize&0	
	> BOX638/IN	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
e va	an assistina	No.
*	> op_serialize	R C3+R 802 -1645 80 124 2 Pl
And the second	op_serialize	<u> </u>
	3 in reset on c t1	R C3+R 2431 -1432 3912 1011 1 PO 0
	iu_reset_op_c_t1	H C3+R 2431 -1432 3912 1011 1 PO 0
	RAT	999 0
	> BOX716/OUT	R C3+R 2431 -1432 3912 1011 1 IOPAD IOPAD
	0 iu_reset_op_c_t1	101710
	> BOX716/IN	R C3+R 2431 -1432 3912 1044 3 IOPAD IOPAD
	0 iu_reset_op_c_t1&0	
	>{a} C2393/y	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
	0 iu_reset_op_c_t1&0	F.00 B. 450 440 50 400 50 400 50 50 50 50 50 50 50 50 50 50 50 50 5
	> C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
	1958 gbfonet_6> gbfocell_6/y	ECO.D 470 4400 70 407 0 ' 00 NOT 0
	gbfonet_6	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
	> gbfocell_6/a	R C3+R 410 -1432 217 43 1 cs invvn 09c NOT
	64 N2031	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
	>{b} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
	0 N2031	1. 55 1.6 1.62 217 16 1.65_HINGOH 026 NAME
	> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND

	107 rcvry_reset_q	n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
	> rcvry_reset.reg_n.lat_0/l2_out_ 0 rcvry_reset_q	_N P C3+N 303 -1432 37 43 3 61_1114411 374 3112
	> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	143 slow mode.c2 1	
	> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
(	0 slow_mode.c2_1	
	4 local_milli_t2.reg_n.lat_0/a 51 NET1056	000 44 1 June 07a
	Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
	1200 slow_mode.c1_4 >{a} BOX789/y	F C3+R 2675 -1366 103 92 3 cs_nnd3z 07c NAND
	0 NET1056	
	> BOX789/b	R C3+R 2620 -1366 139 36 1 cs_nnd3z 07c NAND
	55 NET1054 >{b} BOX785/y	R C3+R 2620 -1366 139 36 1 cs_nnd2f 03c NAND
	0 NET1054	****
	> BOX785/a	F C3+R 2542 -1366 116 19 1 cs_nnd2f 03c NAND
	78 N1866	F C3+R 2542 -1366 116 19 1 cs_ao12n 03c AOI
	>{c} C2555/y 0 N1866	F C3+R 2342 -1300 110 13 1 63_4012H 65676H
	> C2555/b	R C3+R 2431 -1366 3912 1044 3 cs_ao12n 03c AOI
	110 iu_reset_op_c_t1&0	D 00 D 0404 1400 2010 1044 2 co ppd2p 020 NAND
	>{d} C2393/y	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
	0 iu_reset_op_c_t1&0 > C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND-
	1958 abtonet 6	
		F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
	gbfonet_6> gbfocell_6/a	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
	64 N2031	
		R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
	0 N2031 > C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
	107 revry reset a	
		_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
	0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	143 slow_mode.c2_1	11 001 100 100 00 222 10 02
	> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	0 slow_mode.c2_1	
		•
	5 local_milli_t1.reg_n.lat_0/a	F C3+R 2675 -1366 103 92 3 cl_invvn 07c SRL
	51 NET1056	F C3- 160 60 238 14 cl_invvn 07c
	Setup local_milli_t1.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
	>{a} BOX789/y	F C3+R 2675 -1366 103 92 3 cs_nnd3z 07c NAND
	0 NET1056	
	> BOX789/b	R C3+R 2620 -1366 139 36 1 cs_nnd3z 07c NAND
	55 NET1054 >{b} BOX785/y	R C3+R 2620 -1366 139 36 1 cs_nnd2f 03c NAND
	0 NET1054	.,

> BOX785/a	F C3+R	2542 -1366	116	19 1 cs_nnd2f	03c NAND
78 N1866					
>{c} C2555/y	F C3+R	2542 -1366	116	19 1 cs_ao12n	03c AOI
0 N1866					
> C2555/b	R C3+R	2431 -1366	3912	1044 3 cs_ao12	n 03c AOI
110 iu_reset_op_c_t1&0					
>{d} C2393/y	R C3+R	2431 -1432	3912	1044 3 cs_nnd2	n 02c NAND
0 iu_reset_op_c_t1&0					
> C2393/a	F C3+R	473 -1432	78 1	37 3 cs_nnd2n	02c NAND
1958 gbfonet_6					•
> gbfocell_6/y	F C3+R	473 -1432	78 1	37 3 cs_invvn	09c NOT 0
gbfonet_6		**************************************	**	•	
> gbfocell_6/a	R C3+R	410 -1432	217	43 1 cs_invvn	09c NOT
64 N2031					
>{e} C2162/y	R C3+R	410 -1432	217	43 1 cs_nnd3n	02c NAND
0 N2031					
> C2162/b	F C3+R	303 -1432	57 4	19 3 cs_nnd3n	02c NAND
107 rcvry_reset_q		_			
> rcvry_reset.reg_n.lat_0/l2_out	<u>_n</u> F(	C3+R 303 ·	-1432	57 49 3 cl_ir	ovvn 07d SRL
0 rcvry_reset_q					
> rcvry_reset.reg_n.lat_0/c2	R C3	+ 160 N/	C 60	) 222 13 cl_invv	n 07d SRL
143 slow_mode.c2_1					
> slow_mode.clockblock/c2	RC	3+ 160 N	4/C (	60 222 13 cb_cl	k_32_1 LCB
0 slow_mode.c2_1				•	

	U SIOW_ITIOUE.C2_I							
	6 local_milli.reg_n.lat_0/a 51 NET1056	F C3+R	2675	-1366	103	92 3 cl_invvn	07c SRL	
	Setup local_milli.reg_n.lat_0/c1	F C3	- 160	) :	60 2	238 14 cl_invvn	07c 120	00
	310W_1110de.C1_2						to the second of the second	2.22.7
	>{a} BOX789/y 0 NET1056	F C3+H	26/5	-1366	103	92 3 cs_nnd3z	0/c NAND	
the stages	> BOX789/b 55 NET1054	R C3+R	2620	-1366	139	36 1 cs_nnd3z	07c NAND	
1.6 J	>{b} BOX785/y 0 NET1054	R C3+R	2620	-1366	139	36 1 cs_nnd2f	03c NAND	
	> BOX785/a 78 N1866	F C3+R	2542	-1366	116	19 1 cs_nnd2f	03c NAND	
	>{c} C2555/y 0 N1866	F C3+R	2542 -	1366	116	19 1 cs_ao12n	03c AOI	
	> C2555/b 110 iu_reset_op_c_t1&0	R C3+R	2431 -	1366	3912 1	044 3 cs_ao12n	03c AOI	
·	>{d} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2431 -	1432	3912	1044 3 cs_nnd2	n 02c NANE	)
		FC3+R	473 -1	432	78 13	7 3 cs_nnd2n	02c NAND	
	> gbfocell_6/y gbfonet_6	F C3+R	473 -1	432	78 13	37 3 cs_invvn (	9c NOT	0
	> gbfocell_6/a 64 N2031	R C3+R	410 -1	1432	217	43 1 cs_invvn (	09c NOT	
	>{e} C2162/y 0 N2031	R C3+R	410 -1	1432	217	43 1 cs_nnd3n	02c NAND	
	> C2162/b 107 rcvry_reset_q	F C3+R	303 -14	432	57 49	9 3 cs_nnd3n (	2c NAND	
	> rcvry_reset.reg_n.lat_0/l2_out_	_n FC	3+R	303 -1	432	57 49 3 cl_inv	vvn 07d SR	L

	0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 143 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
		070 4000 405 00 0 d invers 070 CDI
	7 local_milli_t2.reg_n.lat_0/a 5 NET1056	R C3+R 2591 -1236 165 92 3 cl_invvn 07c SRL
	Setup local_milli_t2.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
	>{a} BOX789/y 0 NET1056	R C3+R 2591 -1236 165 92 3 cs_nnd3z 07c.NAND
	> BOX789/a 80 N639	F C3+R 2511 -1236 107 32 1 cs_nnd3z 07c NAND
	>{b} C2466/y 0 N639	F C3+R 2511 -1236 107 32 1 cs_nnd2n 02c NAND
	> C2466/b	R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
	80 iu_reset_op_c_t1&0 >{c} C2393/y	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
	0 iu_reset_op_c_t1&0> C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
	<u> </u>	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
	<u>-</u>	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
	64 N2031 >{d} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
	0 N2031 > C2162/b	F C3+R _ 303 -1432 57 49 3 cs_nnd3n 02c NAND
	107 rcvry_reset_q > rcvry_reset.reg_n.lat_0/l2_out_	_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
	<b>,</b>	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
-	143 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	8 local_milli_t1.reg_n.lat_0/a 5 NET1056	R C3+R 2591 -1236 165 92 3 cl_invvn 07c SRL
•	Setup local_milli_t1.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
	>{a} BOX789/y 0 NET1056	R C3+R 2591 -1236 165 92 3 cs_nnd3z 07c NAND
	> BOX789/a 80 N639	F C3+R 2511 -1236 107 32 1 cs_nnd3z 07c NAND
	>{b} C2466/y 0 N639	F C3+R 2511 -1236 107 32 1 cs_nnd2n 02c NAND
	> C2466/b 80 iu_reset_op_c_t1&0	R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
	>{c} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
	> C2393/a 1958 gbfonet_6	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND

-

	> gbfocell_6/y	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
	gbfonet_6	D 00.D 440 4400 047 40.4
	> gbfocell_6/a 64 N2031	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
	>{d} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
	0 N2031	11 00+11 1410 -1402 217 45 1 C3_1110011 02C 14AND
	> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
	107 rcvry_reset_q	
	> rcvry_reset.reg_n.lat_0/l2_ou	ut_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
	0 rcvry_reset_q	
	> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	143 slow_mode.c2_1	D CO. 160 N/C 60 000 10 sh alls 00 1 1 CD
	> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	9 local_milli.reg_n.lat_0/a	R C3+R 2591 -1236 165 92 3 cl_invvn 07c SRL
	5 NET1056	
	Setup local_milli.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c 1200
	slow_mode.c1_2 >{a} BOX789/y	R C3+R 2591 -1236 165 92 3 cs_nnd3z 07c NAND
	0 NET1056	11 00+11 2091 -1200 100 92 0 CS_HHU0Z U/C NANU
	> BOX789/a	F C3+R 2511 -1236 107 32 1 cs_nnd3z 07c NAND
	80 N639	
	>{b} C2466/y	F C3+R 2511 -1236 107 32 1 cs_nnd2n 02c NAND
	0 N639	
Substitution of the substi	> C2466/b 80 iu_reset_op_c_t1&0	R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
	>{c} C2393/y	R C3+R _2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
	0 iu_reset_op_c_t1&0	
	> C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
	1958 gbfonet_6	
	> gbfocell_6/y	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
	gbfonet_6> gbfocell_6/a	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
	64 N2031	The state of the All to I to
	>{d} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
	0 N2031	
	> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
	107 rcvry_reset_q	rt_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
	0 rcvry_reset_q	ıı_ıı ı⁻ ∪o+n
		R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	143 slow_mode.c2_1	the first of the control of the section of the sect
	> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	0 slow_mode.c2_1	·
	10 iu_reset_op_c_t1	F C3+R 2130 -1131 2719 1011 1 PO 0
	iu_reset_op_c_t1	7 3377 2100 1101 2713 1011 170
	RAT	999 0
	> BOX716/OUT	F C3+R 2130 -1131 2719 1011 1 IOPAD IOPAD
	0 iu_reset_op_c_t1	F 00 B 0400 4404 0= 10 10 10 10 10 10 10 10 10 10 10 10 10
	> BOX716/IN	F C3+R 2130 -1131 2719 1044 3 IOPAD IOPAD
	0 iu_reset_op_c_t1&0	

```
2130 -1131 2719 1044 3 cs_nnd2n 02c NAND
                                FC3+R
---->{a} C2393/y
0 iu reset_op_c_t1&0
                                                          137 3 cs_nnd2n 02c NAND
                                         451 -1131
                                                      118
                               RC3+R
----> C2393/a
1679 gbfonet_6
                                                           137 3 cs_invvn 09c NOT
                                                      118
                                        . 451 -1131
                               R C3+R
----> gbfocell_6/y
0 gbfonet_6
                                                           43 1 cs_invvn 09c NOT
                                                      158
                                FC3+R
                                          370 -1131
----> gbfocell_6/a
81 N2031
                                                            43 1 cs_nnd3n 02c NAND
                                FC3+R
                                          370 -1131
                                                      158
---->{b} C2162/y
0 N2031
                                                           49 3 cs_nnd3n 02c NAND
                                                      46
                               RC3+R
                                          290 -1131
----> C2162/b
81 rcvry_reset_q
                                                                  49 3 cl_invvn 07d SRL
                                                290 -1131
                                                             46
                                      RC3+R
----> rcvry reset.reg_n.lat_0/l2_out_n
0 rcvry_reset_q
                                                          60 222 13 cl_invvn 07d SRL
                                    R C3+
                                              160
                                                   N/C
----> rcvry_reset.reg_n.lat_0/c2
130 slow mode.c2_1
                                                           60 222 13 cb_clk_32_1 LCB
                                               160
                                                    N/C
                                     R C3+
----> slow_mode.clockblock/c2
0 slow_mode.c2_1
----------
         > measure
The model <IDCDSUC> has:
                           122
 Primary Inputs
                            ··73
 Primary Outputs
                            0
 Primary BIDIs
                        1142
 Signals
 919
                           1757
 Connections
                           83
 Master REG Bits = =
                             83
 Slave REG Bits
 Internal Area
                        4648
 External Area
                            0
 Gates/Connects =
                          0.523051
 Fanout Count
                           1757 ·
 Average Fanout =
                          1.538529
 Avg Tech Box Size =
                           5.057671
                            0.010912
 Tech Box Size Stddev =
                       0.000000
 Power
 ***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
                           767
 Real signals
                           544
 Real boxes
                            1382
 Real connections
                          2149
 Real LSTs
                         8.544118
  Real ICells/box
                          3.950368
  Real LSTs/box
                         1.409926
  Real nets/box
```

Power Level Function

AOI

AOI

AOI

03c

03c >

10c >

Int Ext Power Int Ext Power

0

0.000

0.000

0.000

42

8

12

0.000

0.000

0.000

0

0

6

4

12

Cell

Each

7

2

1

Type Cnt Boxname

cs\_ao22n03c

cs ao12n03c

cs\_ao12n10c

Total

Cell

```
1
       cs ao22n10c
                                10c
                                            AOI
                                                           0.000
                                                  18
                                                        0
                                                                   18
                                                                         0
                                                                           0.000
  1
       cs_ao12n04c
                                04c
                                            AOI
                                                   4
                                                       0
                                                           0.000
                                                                   4
                                                                        0
                                                                           0.000
 180
        BRKPT
                                        BRKPT
                                                   0
                                    >
                                                       0
                                                          0.000
                                                                   0
                                                                       0
                                                                          0.000
 195
        IOPAD
                                        IOPAD
                                                      0
                                                                      0
                                                  0
                                                         0.000
                                                                  0
                                   >
                                                                         0.000
 160
        cs nnd2n02c
                                 02c
                                                                     480
                                       >
                                            NAND
                                                      3
                                                             0.000
                                                                            0.000
  1
       cs nnd2n10c
                                10c
                                           NAND
                                      >
                                                     8
                                                         0
                                                            0.000
                                                                     8
                                                                         0.000
  3
       cs nnd2n12c
                                12c
                                      >
                                           NAND
                                                    12
                                                         0
                                                             0.000
                                                                     36
                                                                          0
                                                                              0.000
  21
       cs_nnd3n02c
                                 02c
                                            NAND
                                       >
                                                     4
                                                         0
                                                             0.000
                                                                     84
                                                                          0
                                                                              0.000
  4
       cs_nnd2n11c
                                11c
                                           NAND
                                                    11
                                                         0
                                                             0.000
                                                                     44
                                                                          0
                                      >
                                                                              0.000
  3
       cs_nnd2n03c
                                03c
                                           NAND
                                                     3
                                                         0
                                                            0.000
                                                                     9
                                                                         0
                                                                            0.000
  5
       cs_nnd4n03c
                                03c
                                           NAND
                                                    5
                                                         0
                                                            0.000
                                      >
                                                                    25
                                                                          0
                                                                             0.000
  6
       cs_nnd2n14c
                                14c
                                           NAND
                                                    19
                                                         0
                                                            -0.000
                                      >
                                                                    114
                                                                           0...0.000
  1
       cs_nnd3n07c
                                07c
                                           NAND
                                      >
                                                    6
                                                         0
                                                            0.000
                                                                     6
                                                                            0.000
                                                                         0
  2
       cs_nnd2n14e
                                14e
                                           NAND
                                                    19
                                                         0
                                      >
                                                             0.000
                                                                     38
                                                                          0.000
  1
       cs_nnd2n04c
                                04c
                                           NAND
                                      >
                                                    3
                                                         0
                                                            0.000
                                                                     3
                                                                         0
                                                                            0.000
  2
       cs nnd2n07c
                                07c
                                           NAND
                                                    4
                                                         0
                                      >
                                                            0.000
                                                                     8
                                                                         0
                                                                            0.000
  1
       cs nnd2n14b
                                14b
                                           NAND
                                                    20
                                      >
                                                         0
                                                             0.000
                                                                     20
                                                                          0
                                                                              0.000
  1
       cs nnd3n12b
                                12b
                                                    22
                                      >
                                           NAND
                                                         0
                                                             0.000
                                                                     22
                                                                          0
                                                                              0.000
  2
      cs nnd4n10c
                                10c
                                           NAND
                                                    20
                                      >
                                                         0
                                                             0.000
                                                                    40
                                                                          .0
                                                                             0.000
  2
       cs nnd2n08c
                                08c
                                           NAND
                                                    7
                                                         0
                                      >
                                                            0.000
                                                                    14
                                                                          0
                                                                             0.000
  2
      cs_nnd3n05c
                                05c
                                           NAND
                                                    6
                                                         0
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
  1
      cs_nnd2n05c
                                05c
                                           NAND
                                                    4
                                                         0
                                                            0.000
                                                                    4
                                                                         0
                                                                            0.000
      cs nnd3n10c
                                           NAND
                                10c
                                      >
                                                    12
                                                         0
                                                            0.000
                                                                    12
                                                                          0 - 0.000
  1
      cs_nnd2f03c
                               03c.
                                      >
                                           NAND
                                                    4
                                                        0
                                                           0.000
                                                                            0.000
                                                                    4
                                                                        0
  1
      cs_nnd3z07c
                               `07c
                                      >
                                           NAND
                                                    10
                                                         0
                                                            0.000
                                                                   10
                                                                          0.000
...2
      cs_nnd4v06c
                                06c
                                           NAND
                                                    8
                                                         0
                                                            0.000
                                                                   16
                                                                         0
                                                                            0.000...
... 10
       cs nor2n02c
                                02c > :
                                           NOR
                                                  . . 3
                                                        0
                                                           ..0.000
                                                                   30
                                                                         0.000
      cs nor3n03c
                               03c
                                           NOR
                                                   4
                                                       0
                                                           0.000
                                                                   4
                                                                        0 ..
                                                                           0.000
  1
      cs nor2n12c
                               12c
                                      >
                                           NOR
                                                  12
                                                        0
                                                          0.000
                                                                   12
                                                                         0
                                                                            0.000
  1
      cs_nor2n04c
                               04c
                                           NOR
                                     > -
                                                   3
                                                       0
                                                           0.000
                                                                   3
                                                                        0
                                                                           0.000
  1
      cs_nor3n10e
                               10e >
                                           NOR
                                                   16
                                                           0.000
                                                        0
                                                                   16
                                                                            0.000
                                                                         0
- 1
      cs_nor2n11c -
                               11c
                                     >
                                           NOR
                                                  11
                                                       ...0
                                                           0.000 11
                                                                        0.000
 88
       cs invvn01c
                               01c
                                           NOT
                                                   2
                                     >
                                                       0
                                                           0.000
                                                                  176
                                                                         0
                                                                            0.000
  4
      cs_invvn11c
                               11c
                                     >
                                           NOT
                                                  6
                                                       0.000
                                                                  24
                                                                        0
                                                                           0.000
  6
      cs_invvn10c
                               10c
                                           NOT
                                     >
                                                  4
                                                          0.000
                                                       0
                                                                  24
                                                                        0 -
                                                                           0.000
- 21
       cs_invvn12c
                               12c
                                           NOT
                                                   6
                                     >
                                                       0
                                                          0.000
                                                                  126
                                                                         0
                                                                            0.000
  6
      cs_invvn09c
                               09c
                                           NOT
                                     >
                                                  4
                                                       0
                                                          0.000
                                                                  24
                                                                        0
                                                                           0.000
 22
       cs_invvn07c
                               07c
                                           NOT
                                                   2
                                     >
                                                       0
                                                          0.000
                                                                  44
                                                                        0.000
  4
      cs invvn15c
                               15c
                                           NOT
                                                  10
                                                       0
                                                          0.000
                                                                  40
                                     >
                                                                        0
                                                                           0.000
  8
      cs_invvn06c
                               06c
                                          NOT
                                                  2
                                     >
                                                       0
                                                          0.000
                                                                  16
                                                                        0
                                                                           0.000
 12
       cs_invvn05c
                                                   2
                                                          0.000
                               05c
                                           NOT
                                     >
                                                       0
                                                                  24
                                                                        0
                                                                           0.000
  6
      cs invvn13c
                                          NOT
                               13c
                                                  8
                                     >
                                                       0
                                                          0.000
                                                                  48
                                                                        0
                                                                           0.000
  1
      cs_invvv19b
                               19b
                                           NOT
                                                  28
                                     >
                                                       0
                                                          0.000
                                                                  28
                                                                        0
                                                                           0.000
  5
      cs_invvn08c
                                                          0.000
                               08c
                                     Š
                                          NOT
                                                  4
                                                       0
                                                                  20
                                                                          0.000
                                                                       0
  6
      cs invvn02c
                               02c
                                     >
                                          NOT
                                                  2
                                                       0
                                                          0.000
                                                                  12
                                                                       0
                                                                           0.000
  3
      cs_invvn14c
                               14c
                                          NOT
                                                  8
                                     >
                                                       0
                                                          0.000
                                                                  24
                                                                       0
                                                                           0.000
  3
      cs_invvn04c
                               04c
                                          NOT
                                                  2
                                                          0.000
                                     >
                                                       0
                                                                  6
                                                                       0
                                                                          0.000
  1
      cs_invvn19c
                               19c
                                          NOT
                                                  25
                                                          0.000
                                     >
                                                       0
                                                                  25
                                                                        0
                                                                           0.000
  2
      cs_invvn16c
                                          NOT
                               16c
                                     >
                                                  14
                                                       0
                                                          0.000
                                                                  28
                                                                        0
                                                                           0.000
  1
      cs_invvn01e
                               01e
                                     >
                                          NOT
                                                  2
                                                       0
                                                          0.000
                                                                  2
                                                                       0
                                                                          0.000
  2
      cs_oa21n10c
                               10c
                                     >
                                           OAI
                                                  14
                                                       0
                                                          0.000
                                                                  28
                                                                        0
                                                                           0.000
  1
      cs_oa22n10c
                                10c
                                           OAL
                                                  18
                                                       0
                                     >
                                                          0.000
                                                                  18
                                                                           0.000
                                                                        0
 22
      cl_invvn07c
                               07c
                                          REG
                                                  25
                                                       0
                                                          0.000
                                     >
                                                                  550
                                                                        0
                                                                            0.000
 30
       cl_invvn07d
                               07d
                                     >
                                          REG
                                                  25
                                                       0
                                                           0.000
                                                                  750
                                                                         0
                                                                            0.000
 18
       cl nnd2n07c
                               07c
                                           REG
                                                  26
                                     >
                                                        0
                                                           0.000
                                                                  468
                                                                         0
                                                                            0.000
```

```
264
                                                               0.000
                          07c >
                                    REG
                                           33
                                                0
                                                  0.000
   cl_ao22n07c
8
                                    REG
                                          29
                                                0
                                                  0.000
                                                          58
                                                               0
                                                                  0.000
                          07c
2
   cl_nnd3n07c
                               >
                                          26
                                                  0.000
                                                         26
                                                               0
                                                                 0.000
                                    REG
                                               0
                          06c
   cl_nor2n06c
1
                                                          30
                                                               0
                                                                  0.000
                                           30
                                                  0.000
                          07c
                                    REG
                                                0
1
   cl_ao21n07c
                                                                  0.000
                                                   0.000
                                                          30
                                                               0
                                    ŖEG
                                           30
                                                0
                          07c
   cl_oa21n07c
1
                                                                    0.000
                                                     0.000
                                                               70
                                > SEQUENTIAL
                                                70
   cb_mode_block
                                                  0 0.000 480
                                                                  0.000
                              > SEQUENTIAL
                                             80
   cb_clk_32_1
6
                                                               0.000
                                                           8
                                     XNOR
                                             8
                                                 0.000
    cs_xbn2n01b
                           01b
1
                                                           8
                                                               0
                                                                 0.000
                                                   0.000
                                     XOR
                                            8
                                                0
                           01d
                                >
    cs_xbo2n01d
```

```
# of
Levels Output
 0
        1
        55
              50* plus *****
  1
 2
        1
  3
        8
  4
 10
         3
 11
         1
 12
         3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
       20 .
 2
     _ :1
 3
        5
 4
        3.
 5
        10
 7
        3
 9
        1
 10
         6
 12
         1
 14
         6
 15
         9
 16
         14
 17
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
       2
  0
  1
      940
            2
       97
  3
       42
  4
       17
  5
       7
  6
       11
  7
       3
 8
       3
 13
        3
 14
       16
 20
        1
[End of measure]
[measure]: Execution time was 0.6 seconds.
         > randsim q
>>]: randsim( q );
       > echo {inside loop}
inside loop
> measure
The model <IDCDSUC> has:
 Primary Inputs =
                          122
 Primary Outputs
                          73
 Primary BIDIs =
                           0 -
 Signals
                      1142
 Gate Count =
                      919
 Connections
                          1757
 Master REG Bits =
                        83
 Slave REG Bits
                            83
 Internal Area =
                         4648
 External Area
                           0
 Gates/Connects
                         0.523051
 Fanout Count
                          1757
 Average Fanout
                         1.538529
 Avg Tech Box Size =
                          5.057671
 Tech Box Size Stddev =
                           0.010912
Power
                     0.000000
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
 Real signals
                         767
Real boxes
                         544
Real connections
                           1382
Real LSTs
                         2149
Real ICells/box
                       8.544118
Real LSTs/box
                        3.950368
Real nets/box
                       1.409926
Cell
             Total
Each
              Cell
Type Cnt Boxname
                            Power Level Function
                                                 Int Ext Power Int Ext Power
```

```
0.000
                                                                   42
                                                                        0
                                                           0.000
                                           AOI
                                                   6
                                                       0
                               03c
                                      >
     cs_ao22n03c
7
                                                                   8
                                                                        0
                                                                           0.000
                                                           0.000
                                           AOI
                                                   4
                                                       0
     cs_ao12n03c
                               03c
                                     >
2
                                                           0.000
                                                                   12
                                                                         0
                                                                            0.000
                                                  12
                                                        0
                               10c
                                            AOI
                                     >
     cs ao12n10c
1
                                                                            0.000
                                                           0.000
                                                                   18
                                                                         0
                                            AOI
                                                  18
                                                        0
                               10c
                                      >
     cs_ao22n10c
1
                                                           0.000
                                                                   4
                                                                        0
                                                                           0.000
                                            AOI
                                                  4
                                                       0
                               04c
     cs_ao12n04c
1
                                                                           0.000
                                                                   0
                                                                        0
                                                  0
                                                       0
                                                          0.000
                                        BRKPT
                                   >
180
      BRKPT
                                                                       0
                                                                          0.000
                                       IOPAD
                                                 0
                                                      0
                                                         0.000
                                                                  0
      IOPAD
                                   >
195
                                                                            0.000
                                                     3
                                                              0.000
                                                                     480
                                            NAND
                                                          0
                                02c
                                       >
160
      cs_nnd2n02c
                                                            0.000
                                                                     8
                                                                          0
                                                                             0.000
                                                         0
                                           NAND
                                                    8
                                10c
                                      >
     cs nnd2n10c
1
                                                                           0
                                                                              0.000
                                                             0.000
                                                                     36
                                           NAND
                                                    12
                                                          0
                                12c
     cs_nnd2n12c
                                      >
3
                                                                           0
                                                                              0.000
                                                             0.000
                                                                     84
                                                     4
                                                          0
                                02c
                                            NAND
                                      >
21
      cs_nnd3n02c
                                                                              0.000
                                                                     44
                                                                           0
                                                    11
                                                          0
                                                             0.000
                                           NAND
                                11c
                                      >
     cs nnd2n11c
 4
                                                             0.000
                                                                     9
                                                                          0
                                                                             0.000
                                                    3
                                                         0
                                           NAND
                                03c
                                      >
     cs_nnd2n03c
 3
                                                                     25
                                                                          0
                                                                              0.000
                                                             0.000
                                                         0
                                03c
                                      >
                                           NAND
                                                     5
 5
     cs_nnd4n03c
                                                                            0
                                                                               0.000
                                                    19
                                                          0
                                                             0.000
                                                                     114
                                           NAND
                                14c
                                      >
     cs nnd2n14c
 6
                                                                             0.000
                                                                     6
                                                                          0
                                                         0
                                                             0.000
                                           NAND
                                                     6
                                07c
                                      >
     cs_nnd3n07c
 1
                                                                      38
                                                                           0
                                                                               0.000
                                                             0.000
                                           NAND
                                                    19
                                                          0
                                14e
                                      >
      cs_nnd2n14e
 2
                                                                             0.000
                                                                          0
                                           NAND
                                                     3
                                                         0 -
                                                             0.000
                                                                      3
     cs_nnd2n04c
                                04c
                                      >
 1
                                                                          0
                                                                              0.000
                                                     4
                                                         0
                                                             0.000
                                                                      8
                                           NAND
                                07c
                                      >
 2
      cs_nnd2n07c
                                                                           0
                                                                      20
                                                                               0.000
                                                          0
                                                             0.000
                                14b
                                      >
                                            NAND
                                                    20
 1
      cs_nnd2n14b
                                                                      22
                                                                               0.000
                                                          0
                                                              0.000
                                                                           0
                                12b
                                            NAND
                                                    22
                                      >
 1
      cs nnd3n12b
                                                          0
                                                             0.000
                                                                      40
                                                                           0
                                                                               0.000
                                           NAND
                                                    20
                                10c
                                      >
 2
      cs nnd4n10c
                                                                              0.000
                                                                     14
                                                         0
                                                             0.000
                                                                           0
                                           NAND
                                                     7.
                                08c
                                      >
 2
      cs nnd2n08c
                                                             0.000
                                                                     12
                                                                           0
                                                                              0.000
                                            NAND
                                                     6
                                                         0
     cs_nnd3n05c
                                05c
                                      >
 2
                                                             0.000
                                                                      4
                                                                          0.000
                                                     4
                                                         0
                                            NAND
                                05c
                                      >
      cs_nnd2n05c
 1
                                                            0.000
                                                                     12
                                                                           0
                                                                               0.000
                                                          0
                                            NAND
                                                    12
                                10c
                                      >
      cs nnd3n10c
 1
                                                                     4---0
                                                                             0.000
                                                         0
                                                            0.000
                                           NAND
                                                    4
      cs nnd2f03c
                                03c
                                      >
 1
                                                    10
                                                             0.000
                                                                      10
                                                                           0
                                                                               0.000
                                                          0
                                           NAND
      cs_nnd3z07c
                                07c
                                      >
 1
                                                                           Ó
                                                                              0.000 -
                                                             0.000
                                                                     16
                                                     8
                                                         0.
                                            NAND
                                06c
                                      >
 2
      cs_nnd4v06c
                                                                          0
                                                                              0.000
                                                                     30
                                                     3
                                                         0
                                                            0.000
                                            NOR
      cs_nor2n02c
                                02c
                                      >
 10
                                                                         0
                                                                     4
                                                                             0.000 .....
                                                        0
                                                            0.000
                                            NOR
                                                    .4.
                                03c
                                      .>
      cs_nor3n03c
 1
                                                                              0.000
                                                                     12
                                                                          0
                                                         0
                                                            0.000
                                                   12
                                12c
                                      >
                                            NOR
 1
      cs_nor2n12c
                                                                             0.000
                                                                         0
                                                    3
                                                        0
                                                            0.000
                                                                     3
                                04c
                                      >. -
                                            NOR
      cs_nor2n04c
 1
                                                                              0.000
                                                        . 0
                                                                           0
                                                    16
                                                             0.000
                                                                     16
                                10e
                                      >
                                            NOR
      cs_nor3n10e
 1
                                                                              0.000
                                                   11
                                                            0.000
                                                                     11
                                                                          0
                                11c
                                      >
                                            NOR
                                                        : 0
 1
      cs nor2n11c
                                                                              0.000
                                                    2
                                                        0
                                                            0.000
                                                                    176
                                                                          0
                                      >
                                            NOT
                                01c
      cs invvn01c
 88
                                                           0.000
                                                        0
                                                                    24
                                                                         0
                                                                             0.000
                                            NOT
                                                   6
                               11c
                                      >
      cs_invvn11c
 4
                                                           0.000
                                                                    24
                                                                         0
                                                                             0.000
                                            NOT
                                                   4
                                                        0
                               10c
                                      >
 6
      cs invvn10c
                                                                              0.000
                                                                    126
                                                                          0
                                            NOT
                                                    6
                                                        0
                                                            0.000
                                12c
                                      >
       cs invvn12c
 21
                                                           0.000
                                                                         0
                                                                             0.000
                                                   4
                                                        0
                                                                    24
                                            NOT
                               09c
                                      >
 6
      cs_invvn09c
                                                                    44
                                                                          0
                                                                             0.000
                                                    2
                                                        0
                                                            0.000
                                            NOT
                                07c
                                      >
 22
       cs_invvn07c
                                                                          0
                                                                             0.000
                                                         0
                                                            0.000
                                                                    40
                                            NOT
                                                   10
                                15c
                                      >
  4
      cs invvn15c
                                                        0
                                                           0.000
                                                                    16
                                                                          0
                                                                             0.000
                                                   2
                                            NOT
                               06c
                                      >
  8
      cs_invvn06c
                                                    2
                                                                    24
                                                                          0
                                                                             0.000
                                                        0
                                                            0.000
                                            NOT
                                05c
                                      >
 12
       cs_invvn05c
                                                                          0
                                                                             0.000
                                                        0
                                                            0.000
                                                                    48
                                                   8
                                13c
                                            NOT
  6
      cs invvn13c
                                      >
                                                                          0
                                                                             0.000
                                                         0
                                                            0.000
                                                                    28
                                                   28
                                19b
                                            NOT
      cs_invvv19b
                                      >
  1
                                                                             0.000
                                                                    20
                                                                          0
                                            NOT
                                                    4
                                                        0
                                                            0.000
                                08c
                                      >
  5
      cs_invvn08c
                                                                             0.000
                                                    2
                                                        0
                                                            0.000
                                                                    12
                                                                          0
                                            NOT
                                02c
                                      >
  6
      cs invvn02c
                                                            0.000
                                                                    24
                                                                          0
                                                                             0.000
                                                    8
                                                        0
                                14c
                                      >
                                            NOT
      cs invvn14c
  3
                                                                            0.000
                                                                    6
                                                                         0
                                                    2
                                                        0
                                                            0.000
                                04c
                                            NOT
      cs invvn04c
                                      >
  3
                                                            0.000
                                                                    25
                                                                          0
                                                                              0.000
                                                   25
                                                         0
                                            NOT
                                19c
                                      >
      cs_invvn19c
  1
                                                                    28
                                                                          0
                                                                             0.000
                                                            0.000
                                            NOT
                                                   14
                                                         0
                                16c
                                      >
  2
      cs invvn16c
                                                                     2
                                                                         0
                                                                             0.000
                                            NOT
                                                    2
                                                         0
                                                            0.000
                                01e
                                      >
  1
      cs_invvn01e
                                                                     28
                                                                          0
                                                                              0.000
                                                   14
                                                         0
                                                            0.000
                                             OAI
                                 10c
  2
      cs_oa21n10c
```

```
1
    cs oa22n10c
                           10c
                                      OAI
                                           18
                                                0
                                                   0.000
                                                          18
                                                               0.000
22
    cl invvn07c
                          07c
                                     REG
                                           25
                                                0
                                                   0.000
                                >
                                                          550
                                                                0
                                                                  0.000
30
    cl_invvn07d
                          07d
                                >
                                     REG
                                           25
                                                0
                                                   0.000
                                                          750
                                                                0
                                                                   0.000
18
    cl_nnd2n07c
                           07c
                                >
                                     REG
                                            26
                                                 0
                                                   0.000
                                                          468
                                                                 0.000
    cl_ao22n07c
8
                           07c
                                >
                                     REG
                                            33
                                                 0
                                                   0.000
                                                          264
                                                                0.000
2
    cl_nnd3n07c
                          07c
                                >
                                     REG
                                           29
                                                 0
                                                   0.000
                                                           58
                                                                0
                                                                   0.000
1
    cl_nor2n06c
                          06c
                                     REG
                                           26
                                                0.000
                                                          26
                                                               0
                                                                  0.000
1
    cl_ao21n07c
                          07c
                                     REG
                                           30
                                                   0.000
                                                           30
                                                 0
                                                                0
                                                                   0.000
    cl_oa21n07c
1
                          07c
                                     REG
                                            30
                                                 0.000
                                                           30
                                                                   0.000
                                                                0
    cb_mode_block
1
                                > SEQUENTIAL
                                                70
                                                     0.000
                                                                    0.000
                                                               70
    cb_clk_32_1
6
                              > SEQUENTIAL
                                              80
                                                   0 0.000 480
                                                                   0.000
    cs xbn2n01b
1
                           01b
                                     XNOR
                                              8
                                                 0.000
                                >
                                                            8
                                                                0.000
1
    cs_xbo2n01d
                           01d
                                      XOR
                                             8
                                                           8
                                >
                                                 0
                                                   0.000
                                                               0
                                                                  0.000
```

```
# of
Levels Output
 0
 1
       55
 2
        1
 3
        8
 4
        1
 10
        3
 11
        1
12
        3
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 0
        7
 2
       20
 3
        1
 4
        5
 5
        3
 6
       10
 7
        3
 9
        1
 10
        6
 12
        1
 14
        6
 15
        9
 16
        4
 17
        14
```

The Histogram Of Fanin vs. Box

```
18
 4
The Histogram Of Fanout vs. Net
   # of
Fanout Nets
       2
 0
            940
 1
            50* plus *********
 2
       97
  3
       42
  4
       17
  5
       7
  6
  7
       3
  8
 13
       16
 14
 20
        1
[End of measure]
[measure]: Execution time was 0.6 seconds.
       > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:00:19 1999
Part: IDCDSUC
Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                             Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                              Max. Endpoints: 3
 Sort Field: Slack
                      Abbreviation Comparison/Description
  Cause of Slack
                                   Slack due to a point downstream on path
                        SIkCont
  Slack Continuation
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                         RAT
  Required Arrival Time
                                        ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
  Asserted Required Arrival Time AssrtRAT
 TIME)
                                   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                         ClkGSet
  Clock Gating Setup
 ARRIVAL TIME + ADJUST )
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
  Clock Gating Hold
                        CIkGHId
 ARRIVAL TIME + ADJUST )
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
  Clock Tree Pulse Width
                          CIKTPW
 TRAILING EDGE)
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
  Setup
 ADJUST)
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                    Hold
  Hold
 ADJUST)
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                       EndOfC
  EndOfCycle
 ADJUST)
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                         CIkPW
  ClockPulseWidth
 TRAILING EDGE)
```

3

35

	ClockSeparation ARRIVAL TIME + ADJUS	
		Test (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
	CLOCK + ADJUST )	( *************************************
	Arrival Time Limiting	ATLimit Slack discontinuity due to failed test
	Num/	LimitedAT/ Delay/ Failed Test/
	Test PinName	E Phase AT Slack Slew CL FO Cell P Func T.Adj
	NetName	•
	1 dcd_succ_last_t1	R C3+R 2954 -1955 3847 1011 1 PO 0
	dcd_succ_last_t1	
	RAT	999 0
	> BOX714/OUT	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1 > BOX714/IN	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1&0	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
	> C167/y	R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	11 00 FTC 2334 - 1333 3047 1011 1 CS_IIIVVII 010 NO1
	> C167/a	F C3+R 1092 -1955 55 139 4 cs_invvn 01c NOT
	1862 N675	7 COM 1002 1000 00 100 100_MINITED TO THE TOTAL
	>{a} C2738/y	F C3+R 1092 -1955 55 139 4 cs_nnd2n 14b NAND
	0 N675	
	> C2738/a	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
	29 last_cycle	
	>{b} C2487/y -	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND
	0 last_cycle	and the second s
		F.C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
	29 N1587	F CO. D. 4004 4055 00 440 0
	> C1952/y N1587	F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
	> C1952/a	R_C3+R1024 -1955
	10 num_dcd_cyl&0(1)	11.00TIT 1024 -1300 00 019 1 CS_IIIVV 190 NO1
	> BOX679/OUT	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
The second of the second	0 num_dcd_cyl&0(1)	Community of the Commun
	> BOX679/IN	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
	num_dcd_cyl(1)	<b>.</b>
	> num_dcd_cyl(1)	R C3+R 1024 -1955 80 319 1 PI 0
	num_dcd_cyl(1)	
	O ded even lest ti	E CO. D
•	dcd_succ_last_t1	F C3+R 2644 -1645 2362 1011 1 PO 0
	RAT	999 0
	> BOX714/OUT	999 F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1	1 00411 2044 -1043 2302 1011 1 10FAD 10FAD
	> BOX714/IN	F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1&0	. com Lond Look for Horne
	> C167/y	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	
	> C167/a	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
	1436 N675	
	>{a} C2738/y	R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
	0 N675	

> C2738/b	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND					
56 N1692	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND					
>{b} C2725rwr/y	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND					
0 N1692 > C2725rwr/a	R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND					
56 N1479						
>{c} C2721rwr/y	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND					
0 N1479	= 00 D 004 4045 405 05 0 on nnd2n 12h NAND					
> C2721rwr/c	F C3+R 994 -1645 125 95 2 cs_nnd3n 12b NAND					
102 N1497	F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR					
>{d} C2709rwr/y 0 N1497	F CO+N 984 1040 120 00 2 00_101011 124 11211					
> C2709rwr/c	R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR					
96 N1781	and the second s					
>{e} C2885/y	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND					
0 N1781	= 00 D 005 4045 44 50 1 co npd4p 10c NAND					
> C2885/d	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND					
73 N1997 >{f} C2886/y	F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND					
>{t} C2886/y 0 N1997	1 COTIL 025 1040 11 00 102					
> C2886/a	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND					
23 on serialize&0	3 on serialize&0					
> BOX638/OUT	> BOX638/OUT R C3+R 802 -1645 80 124 2 IOPAD IOPAD					
0 op_serialize&0	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0					
t - t						
op_serialize	R C3+R 802 -1645 80 124 2 Pl 0					
op_serialize	A CONTRACT OF THE CONTRACT OF					
	R C3+R 2431 -1432 3912 1011 1 PO 0					
	D C2 D 2/21 -1/32 3012 1011 1 PO 0					
3 iu_reset_op_c_t1	N C3+N 2431 -1402 3312 1011 113					
lu_reset_op_c_t1	and the control of th					

	> BOX638/IN op_serialize	R C3+R	802 -1645 80 124 2 IOPAD	IOPAD 0
	> op_serialize	R C3+R	802 -1645 80 124 2 PI	0.
	op_serialize			
		· · · · · · · · · · · · · · · · · · ·		
	3 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R	2431 -1432 3912 1011 1 PO	0
:	RAT	999	0	·
	> BOX716/OUT	R C3+R	2431 -1432 3912 1011 1 IOPAI	D IOPAD
	0 iu_reset_op_c_t1> BOX716/IN	R C3+R	2431 -1432 3912 1044 3 IOPAD	IOPAD
-	0 iu_reset_op_c_t1&0 >{a} C2393/y	R C3+R	2431 -1432 3912 1044 3 cs_nnd2	n 02c NAND
	0 iu_reset_op_c_t1&0 > C2393/a	F C3+R	473 -1432 78 137 3 cs_nnd2n	02c NAND
	1958 gbfonet_6> gbfocell_6/y	F C3+R	473 -1432 78 137 3 cs_invvn (	09c NOT 0
	gbfonet_6 > gbfocell_6/a	R C3+R	410 -1432 217 43 1 cs_invvn	09c NOT-
	64 N2031 >{b} C2162/y	R C3+R	410 -1432 217 43 1 cs_nnd3n	02c NAND
	0 N2031 > C2162/b	F C3+R	303 -1432 57 49 3 cs_nnd3n (	02c NAND
	107 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_ou	ıt_n FC	C3+R 303 -1432 57 49 3 cl_in	vvn 07d SRL
	0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2	R C3	+ 160 N/C 60 222 13 cl_invv	n 07d SRL
	143 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1	RC	3+ 160 N/C 60 222 13 cb_cll	k_32_1 LCB

```
> reset critical slack limit
-1955.13 Avg: -188.47
resetting the current slack to -1955.1339
         > get_default_delay_synlimit
           > tc_parm OFFSET(0)
         > tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1), ...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0,000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: ============
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
         > hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
         > hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao...
         > hide -no_clear -cells { cs_buffe }
         > hide -no_clear -cells { cs_invvn cs_invvv }
         > hide -no_clear -cells { cs_nnd2f cs_nnd2g cs_nnd2n cs_nn...
         > hide -no_clear -cells { cs_nnd3f cs_nnd3g cs_nnd3h cs_nn...
         > hide -no_clear -cells { cs_nnd4n cs_nnd4v }
         > hide -no_clear -cells { cs_nor2f cs_nor2g cs_nor2n cs_no...
         > hide -no_clear -cells { cs_nor3f cs_nor3g cs_nor3h cs_no...
         > hide -no_clear -cells { cs_oa12f cs_oa12g cs_oa12n cs_oa...
         > hide -no_clear -cells { cs_oa21n cs_oa21v }
         > hide -no_clear -cells { cs_oa22n cs_oa22v }
         > hide -no_clear -cells { cs_xbn2n cs_xbn2v }
         > hide -no_clear -cells { cs_xbo2n cs_xbo2v }
         > find cell cs *
         > hide -no_clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f0...
         > find cell cs buffe*
         > hide -no_clear -cells {cs_buffe01a cs_buffe02a cs_buffe0...
         > hide -clear -cells { "cs_invvn" }
         > find cell cs_invvn*c
         > hide -clear -cells {cs_invvn01c cs_invvn02c cs_invvn03c ...
         > hide -clear -cells { "cs_nnd2n" }
         > find cell cs_nnd2n*c
         > hide -clear -cells {cs_nnd2n02c cs_nnd2n03c cs_nnd2n04c ...
         > hide -clear -cells { "cs_nnd3n" }
         > find cell cs_nnd3n*c
         > hide -clear -cells {cs_nnd3n02c cs_nnd3n03c cs_nnd3n04c ...
         > hide -clear -cells { "cs_nnd4n" }
         > find cell cs nnd4n*c
         > hide -clear -cells {cs_nnd4n03c cs_nnd4n04c cs_nnd4n05c ...
         > hide -clear -cells { "cs_nor2n" }
         > find cell cs_nor2n*c
         > hide -clear -cells {cs_nor2n02c cs_nor2n03c cs_nor2n04c ...
         > hide -clear -cells { "cs_nor3n" }
         > find cell cs_nor3n*c
         > hide -clear -cells {cs_nor3n03c cs_nor3n04c cs_nor3n05c ...
         > hide -clear -cells { "cs_ao12n" }
         > find cell cs_ao12n*c
         > hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
         > hide -clear -cells { "cs_ao21n" }
         > find cell cs_ao21n*c
```

```
> hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
         > hide -clear -cells { "cs_ao22n" }
         > find cell cs_ao22n*c
         > hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
         > hide -clear -cells { "cs_oa12n" }
         > find cell cs_oa12n*c
         > hide -clear -cells {cs_oa12n03c cs_oa12n04c cs_oa12n05c ...
         > hide -clear -cells { "cs_oa21n" }
         > find cell cs_oa21n*c
         > hide -clear -cells {cs_oa21n03c cs_oa21n04c cs_oa21n05c ...
         > hide -clear -cells { "cs_oa22n" }
         > find cell cs_oa22n*c
         > hide -clear -cells {cs_oa22n03c cs_oa22n04c cs_oa22n05c ...
         > hide -clear -cells { "cs_buffe" }
         > find cell cs_buffe*
         > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
         > hide -clear -cells { "cs_xbo2n" }
         > find cell cs xbo2n*c
         > hide -clear -cells {cs_xbo2n01c cs_xbo2n02c cs_xbo2n03c ...
         > hide -clear -cells { "cs_xbn2n" }
         > find cell cs_xbn2n*c
         > hide -clear -cells {cs_xbn2n01c cs_xbn2n02c cs_xbn2n03c ...
Binding: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/dll-rs6000/hier.dll
hier.dll version 4.1 (Apr 14 1999 17:21:46)
BooleDozer Hierarchical Timing Correction
         > scritflow {trestructure_tree( MAX_INPUTS( 16 ) MAX_DECOM...
[critflow]: Compiled on Mar 10 1999 at 07:07:06.
[critflow]: trestructure_tree( MAX_INPUTS( 16 ) MAX_DECOMPOSE( 4 ) SORT_PINS CHECK_INPUTS
MIN INPUTS(2))
[trestructure]: Thresholds: Inputs=2 Slack=-0.000
[trestructure]: MaxInputs=16 MaxDecompose=4 DoubleInverters=true
[trestructure]: SortPins=true ReduceArea=false
[trestructure]: CheckInputs=true PartialTrees=false
[trestructure]: IgnoreHideFlags=false TibOnly=false
[trestructure]: MatchEffort=2 DebugNet=none
[trestructure]: Compiled on Apr 13 1999 at 18:34:22.
[critflow]: Critical Slack = -1955.134
[padnet]: Compiled on Mar 10 1999 at 05:18:12.
[padnet]: Added 9 IOPADs.
>>1: nextbox( genmark() );
>>1: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
 [onein]: Execution time was 0.0 seconds.
 [BD-40600]: Removed 0 double inverters.
 [invrem]: Execution time was 0.0 seconds.
 [cleanup]: 0 boxes disconnected
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 24 signals, 14 usage boxes and 22 connections.
```

```
[unpadnet]: Compiled on Mar 10 1999 at 05:21:34.
[unpadnet]: Removed 9 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                        The model has 13 signals, 3 usage boxes and 11 connections.
[Hdecompose]: Inserted 11 pairs of double inverters.
[ET-0203]: Timing top level created for design: SINGLE_SINK_INFO, analysis mode: default.
[ET-0112]: Deleting timing for design: SINGLE_SINK_INFO, analysis mode:default, and below.
[Hdecompose]: Single Sink: Load=12.000 Delay=0.000
[Hdecompose]: Max Inputs: 4
[Hdecompose]: Stage Delay: AND=144.431 XOR=259.360
[cleanup]: 49 boxes disconnected
[sweep]: sweep deleted 38 signals and 5 usage boxes.
                        The model has 17 signals, 7 usage boxes and 15 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input num dcd q(1)
[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(0)
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 22 signals, 14 usage boxes and 20 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 4 boxes disconnected
[sweep]: sweep deleted 4 signals and 0 usage boxes.
                        The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 5 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 32 signals and 2 usage boxes.
                        The model has 13 signals, 5 usage boxes and 11 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input ireg_valid&0
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
>>]: nextbox( genmark() );
```

```
>>]: nextnet( geninv() );
>>1: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 20 signals, 12 usage boxes and 18 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 9 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 31 signals and 6 usage boxes.
                          The model has 18 signals, 10 usage boxes and 16 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input op_cmp_raw&0
[trestructure]: (W) Covering is invalid due to electrical violation at input frc_blk_1cyc_q
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 3 IOPADs.
 >>]: nextbox( genmark() );
>>]: nextnet( geninv() );
 >>]: nextbox( twoin() onein() invrem() );
 [BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
 [BD-40500]: Removed 0 noninverting buffers.
 [BD-40501]: Changed 0 gates to inverters.
 [onein]: Execution time was 0.0 seconds.
 [BD-40600]: Removed 0 double inverters.
 [invrem]: Execution time was 0.0 seconds.
 [cleanup]: 0 boxes disconnected
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 8 signals, 4 usage boxes and 6 connections.
 [unpadnet]: Removed 3 IOPADs.
 [cleanup]: 0 boxes disconnected
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 5 signals, 1 usage boxes and 3 connections.
 [Hdecompose]: Inserted 3 pairs of double inverters.
 [cleanup]: 7 boxes disconnected
 [sweep]: sweep deleted 6 signals and 0 usage boxes.
                          The model has 5 signals, 1 usage boxes and 3 connections.
 [ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
 [padnet]: Added 4 IOPADs.
```

```
>>]: nextbox( genmark() );
  >>]: nextnet( geninv() );
 >>]: nextbox( twoin() onein() invrem() );
 [BD-40550]: Removed 0 redundant pins.
 [twoin]: Execution time was 0.0 seconds.
 [BD-40500]: Removed 0 noninverting buffers.
  [BD-40501]: Changed 0 gates to inverters.
 [onein]: Execution time was 0.0 seconds.
 [BD-40600]: Removed 0 double inverters.
 [invrem]: Execution time was 0.0 seconds.
 [cleanup]: 0 boxes disconnected
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                                                  The model has 12 signals, 7 usage boxes and 10 connections.
 [unpadnet]: Removed 4 IOPADs.
 [cleanup]: 2 boxes disconnected
 [sweep]: sweep deleted 2 signals and 0 usage boxes.
                                                  The model has 6 signals, 1 usage boxes and 4 connections.
 [Hdecompose]: Inserted 4 pairs of double inverters.
 [cleanup]: 16 boxes disconnected
 [sweep]: sweep deleted 12 signals and 2 usage boxes.
                                                  The model has 8 signals, 3 usage boxes and 6 connections.
 [ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
 [padnet]: Added 14 IOPADs.
 >>]: nextbox( genmark() );
          and the second of the second o
 >>]: nextnet( geninv() );
 >>]: nextbox( twoin() onein() invrem() );
 [BD-40550]: Removed 0 redundant pins.
 [twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 3 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 9 signals and 6 usage boxes.
                                                 The model has 42 signals, 27 usage boxes and 40 connections.
[unpadnet]: Removed 14 IOPADs.
[cleanup]: 4 boxes disconnected
[sweep]: sweep deleted 4 signals and 0 usage boxes.
                                                 The model has 24 signals, 9 usage boxes and 22 connections.
[Hdecompose]: Inserted 20 pairs of double inverters.
[cleanup]: 92 boxes disconnected
[sweep]: sweep deleted 66 signals and 5 usage boxes.
                                                 The model has 28 signals, 13 usage boxes and 26 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input op_dsbl_before&0
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[trestructure]: Rebuilt 0 logic trees
```

```
[trestructure]: Execution time was 38.6 seconds.
           > sweep
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 1142 signals, 919 usage boxes and 1757 connections.
          > hide -clear -cells { "cs_invvn" }
          > find cell cs_invvn*
          > hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...
          > hide -clear -cells { "cs_nnd2n" }
          > find cell cs_nnd2n*
          > hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...
          > hide -clear -cells { "cs_nnd3n" }
          > find cell cs_nnd3n*
          > hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
          > hide -clear -cells { "cs_nnd4n" }
          > find cell cs_nnd4n*
          > hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
          > hide -clear -cells { "cs_nor2n" }
          > find cell cs nor2n*
          > hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
          > hide -clear -cells { "cs_nor3n" }
          > find cell cs nor3n'
          > hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
          > hide -clear -cells { "cs_ao12n" }
          > find cell cs_ao12n*
          > hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
          > hide -clear -cells { "cs_ao21n" }
          > find cell cs_ao21n*
          > hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
          > hide -clear -cells { "cs_ao22n" }
          > find cell cs ao22n*
           > hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
           > hide -clear -cells { "cs_oa12n" }
           > find cell cs oa12n*
           > hide -clear -cells {cs_oa12n03b cs_oa12n03c cs_oa12n03d ...
           > hide -clear -cells { "cs_oa21n" }
           > find cell cs_oa21n*
           > hide -clear -cells {cs_oa21n03b_cs_oa21n03c cs_oa21n03d ...
           > hide -clear -cells { "cs_oa22n" }
           > find cell cs_oa22n*
           > hide -clear -cells {cs_oa22n03b cs_oa22n03c cs_oa22n03d ...
           > hide -clear -cells { "cs_buffe" }
           > find cell cs buffe*
           > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
           > hide -clear -cells { "cs_xbo2n" }
           > find cell cs xbo2n'
           > hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
           > hide -clear -cells { "cs_xbn2n" }
           > find cell cs_xbn2n*
           > hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
            > hide -clear -cells { cs_ao12f }
             > find cell cs_ao12f*
             > hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
             > hide -clear -cells { cs_nnd2f cs_nnd2w }
             > find cell cs_nnd2f*
             > hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
```

```
> find cell cs_nnd2w*
      > hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
      > hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
      > find cell cs nnd3f*
      > hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
      > find cell cs nnd3h*
      > hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
      > find cell cs_nnd3w*
      > hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
      > find cell cs_nnd3y*
      > hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
      > hide -clear -cells { cs_nor2f cs_nor2w }
      > find cell cs_nor2f*
     > hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...
     > find cell cs_nor2w*
     > hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...
     > hide -clear -cells { cs_nor3f cs_nor3h }
     > find cell cs nor3f*
     > hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
     > find cell cs_nor3h*
     > hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
     > hide -clear -cells { cs_oa12f }
     > find cell cs_oa12f*
     > hide -clear -cells {cs_oa12f03b cs_oa12f03c cs_oa12f03d ...
     > hide -clear -cells { "cs_invvv" }
> find cell cs_invvv*
   > hide -clear -cells {cs_invvv01b cs_invvv01c cs_invvv01d ...
     > hide -clear -cells { cs_ao12v cs_ao12g }
> find cell cs_ao12v*
 > find cell cs_ao12v*
> hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
  > find cell cs_ao12g*
> hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
     > hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
     > find cell cs nnd2v*
     > hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
  > find cell cs_nnd2g*
> hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
     > find cell cs_nnd2x*
     > hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
     > hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
     > find cell cs_nnd3v*
     > hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
     > find cell cs_nnd3a*
     > hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
     > find cell cs nnd3i*
     > hide -clear -cells {cs_nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
     > find cell cs_nnd3x*
     > hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
     > find cell cs nnd3z*
     > hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
     > hide -clear -cells { cs_nnd4v }
     > find cell cs nnd4v*
     > hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
     > hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
     > find cell cs nor2v*
```

```
> hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
         > find cell cs_nor2g*
         > hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
         > find cell cs_nor2x*
         > hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
         > hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
         > find cell cs nor3v*
         > hide -clear -cells {cs_nor3v03b cs_nor3v03c cs_nor3v03d ...
         > find cell cs_nor3g*
         > hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...
         > find cell cs_nor3i*
         > hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
         > hide -clear -cells { cs_oa12v cs_oa12g }
         > find cell cs_oa12v*
         > hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
         > find cell cs_oa12g*
         > hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
       > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
       > critical tsteal(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,UP...
critical( tsteal(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, UP, NO_VIOLATIONS) );
maximum area for proto box IDCDSUC is 4648
[tsteal]: CMVC version 1.24 compiled on Apr 13 1999 at 18:28:20.
[tsteal]: setting SCORE option to ALL.
[tsteal]: setting RE_POWER option.
[tsteal]: setting FASTEST mode.
Itsteal: setting SORT_PINS option.
[tsteal]: setting UP option.
[tsteal]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tsteal]: tsteal applied 0 times
[tsteal]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > critical tpushl(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, NO...
critical(tpushl(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, NO_VIOLATIONS));
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tpushl]: CMVC version 1.16 Compiled on Apr 1 1999 at 05:20:40.
[tpushl]: setting SCORE option to ALL.
[tpushl]: setting RE_POWER option.
[tpushl]: setting FASTEST mode.
```

```
[tpushl]: setting SORT_PINS option.
 [tpushl]: setting NO_VIOLATIONS option.
 -1955.13 Avg: -188.47
 -1955.13 Avg: -188.47
 ArrayNum: 6 ArrayMax: 919
 [tpushl]: applied 0 times
 [BD-502000]: Called transforms 6 times and applied 0 of them.
         > critical tpushr(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO...
 critical( tpushr(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS) );
 -1955.13 Avg: -188.47
 maximum area for proto box IDCDSUC is 4648
 [tpushr]: CMVC version 1.17 compiled on Mar 31 1999 at 11:36:43.
 [tpushr]: setting SCORE option to ALL.
 [tpushr]: setting RE_POWER option.
 [tpushr]: setting FASTEST mode.
 [tpushr]: setting SORT_PINS option.
 [tpushr]: setting NO_VIOLATIONS option.
 -1955.13 Avg: -188.47
 -1955.13 Avg: -188.47
 ArrayNum: 6 ArrayMax: 919
 [tpushr]: applied 0 times
 [tpushr eval]: Execution time was 0.0 seconds.
 [tpushr exec]: Execution time was 0.0 seconds.
 [BD-502000]: Called transforms 6 times and applied 0 of them.
         > critical tpushb(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO...
critical( tpushb(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,NO_VIOLATIONS) );
maximum area for proto box IDCDSUC is 4648

[tpushbl: CMVC version 1.45]
-- 1955.13 Avg: -188.47
[tpushb]: cMVC version 1.15 compiled on Mar 31 1999 at 11:36:11.
[tpushb]: setting SCORE option to ALL.
[tpushb]: setting RE_POWER option.
[tpushb]: setting FASTEST mode.
[tpushb]: setting SORT_PINS option.
[tpushb]: setting SORT_PINS option.
[tpushb]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tpushb]: applied 0 times
[tpushb eval]: Execution time was 0.5 seconds.
[tpushb exec]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
         > critical {texpand(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_...
critical( texpand(SCORE(ALL),PUSH,RE_POWER,FASTEST,SORT_PINS,SIMILAR,
VIEW(TRULE_BASE_AUTOGEN),NO_VIOLATIONS));
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[texpand]: setting SCORE option to ALL.
[texpand]: setting PUSH option.
[texpand]: setting RE_POWER option.
[texpand]: setting FASTEST mode.
[texpand]: setting SORT PINS option.
[texpand]: setting SIMILAR option.
[texpand]: explicit VIEWs used.
[texpand]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
```

```
[texpand]: TRULE view TRULE_BASE_AUTOGEN was found.
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[texpand]: Execution time was 0.0 seconds.
IBD-502600]: 0 gates checked and 0 expanded.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > critical {texpand(SCORE(ALL), PUSH, COMPLEMENT, RE_POWER, FA...
critical( texpand(SCORE(ALL), PUSH, COMPLEMENT, RE_POWER, FASTEST, SORT_PINS, SIMILAR,
VIEW(TRULE_BASE_AUTOGEN),NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[texpand]: setting SCORE option to ALL.
[texpand]: setting PUSH option.
[texpand]: setting COMPLEMENT option.
[texpand]: setting RE_POWER option.
[texpand]: setting FASTEST mode.
[texpand]: setting SORT_PINS option.
[texpand]: setting SIMILAR option.
[texpand]: explicit VIEWs used.
[texpand]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
[texpand]: TRULE view TRULE_BASE_AUTOGEN was found.
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[texpand]: Execution time was 0.0 seconds.
IBD-5026001: 0 gates checked and 0 expanded.
[BD-502000]: Called transforms 6 times and applied 0 of them.
> critical texpao(SCORE(ALL), PUSH, RE_POWER, FASTEST, SORT_PI...
critical( texpao(SCORE(ALL), PUSH, RE_POWER, FASTEST, SORT_PINS, NO_VIOLATIONS) );
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[texpao]: CMVC version 1.9 compiled on Mar 31 1999 at 11:28:36.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[texpao]: applied 0 times
[texpao]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > critical {tbmove(SCORE(ALL),RE_POWER,FASTEST,SORT_PINS,M...
critical( tbmove(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, MULTIPLE_CRITICAL,
INVERTC, CLONE, NO_VIOLATIONS));
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tbmove]: CMVC version 1.28 compiled on Apr 13 1999 at 18:25:40.
[tbmove]: setting SCORE option to ALL.
[tbmove]: setting RE_POWER option.
[tbmove]: setting FASTEST mode.
[tbmove]: setting SORT_PINS option.
[tbmove]: setting MULTIPLE_CRITICAL option.
[tbmove]: setting INVERTC option.
 [tbmovel: setting CLONE option.
```

```
[tbmove]: setting NO_VIOLATIONS option.
 -1955.13 Avg: -188.47
 [tbmove]: WORST SLACK in this network: -1955.18
 -1955.13 Avg: -188.47
 ArrayNum: 6 ArrayMax: 919
 [tbmove_analysis]: working on box C167.
 [tbmove_match_qualify]: box is hidden
 [tbmove_match_pattern]: boxC is rejected.
 [tbmove_analysis]: working on box C1952.
[tbmove_match_qualify]: boxD def box not base type or complement
[tbmove_match_qualify]: boxD def box not base type or complement
[[tbmove]]: 1 sinks moved to clone TBMOVE.
[tbmove_match_qualify]: boxC def box not base type or complementary base type
[tbmove_match_pattern]: boxC is rejected.
[tbmove_analysis]: working on box C2487.
[tbmove_match_pattern]: critB array max increased to 64
[tbmove_match_pattern]: boxB has 1 input.
[tbmove_match_pattern]: critA array max increased to 64
[tbmove_match_pattern]: boxA is rejected.
[tbmove_analysis]: working on box C2738.
[tbmove_match_qualify]: box is hidden
[tbmove_match_qualify]: box is hidden
[[tbmove]]: 1 sinks moved to clone TBMOVE.
[tbmove_save_arrays]: save arrays box max increased to 256
[tbmove_save_arrays]: save arrays pin max increased to 256
[tbmove_analysis]: before transform.
 y:N675<3> = C2738:cs_nnd2n14b (a:last_cycle, b:N1692)
 v:N1692<4> = C2725rwr:cs_nnd2n14e (a:N1479, b:N1681)
 y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892, b:N1858, c:N1497)
[tbmove]: 1 boundary move
[tbmove_analysis]: after transform.
y:N1689<2> = C2742:cs_nnd3f02c (a:N1652, b:N1479&0, c:N675)
v:N648<1> = C2743:cs_nnd3f02c (a:N675, b:N1479&0, c:N1862)
v:N2086&0<7> = C2744:cs_nnd2f13c (a:N675, b:N1479&0)
y:N675&0<1> = TBMOVE:cs_nnd2n14b (a:last_cycle, b:N1692)
 y:N675<3> = C2738:cs_nnd2n14b (a:N1692&0, b:last_cycle)
y:N1692<3> = C2725rwr:cs_nnd2n14e (a:N1479, b:N1681)
y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892, b:N1858, c:N1497)
y:N1479&0<3> = TBMOVE799:cs_nnd4n06c (a:N1858, b:N1497, c:last_cycle
     d:N892)
y:N1692&0<1> = TBMOVE798:cs_invvn07c (a:N1681)
[tbmove_analysis]: original
slack=-1955.1339,new_total_slack=-1881.8721,old_slack=-1955.1339,new_slack=-382.4436
[tbmove_analysis]: transform_cost = 9999 transform_slack = -1955.1339 restore flag 1 violation 1
[tbmove_analysis]: before restore arrays.
[tbmove_analysis]: save_box_array[ 0 ]
v:N1689<2> = C2742:cs_nnd3f02c (a:N1652, b:-, c:N675)
[tbmove_analysis]: save_box_array[ 1 ]
y:N648<1> = C2743:cs_nnd3f02c (a:N675, b:-, c:N1862)
[tbmove_analysis]: save_box_array[ 2 ]
y:N2086&0<7> = C2744:cs_nnd2f13c (a:N675, b:N1479)
[tbmove_analysis]: save_box_array[3]
y:N675&0<1> = TBMOVE:cs_nnd2n14b (a:last_cycle, b:N1692)
[tbmove_analysis]: save_box_array[ 4 ]
y:N675<3> = C2738:cs_nnd2n14b (a:N1692, b:last_cycle)
```

```
[tbmove_analysis]: save_box_array[ 5 ]
v:N1692<4> = C2725rwr:cs_nnd2n14e (a:N1479, b:N1681)
[tbmove_analysis]: save_box_array[ 6 ]
y:N1479<3> = C2721rwr:cs_nnd3n12b (a:N892, b:N1858, c:N1497)
Unbinding usage[0] C2742 cs_nnd3f02c
Binding usage C2742 to cs_nnd2n02c
Unbinding usage[1] C2743 cs_nnd3f02c
Binding usage C2743 to cs_nnd2n02c
Unbinding usage[2] C2744 cs_nnd2f13c
Binding usage C2744 to cs_invvn13c
Unbinding usage[3] TBMOVE cs_nnd2n14b
Binding usage TBMOVE to cs_nnd2n14b
Unbinding usage[4] C2738 cs_nnd2n14b
Binding usage C2738 to cs_nnd2n14b
Unbinding usage[5] C2725rwr cs_nnd2n14e
Binding usage C2725rwr to cs_nnd2n14e
Unbinding usage[6] C2721rwr cs_nnd3n12b
Binding usage C2721rwr to cs_nnd3n12b
[tbmove_restore_arrays]: after deleting pins.
[tbmove_restore_arrays]: save_box_array[ 0 ]
v:N1689<2> = C2742:cs_nnd2n02c (a:N1652, b:N675)
[tbmove restore arrays]: save_box_array[ 1 ]
y:N648<1> = C2743:cs_nnd2n02c (a:N1862, b:N675)
[tbmove_restore_arrays]: save_box_array[ 2 ]
y:N2086&0<7> = C2744:cs_invvn13c (a:N675)
[tbmove_restore_arrays]: save_box_array[ 3 ]
y:N675&0<1> = TBMOVE:cs_nnd2n14b (a:last_cycle, b:N1692)
[tbmove_restore_arrays]: save_box_array[ 4 ]
-y:N675<3> = C2738:cs_nnd2n14b (a:last_cycle, b:N1692)
[tbmove restore arrays]: save_box_array[5]
y:N1692<4> = C2725rwr:cs_nnd2n14e (a:N1479, b:N1681)
[tbmove_restore_arrays]: save_box_array[ 6 ]
y:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892, b:N1858, c:N1497)
[tbmove_analysis]: after restoration.
y:N675<4> = C2738:cs_nnd2n14b (a:last_cycle, b:N1692)
y:N1692<3> = C2725rwr:cs_nnd2n14e (a:N1479, b:N1681)
v:N1479<2> = C2721rwr:cs_nnd3n12b (a:N892, b:N1858, c:N1497)
[tbmove]: C2738 <=
[tbmove]: slack = -1955.13
[tbmove]: slack = -1950.22
[tbmove_analysis]: slack = -382.44, old slack = -1955.13, cost = 35.
[tbmove_analysis]: working on box BOX679.
[tbmove_match_pattern]: boxC is rejected.
[tbmove_analysis]: working on box BOX714.
[tbmove_match_pattern]: boxC is rejected.
[tbmove]: tbmove applied 0 times
[tbmove eval]: Execution time was 0.6 seconds.
[tbmove exec]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > critical tsteal(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, DO...
critical(tsteal(SCORE(ALL), RE_POWER, FASTEST, SORT_PINS, DOWN, NO_VIOLATIONS));
-1955.13 Avg: -188.47
maximum area for proto box IDCDSUC is 4648
[tsteal]: setting SCORE option to ALL.
[tsteal]: setting RE_POWER option.
```

```
[tsteal]: setting FASTEST mode.
[tsteal]: setting SORT PINS option.
[tsteal]: setting DOWN option.
[tsteal]: setting NO VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
[tsteal]: tsteal applied 0 times
[tsteal]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > critical tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tnc...
critical( tswap(SCORE(ALL),ACTUAL,ORD2,NO_VIOLATIONS),tncube(SCORE(ALL),NO_VIOLATIONS)
-1955.13 Ava: -188.47
maximum area for proto box IDCDSUC is 4648
setting SCORE option to ALL.
setting ACTUAL option.
setting ORD2 option.
setting NO VIOLATIONS option.
[tncube]: CMVC version 1.11 compiled on Mar 31 1999 at 11:35:50.
[tncube]: setting SCORE option to ALL.
[tncube]: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.47
-1955.13 Avg: -188.47
ArrayNum: 6 ArrayMax: 919
-1955.13 Avg: -188.47
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[thcube]: Opins swapped in 0 chains of gates
[thcube]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
       > repower_paths FUZZY(0.02)
initial slack is -1955
after repower paths slack is -1955
        > repower_paths {FUZZY(0.02), SIMULTANEOUS REPOWER}
initial slack is -1955
after repower paths slack is -1955
        > critical {repower(SCORE(ALL),FASTEST,NO_VIOLATIONS), rep...
critical(repower(SCORE(ALL),FASTEST,NO_VIOLATIONS),
repower(SCORE(ALL), INC, NO_VIOLATIONS, REPOWER GROUP(BETA))):
-1955.13 Avg: -188.11
maximum area for proto box IDCDSUC is 4656
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.11
ArrayNum: 6 ArrayMax: 919
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
        > critical clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIO...
```

```
critical( clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS) );
-1955.13 Avg: -188.11
maximum area for proto box IDCDSUC is 4656
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
setting FASTEST mode.
setting NO_VIOLATIONS option.
-1955.13 Avg: -188.11
ArrayNum: 6 ArrayMax: 919
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
       > critical {onebuff(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATI...
critical( onebuff(SCORE(ALL), RE_POWER, FASTEST, NO_VIOLATIONS),
dinv(SCORE(ALL), RE_POWER, FASTEST, NO_VIOLATIONS));
-1955.13 Avg: -188.11
maximum area for proto box IDCDSUC is 4656
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting FASTEST mode.
[onebuff]: setting NO_VIOLATIONS option.
-1955.13 Avg. -188.11
setting SCORE option to ALL.
setting RE_POWER option.
setting FASTEST mode.
setting NO_VIOLATIONS option.
-1955.13 Avg: -188.11
-1955.13 Avg: -188.11
ArrayNum: 6 ArrayMax: 919
[onebuff]: was applied 0 times
[BD-500500]: Moved 0 sinks and removed 0 inverters.
[BD-502000]: Called transforms 12 times and applied 0 of them.
        > critical tcte(SCORE(ALL),RE_POWER,FASTEST,NO_VIOLATIONS)
critical( tcte(SCORE(ALL), RE_POWER, FASTEST, NO_VIOLATIONS) );
-1955.13 Avg: -188.11
maximum area for proto box IDCDSUC is 4656
-1955.13 Avg: -188.11
-1955.13 Avg: -188.11
ArrayNum: 6 ArrayMax: 919
[BD-502200]: Combined 0 gates.
[tcte]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > critical speedreg(RE_POWER),absrbreg()
critical( speedreg(RE_POWER),absrbreg() );
-1955.13 Avg: -188.11
maximum area for proto box IDCDSUC is 4656
[speedreg]: Compiled on Mar 31 1999 at 11:35:02.
[BD-500000]: absrbreg CMVC version 1.9 compiled on Apr 13 1999 at 18:19:51
-1955.13 Avg: -188.11
ArrayNum: 6 ArrayMax: 919
[speedreg]: 0 registers checked 0 changed
[BD-502800]: 0 registers checked 0 absorbed logic.
[absrbreg]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
```

```
> noncritical speedreg(RE_POWER),absrbreg()
[noncritical]: CMVC version 1.17 compiled on Mar 31 1999 at 11:26:31.
maximum area for proto box IDCDSUC is 4656
-1955.13 Avg: -188.11
[noncritical]: noncritical applied to boxes with slack > -0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -188.01
[speedreg]: 263 registers checked 28 changed
[BD-502800]: 0 registers checked 0 absorbed logic.
[absrbreq]: Execution time was 0.0 seconds.
          > hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
          > hide -no_clear -cells { cs_ao21n cs_ao21v cs_ao22n cs_ao...
          > hide -no_clear -cells { cs_buffe }
          > hide -no_clear -cells { cs_invvn cs_invvv }
          > hide -no_clear -cells { cs_nnd2f cs_nnd2g cs_nnd2n cs_nn...
          > hide -no_clear -cells { cs_nnd3f cs_nnd3g cs_nnd3h cs_nn...
         > hide -no_clear -cells { cs_nnd4n cs_nnd4v }
          > hide -no_clear -cells { cs_nor2f cs_nor2g cs_nor2n cs_no...
          > hide -no_clear -cells { cs_nor3f cs_nor3g cs_nor3h cs_no...
          > hide -no_clear -cells { cs_oa12f cs_oa12g cs_oa12n cs_oa...
          > hide -no_clear -cells { cs_oa21n cs_oa21v }
          > hide -no_clear -cells { cs_oa22n cs_oa22v }
          > hide -no_clear -cells { cs_xbn2n cs_xbn2v }
          > hide -no_clear -cells { cs_xbo2n cs_xbo2v }
          > find cell cs_*
         > hide -no_clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f0...
          > find cell cs buffe*
                                             ا و الماسي الماسية المستخدم الماسية المراجعة الماسية المستخدم الماسية المستخدم الماسية الماسية الماسية الماسية
          > hide -no_clear -cells {cs_buffe01a cs_buffe02a cs_buffe0...
         > hide -clear -cells { "cs_invvn" }
         > find cell cs_invvn*c
          > hide -clear -cells {cs_invvn01c cs_invvn02c cs_invvn03c ...
          > hide -clear_-cells { "cs_nnd2n" }
          > find cell cs_nnd2n*c
          > hide -clear -cells {cs_nnd2n02c cs_nnd2n03c cs_nnd2n04c ...
         > hide -clear -cells { "cs_nnd3n" }
         > find cell cs nnd3n*c
          > hide -clear -cells {cs_nnd3n02c cs_nnd3n03c cs_nnd3n04c ...
          > hide -clear -cells { "cs nnd4n" }
          > find cell cs nnd4n*c
         > hide -clear -cells {cs_nnd4n03c cs_nnd4n04c cs_nnd4n05c ...
         > hide -clear -cells { "cs_nor2n" }
         > find cell cs nor2n*c
         > hide -clear -cells {cs_nor2n02c cs_nor2n03c cs_nor2n04c ...
         > hide -clear -cells { "cs_nor3n" }
         > find cell cs nor3n*c
         > hide -clear -cells {cs_nor3n03c cs_nor3n04c cs_nor3n05c ...
         > hide -clear -cells { "cs_ao12n" }
         > find cell cs ao12n*c
         > hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
         > hide -clear -cells { "cs ao21n" }
         > find cell cs_ao21n*c
         > hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
         > hide -clear -cells { "cs_ao22n" }
         > find cell cs_ao22n*c
```

```
> hide -clear -cells {cs ao22n03c cs_ao22n04c cs_ao22n05c ...
         > hide -clear -cells { "cs_oa12n" }
         > find cell cs_oa12n*c
         > hide -clear -cells {cs_oa12n03c cs_oa12n04c cs_oa12n05c ...
         > hide -clear -cells { "cs_oa21n" }
         > find cell cs oa21n*c
         > hide -clear -cells {cs_oa21n03c cs_oa21n04c cs_oa21n05c ...
         > hide -clear -cells { "cs_oa22n" }
         > find cell cs oa22n*c
         > hide -clear -cells {cs_oa22n03c cs_oa22n04c cs_oa22n05c ...
         > hide -clear -cells { "cs_buffe" }
         > find cell cs_buffe'
         > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
         > hide -clear -cells { "cs_xbo2n" }
         > find cell cs_xbo2n*c
         > hide -clear -cells {cs_xbo2n01c cs_xbo2n02c cs_xbo2n03c ...
         > hide -clear -cells { "cs_xbn2n" }
         > find cell cs_xbn2n*c
         > hide -clear -cells {cs_xbn2n01c cs_xbn2n02c cs_xbn2n03c ...
        > scritflow {trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMP...
[critflow]: trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS CHECK_INPUTS
MIN INPUTS(2))
[trestructure]: Thresholds: Inputs=2 Slack=-0.000
[trestructure]: MaxInputs=4 MaxDecompose=4 DoubleInverters=true
[trestructure]: SortPins=true ReduceArea=false
[trestructure]: CheckInputs=true PartialTrees=false
[trestructure]: IgnoreHideFlags=false TibOnly=false
[trestructure]: MatchEffort=2 DebugNet=none
[critflow]: Critical Slack = -1955.134
[padnet]: Added 9 IOPADs...
>>]: nextbox( genmark() );
>>1: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 24 signals, 14 usage boxes and 22 connections.
[unpadnet]: Removed 9 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 13 signals, 3 usage boxes and 11 connections.
[Hdecompose]: Inserted 11 pairs of double inverters.
[cleanup]: 49 boxes disconnected
[sweep]: sweep deleted 38 signals and 5 usage boxes.
                         The model has 17 signals, 7 usage boxes and 15 connections.
```

```
[trestructure]: (W) Covering is invalid due to electrical violation at input num dcd q(1)
[trestructure]: (W) Covering is invalid due to electrical violation at input num dcd q(0)
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 22 signals, 14 usage boxes and 20 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 4 boxes disconnected
[sweep]: sweep deleted 4 signals and 0 usage boxes.
           The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 5 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 32 signals and 2 usage boxes.
                         The model has 13 signals, 5 usage boxes and 11 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input ireg_valid&0
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 20 signals, 12 usage boxes and 18 connections.
[unpadnet]: Removed 7 IOPADs.
```

```
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                          The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 9 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]; sweep deleted 31 signals and 6 usage boxes.
                          The model has 18 signals, 10 usage boxes and 16 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input op_cmp_raw&0
[trestructure]: (W) Covering is invalid due to electrical violation at input frc_blk_1cyc_q
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 3 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>1: nextbox( twoin() onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 8 signals, 4 usage boxes and 6 connections.
[unpadnet]: Removed 3 IOPADs.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 5 signals, 1 usage boxes and 3 connections.
[Hdecompose]: Inserted 3 pairs of double inverters.
[cleanup]: 7 boxes disconnected
[sweep]: sweep deleted 6 signals and 0 usage boxes.
                          The model has 5 signals, 1 usage boxes and 3 connections.
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 4 IOPADs.
>>1: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
```

```
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 12 signals, 7 usage boxes and 10 connections.
[unpadnet]: Removed 4 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 6 signals, 1 usage boxes and 4 connections.
[Hdecompose]: Inserted 4 pairs of double inverters.
[cleanup]: 16 boxes disconnected
[sweep]: sweep deleted 12 signals and 2 usage boxes.
                         The model has 8 signals, 3 usage boxes and 6 connections.
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 9 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
using pattern information
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 2 signals and 2 usage boxes.
                         The model has 27 signals, 17 usage boxes and 25 connections.
[unpadnet]: Removed 9 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 16 signals, 6 usage boxes and 14 connections.
[Hdecompose]: Inserted 10 pairs of double inverters.
[cleanup]: 62 boxes disconnected
[sweep]: sweep deleted 42 signals and 8 usage boxes.
                         The model has 20 signals, 10 usage boxes and 18 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input op_dsbl_before&0
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[trestructure]: Rebuilt 0 logic trees
[trestructure]: Execution time was 31.8 seconds.
         > sweep
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1142 signals, 919 usage boxes and 1757 connections.
         > hide -clear -cells { "cs_invvn" }
         > find cell cs invvn*
         > hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...
         > hide -clear -cells { "cs_nnd2n" }
         > find cell cs nnd2n*
         > hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...
```

```
> hide -clear -cells { "cs_nnd3n" }
 > find cell cs_nnd3n*
 > hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
 > hide -clear -cells { "cs_nnd4n" }
 > find cell cs_nnd4n*
 > hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
 > hide -clear -cells { "cs_nor2n" }
 > find cell cs_nor2n*
 > hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
 > hide -clear -cells { "cs_nor3n" }
 > find cell cs nor3n3
 > hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ....
 > hide -clear -cells { "cs_ao12n" }
 > find cell cs_ao12n*
 > hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
 > hide -clear -cells { "cs_ao21n" }
 > find cell cs_ao21n*
 > hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
 > hide -clear -cells { "cs_ao22n" }
 > find cell cs_ao22n*
 > hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
 > hide -clear -cells { "cs_oa12n" }
 > find cell cs_oa12n*
 > hide -clear -cells {cs_oa12n03b cs_oa12n03c cs_oa12n03d ...
... > hide -clear -cells { "cs_oa21n" }
 > find cell cs_oa21n*
 > hide -clear -cells {cs_oa21n03b cs_oa21n03c cs_oa21n03d ...
 > hide -clear -cells { "cs_oa22n" }
> find cell cs_oa22n*
 > hide -clear -cells {cs_oa22n03b cs_oa22n03c cs_oa22n03d ...
 > hide -clear -cells { "cs buffe" }
 > find cell cs_buffe*
 > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
 > hide -clear -cells { "cs_xbo2n" }
 > find cell cs_xbo2n*
 > hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
 > hide -clear -cells { "cs_xbn2n" }
 > find cell cs_xbn2n*
 > hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
   > hide -clear -cells { cs_ao12f }
  > find cell cs_ao12f*
   > hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
   > hide -clear -cells { cs_nnd2f cs_nnd2w }
   > find cell cs_nnd2f*
   > hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
   > find cell cs_nnd2w*
   > hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
   > hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
   > find cell cs_nnd3f*
   > hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
   > find cell cs_nnd3h*
   > hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
   > find cell cs_nnd3w*
   > hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
   > find cell cs_nnd3y*
```

```
> hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
> hide -clear -cells { cs_nor2f cs_nor2w }
> find cell cs_nor2f*
```

- > hide -clear -cells {cs\_nor2f02b cs\_nor2f02c cs\_nor2f03b ...
- > find cell cs\_nor2w\*
- > hide -clear -cells {cs\_nor2w02b cs\_nor2w02c cs\_nor2w02d ...
- > hide -clear -cells { cs\_nor3f cs\_nor3h }
- > find cell cs\_nor3f\*
- > hide -clear -cells {cs\_nor3f03b cs\_nor3f03c cs\_nor3f03d ...
- > find cell cs\_nor3h\*
- > hide -clear -cells {cs\_nor3h03b cs\_nor3h03c cs\_nor3h03d ...
- > hide -clear -cells { cs\_oa12f }
- > find cell cs\_oa12f\*
- > hide -clear -cells {cs\_oa12f03b cs\_oa12f03c cs\_oa12f03d ...
- > hide -clear -cells { "cs\_invvv" }
- > find cell cs invvv\*
- > hide -clear -cells {cs\_invvv01b cs\_invvv01c cs\_invvv01d ...
- > hide -clear -cells { cs\_ao12v cs\_ao12g }
- > find cell cs\_ao12v\*
- > hide -clear -cells {cs\_ao12v03b cs\_ao12v03c cs\_ao12v03d ...
- > find cell cs\_ao12g\*
- > hide -clear -cells {cs\_ao12g03b cs\_ao12g03c cs\_ao12g03d ...
- > hide -clear -cells { cs\_nnd2v cs\_nnd2g cs\_nnd2x }
- > find cell cs\_nnd2v\*
- > hide -clear -cells {cs\_nnd2v02b cs\_nnd2v02c cs\_nnd2v02d ...
- > find cell cs\_nnd2g\*
- > hide -clear -cells {cs\_nnd2g02b cs\_nnd2g02c cs\_nnd2g02d ....
- > find cell\_cs\_nnd2x\*
- > hide -clear -cells {cs\_nnd2x02b cs\_nnd2x02c cs\_nnd2x02d ...
- > hide -clear -cells { cs\_nnd3v cs\_nnd3g cs\_nnd3i cs\_nnd3x...
- > find cell cs\_nnd3v\*
- > hide -clear -cells {cs\_nnd3v02b cs\_nnd3v02c cs\_nnd3v02d ...
- > find cell cs\_nnd3g\*
- > hide -clear -cells {cs\_nnd3g02b cs\_nnd3g02c cs\_nnd3g02d ...
- > find cell cs\_nnd3i\*
- > hide -clear -cells {cs\_nnd3i02b cs\_nnd3i02c cs\_nnd3i02d ...
- > find cell cs\_nnd3x\*
- > hide -clear -cells {cs\_nnd3x02b cs\_nnd3x02c cs\_nnd3x02d ...
- > find cell cs\_nnd3z\*
- > hide -clear -cells {cs\_nnd3z02b cs\_nnd3z02c cs\_nnd3z02d ...
- > hide -clear -cells { cs\_nnd4v }
- > find cell cs nnd4v\*
- > hide -clear -cells {cs\_nnd4v03b cs\_nnd4v03c cs\_nnd4v03d ...
- > hide -clear -cells { cs\_nor2v cs\_nor2g cs\_nor2x }
- > find cell cs\_nor2v\*
- > hide -clear -cells {cs\_nor2v02b cs\_nor2v02c cs\_nor2v02d ...
- > find cell cs nor2a\*
- > hide -clear -cells {cs\_nor2g02b cs\_nor2g02c cs\_nor2g03b ...
- > find cell cs\_nor2x\*
- > hide -clear -cells {cs\_nor2x02b cs\_nor2x02c cs\_nor2x02d ...
- > hide -clear -cells { cs\_nor3v cs\_nor3g cs\_nor3i }
- > find cell cs\_nor3v\*
- > hide -clear -cells {cs\_nor3v03b cs\_nor3v03c cs\_nor3v03d ...
- > find cell cs\_nor3q\*
- > hide -clear -cells {cs\_nor3g03b cs\_nor3g03c cs\_nor3g03d ...

```
> find cell cs nor3i*
         > hide -clear -cells {cs_nor3i03b cs_nor3i03c cs_nor3i03d ...
         > hide -clear -cells { cs_oa12v cs_oa12g }
         > find cell cs_oa12v*
         > hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
         > find cell cs_oa12g*
          > hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d ...
       > compare_critical_slack_limit
-1955.13 Avg: -188.01
comparing new slack -1955.1339 to saved slack -1935.5825
          > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
          > noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
repower: setting SCORE option to ALL.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -188.01
maximum area for proto box IDCDSUC is 4656
-1955.13 Avg: -188.01
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -181.26
[BD-500026]: repower was applied 73 times.
[repower]: Execution time was 5.7 seconds.
         > tc_parm MARGIN(10000000)
         > fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}
>>]: Itorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
setting ACTUAL option.
setting ONE_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.26
[BD-500300]: 16 pins on 7 gates swapped.
                          -1955.13 Avg: -181.16
[fanmatch]: Execution time was 3.6 seconds.
         > tc parm OFFSET(0)
         > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
         > tc_parm REGALL
         > repower_paths FUZZY(0.02)
initial slack is -1955
after repower paths slack is -1955
         > critical {repower(SCORE(ALL),FASTEST ,NO_VIOLATIONS)...
critical( repower(SCORE(ALL ), FASTEST , NO_VIOLATIONS),
repower(SCORE(ALL), FASTEST, NO_VIOLATIONS, REPOWER_GROUP(BETA)));
-1955.13 Avg: -181.15
maximum area for proto box IDCDSUC is 4655
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO_VIOLATIONS option.
```

```
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.15
ArrayNum: 6 ArrayMax: 919
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
         > compare_critical_slack_limit
-1955.13 Avg: -181.15
comparing new slack -1955.1339 to saved slack -1935.5825
       > measure
The model <IDCDSUC> has:
 Primary Inputs
                              122
 Primary Outputs
                               73
 Primary BIDIs
                               0
 Signals
                           1142
 Gate Count
                             919
 Connections
                             1757
 Master REG Bits
                               83
 Slave REG Bits
                               83
 Internal Area
                            4655
 External Area
                               0
 Gates/Connects
                            0.523051
 Fanout Count
                             1757
 Average Fanout
                            1.538529
 Avg Tech Box Size =
                             5.065288
 Tech Box Size Stddev =
                              0.010915
 Power
                        0.000000
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
 Real signals
                            767
 Real boxes
                             544
 Real connections
                              1382
Real LSTs
                            2149
Real ICells/box
                          8.556985
Real LSTs/box
                           3.950368
Real nets/box
                          1.409926
Cell
               Total
Each
                Cell
Type Cnt Boxname
                                Power Level Function
                                                        Int Ext Power
                                                                         Int
  6
      cs_ao22n03c
                                03c
                                      >
                                            AOI
                                                   6
                                                        0
                                                           0.000
                                                                   36
                                                                         0
                                                                            0.000
  2
      cs_ao12n03c
                                03c
                                            AOI
                                      >
                                                   4
                                                        0
                                                           0.000
                                                                    8
                                                                        0
                                                                            0.000
  1
      cs_ao12n10c
                                10c
                                            AOI
                                      >
                                                   12
                                                           0.000
                                                                   12
                                                                         0.000
  1
      cs_ao22n04c
                                04c
                                            AOI
                                      >
                                                   6
                                                        0
                                                           0.000
                                                                    6
                                                                        0
                                                                            0.000
  1
      cs_ao22n10c
                                10c
                                            AOI
                                                   18
                                      >
                                                        0
                                                           0.000
                                                                   18
                                                                         0.000
  1
      cs_ao12n05c
                                05c
                                            AOL
                                                   6
                                                       0
                                                           0.000
                                                                   6
                                                                        0
                                                                           0.000
180
       BRKPT
                                        BRKPT
                                                   0
                                    >
                                                       0
                                                          0.000
                                                                   0
                                                                        0
                                                                           0.000
       IOPAD
195
                                        IOPAD
                                                  0
                                                      0
                                   >
                                                          0.000
                                                                  0
                                                                       0
                                                                          0.000
144
       cs_nnd2n02c
                                 02c
                                            NAND
                                                      3
                                                          0
                                                             0.000
                                                                     432
                                                                               0.000
                                                                            0
 17
      cs_nnd2n04c
                                04c
                                       >
                                            NAND
                                                     3
                                                             0.000
                                                          0
                                                                     51
                                                                           0
                                                                              0.000
```

```
0.000
                                          NAND
                                                         0
                                                            0.000
                               10c
                                                    8
                                                                     8
    cs_nnd2n10c
                                     >
1
                                                   12
                                                                          0
                                                                              0.000
                                          NAND
                                                         0
                                                            0.000
                                                                     48
    cs nnd2n12c
                               12c
                                     >
4
                                                                     76
                                                                          0
                                                                              0.000
                               02c
                                           NAND
                                                    4
                                                         0
                                                            0.000
19
     cs_nnd3n02c
                                     >
                                                                             0.000
                                          NAND
                                                    3
                                                         0
                                                            0.000
                                                                     9
                                                                         0
                               03c
3
     cs nnd2n03c
                                     >
                                                    5
                                                         0
                                                            0.000
                                                                    25
                                                                          0
                                                                             0.000
                               03c
                                          NAND
5
    cs_nnd4n03c
                                     >
                                                    4
                                                            0.000
                                                                     8
                                                                         0
                                                                             0.000
                               03c
                                          NAND
                                                         0
2
     cs_nnd3n03c
                                     >
                                                                              0.000
                                          NAND
                                                   11
                                                         0
                                                            0.000
                                                                     33
                                                                          0
3
     cs nnd2n11c
                               11c
                                     >
                                          NAND
                                                   19
                                                         0
                                                             0.000
                                                                    114
                                                                           0
                                                                              0.000
                               14c
6
     cs_nnd2n14c
                                     >
                                                         0
                                                            0.000
                                                                     15
                                                                          0
                                                                              0.000
                                          NAND
                                                   15
                               13c
1
     cs_nnd2n13c
                                     >
                                                                         0
                                                                             0.000
                                                         0
                                                            0.000
                                                                     6
                               07c
                                          NAND
                                                    6
1
     cs nnd3n07c
                                     >
                                                   19
                                                         0
                                                            0.000
                                                                     38
                                                                           0.000
                               14e
                                           NAND
2
     cs nnd2n14e
                                     >
                                                                         0.000
                                                            0.000
                                                                     8
                                          NAND
                                                    4
                                                         0.
2
     cs nnd2n07c
                               07c
                                     >
                                                                     20
                                                                           0
                                                                              0.000
     cs_nnd2n14b
                               14b
                                     >
                                           NAND
                                                   20
                                                         0
                                                             0.000
1
                                                             0.000
                                                                     22
                                                                           0
                                                                              0.000
                               12b
                                           NAND
                                                   22
                                                         0
1
     cs_nnd3n12b
                                     >
                                                                          0
                                                                              0.000
                                          NAND
                                                   20
                                                         0
                                                             0.000
                                                                     40
2
     cs_nnd4n10c
                               10c
                                     >
                                          NAND
                                                    7
                                                         0
                                                            0.000
                                                                     7
                                                                         0
                                                                             0.000
1
     cs_nnd2n08c
                               08c
                                     >
                               05c
                                          NAND
                                                    6
                                                         0
                                                            0.000
                                                                    12
                                                                          0
                                                                             0.000
2
     cs_nnd3n05c
                                     >
                                                         0
                                                            0.000
                                                                     4
                                                                         0
                                                                             0.000
                               05c
                                          NAND
                                                    4
1
     cs nnd2n05c
                                     >
                                                         0
                                                             0.000
                                                                     12
                                                                           0
                                                                              0.000
                               10c--->
                                          NAND
                                                   12
1
     cs_nnd3n10c
                                                            0.000
                                                                    4
                                                                         0
                                                                            0.000
                                          NAND
                                                   4
                                                        0
                              03c
1
     cs_nnd2f03c
                                     >
                                                                     10
                                                                          0
                                                                              0.000
                                                   10
                                                         0
                                                            0.000
                               07c
                                          NAND
1
     cs_nnd3z07c
                                     >
                                                                          0
                                          NAND
                                                         0
                                                            0.000
                                                                    16
                                                                             0.000
2
                               06c
                                                    8
     cs nnd4v06c
                                     >
                                                           0.000
                                                                   24
                                                                         0
                                                                            0.000
                               02c
                                           NOR
                                                   3
                                                        0
8
     cs nor2n02c
                                     >
                                                                            0.000
                                                                        0
                                                        0
                                                           0.000
                                                                    9
                               04c
                                           NOR
                                                   3
3
     cs_nor2n04c
                                     >
                                                   4
                                                        0
                                                           0.000
                                                                    4
                                                                        0
                                                                            0.000
                              03c
                                           NOR
1
     cs_nor3n03c
                                     >
                                                                             0.000
                                                        0
                                                            0.000
                                                                    12
                                                                         0
                                          NOR
                                                   12
     cs nor2n12c
                               12c
                                                                    16
                                                                          0
                                                                             0.000
                                                   16
                                                      ---0
                                                            0.000
1
     cs_nor3n10e
                               10e
                                     >
                                           NOR
                                                                             0.000
                                           NOR
                                                  11
                                                        0
                                                            0.000
                                                                    11
                                                                          0
1
     cs_nor2n11c
                               11c
                                     >
                                                                             0.000
                                                   2
                                                           0.000
                                                                  120
                                                                         0
60
     cs_invvn01c
                               01c
                                     >
                                           NOT
                                                       0
                                                  6
                                                       0
                                                          0.000
                                                                   24
                                                                        0
                                                                            0.000
4
     cs invvn11c
                              11c
                                    .>
                                          NOT
                                          NOT
                                                       0
                                                          0:000
                                                                   28
                                                                        0
                                                                            0.000
7
     cs_invvn10c
                              10c
                                    >
                                                  4
                                                   6
                                                       0
                                                           0.000
                                                                   126
                                                                         0
                                                                             0.000
                               12c >
                                           NOT
21
     cs_invvn12c
                                                          0.000
                                                                   24
                                                                        0
                                                                            0.000
                              09c
                                    >
                                          NOT
                                                  4
                                                       0
6
     cs_invvn09c
                                                   2
                               .07c
                                     >
                                           NOT
                                                       0
                                                           0.000
                                                                   100
                                                                         0
                                                                             0.000
50
     cs invvn07c
                                                                            0.000
                                          NOT
                                                       0
                                                           0.000
                                                                   50
                                                                         0
                              15c .
                                                  10
5
     cs invvn15c
                                    >
                                                       0
                                                          0.000
                                                                   48
                                                                        0
                                                                            0.000
                              13c ...
                                          NOT
                                                  8
6
     cs_invvn13c
                                    >
                                          NOT
                                                  28
                                                        0
                                                           0.000
                                                                   28
                                                                         0
                                                                            0.000
                              19b.
     cs_invvv19b
                                    >
1
                                                  2
                                                       0
                                                          0.000
                                                                   12
                                                                        0
                                                                            0.000
                                          NOT
                              06c
6
     cs_invvn06c
                                    >
                                                                        0
                                                                            0.000
                                                  4
                                                       0
                                                          0.000
                                                                   16
                              08c
                                    >
                                          NOT
4
     cs invvn08c
                                          NOT
                                                  2
                                                       0
                                                          0.000
                                                                   10
                                                                        0
                                                                            0.000
5
     cs_invvn02c
                              02c
                                    >
                                                          0.000
                                                                   24
                                                                        0
                                                                            0.000
                              14c
                                    >
                                          NOT
                                                  8
                                                       0
3
     cs invvn14c
                                                   2
                                                                            0.000
                               04c
                                     >
                                           NOT
                                                       0
                                                           0.000
                                                                   20
                                                                         0
10
     cs_invvn04c
                                                  2
                                                           0.000
                                                                   16
                                                                        0
                                                                            0.000
                              05c
                                          NOT
                                                       0
     cs_invvn05c
8
                                    >
                                                          0.000
                                                                   25
                                                                         -0-
                                                                           -0.000
                                                  25
                                                        0.
                              19c
                                          NOT
1
     cs_invvn19c
                                    >
                                                                            0.000
                                                           0.000
                                                                   14
                                                                         0
                              16c
                                    >
                                          NOT
                                                  14
                                                        0
1
     cs invvn16c
                                                           0.000
                                                                   2
                                                                        0
                                                                           0.000
                                     >
                                          NOT
                                                   2
                                                       0
1
     cs invvn01e
                              01e
                                                                   28
                                                                         0
                                                                            0.000
                                                        0
                                                           0.000
2
     cs_oa21n10c
                               10c
                                     >
                                           OAI
                                                  14
                                                                            0.000
1
     cs_oa22n10c
                               10c
                                     >
                                           OAL
                                                  18
                                                        0
                                                           0.000
                                                                   18
                                                                         0
                                                                          0
                                                                             0.000
                              07d
                                           REG
                                                  25
                                                        0
                                                           0.000
                                                                   550
22
      cl_invvn07d
                                     >
                                                  25
                                                        0
                                                           0.000
                                                                   300
                                                                          0
                                                                             0.000
12
      cl invvn07c
                              07c
                                    >
                                          REG
                                           REG
                                                   26
                                                         0
                                                            0.000
                                                                    468
                                                                           0
                                                                              0.000
18
      cl_nnd2n07c
                               07c
                                     >
                                                           0.000
                                                                   25
                                                                         0
                                                                            0.000
                              05c
                                          REG
                                                 25
                                                       0
1
     cl invvn05c
                                    >
                                                  33
                                                            0.000
                                                                   264
                                                                          0
                                                                             0.000
                              07c
                                           REG
                                                        0
8
     cl_ao22n07c
                                     >
                                                                   350
                                                                          0
                                                                             0.000
                                          REG
                                                  25
                                                        0
                                                           0.000
                              06d
14
      cl invvn06d
                                     >
                                                                   25
                                                  25
                                                       0
                                                           0.000
                                                                         0
                                                                            0.000
                                          REG
     cl invvn05d
                              05d
                                    >
1
```

```
cl_nnd3n07c
                       07c >
                                 REG
                                      29
                                           0.000
                                                   58
                                                        0.000
   cl_nor2n06c
1
                       06c
                                REG
                                      26
                                           0.000
                                                    26
                                                        0.000
1
   cl_ao21n07c
                       07c
                                 REG
                                      30
                                           0.000
                                                   30
                                                        0.000
2
   cl_invvn06c
                      06c >
                                REG
                                      25
                                          0.000
                                                   50
                                                        0.000
   cl_oa21n07c
1
                       07c >
                                 REG
                                      30
                                           0 0.000 30
                                                        0.000
   cb_mode_block
1
                         A > SEQUENTIAL
                                           70
                                               0.000
                                                        70
                                                             0.000
6
   cb_clk_32_1
                           > SEQUENTIAL 80
                                             0 0.000 480
                                                           0.000
   cs_xbn2n01b
                       01b
1
                                 XNOR
                                        8
                                            0.000
                                                     8
                                                         0.000
1
   cs_xbo2n01d
                        01d
                                 XOR
                                       8
                                           0.000
                                                    8
                                                        0
                                                           0.000
```

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# O	f	
Levels	Outp	out
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 2
       20
 3
       1
 4.
       5
       3
       10
       3
 9
        1
 10
        6
 12
        1
 14
        6
15
        9
 16
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
       2
 0
             900* plus *
      940
 1
             50* plus *
 2
       97
 3
       42
 4
       17
 5
       7
 6
       11
 7
        3
 8
        3
        3
 13
        16
 14
 20
        1
[End of measure]
[measure]: Execution time was 0.6 seconds.
       > critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...
repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS), fantom(LIMITED), faninv(LIMITED));
-1955.13 Avg: -181.15
maximum-area for proto box IDCDSUC is 4655
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
setting INC mode.
setting NO VIOLATIONS option.
fantom: Found 152 valid buffers or inverters.
[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.
[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
-1955.13 Avg: -181.15
ArrayNum: 6 ArrayMax: 919
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.0 seconds.
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.0 seconds.
[BD-500700]: Added 0 buffers.
[fantom]: Execution time was 0.0 seconds.
[BD-500701]: Added 0 inverters.
[faninv]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 24 times and applied 0 of them.
       > nextbox synexpand(XPANDVIEW)
>>]: nextbox( synexpand(XPANDVIEW) );
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
```

```
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                      The model has 1142 signals, 919 usage boxes and 1757 connections.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names.
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
      > measure
The model <IDCDSUC> has:
 Primary Inputs
                            122
 Primary Outputs
                             73
 Primary BIDIs
                             0
 Signals
                         1142
 Gate Count
                           919
 Connections
                           1757
 Master REG Bits
                              83
 Slave REG Bits
                             83
 Internal Area
                          4655
 External Area
                             0
 Gates/Connects
                          0.523051
 Fanout Count
                           1757
 Average Fanout
                          1.538529
 Avg Tech Box Size
                           5.065288
 Tech Box Size Stddev =
                            0.010915
 Power = ___
                       0.000000
***R-E-A-L***S-T-A-T-I-S-T-I-C-S***
                           767
 Real signals
 Real boxes
                           544
 Real connections
                            1382
 Real LSTs
                          2149
 Real ICells/box
                         8.556985
 Real LSTs/box
                          3.950368
 Real nets/box
                         1.409926
 Cell
              Total
Each
               Cell
Type Cnt Boxname
                              Power Level Function
                                                        Ext Power
                                                     Int
                                                                     Int
      cs ao22n03c
                              03c
                                          IOA
                                                6
                                                     0
                                                      0.000
                                                               36
                                                                     0.000
 2
      cs_ao12n03c
                              03c
                                          AOI
                                                4
                                    >
                                                     0
                                                        0.000
                                                                8
                                                                    0
                                                                       0.000
 1
      cs_ao12n10c
                              10c
                                    >
                                          AOI
                                                12
                                                     0
                                                        0.000
                                                                12
                                                                     0.000
  1
      cs_ao22n04c
                              04ċ
                                    >
                                          AOI
                                                6
                                                     0.000
                                                                6
                                                                    0.000
 1
      cs_ao22n10c
                              10c
                                          AOI
                                                18
                                    >
                                                     0
                                                        0.000
                                                                18
                                                                     0.000
 1
      cs_ao12n05c
                              05c
                                          AOI
                                                6
                                                    0
                                                        0.000
                                                                6
                                                                    0
                                                                       0.000
 180
       BRKPT
                                      BRKPT
                                  >
                                                0
                                                    0
                                                       0.000
                                                               0
                                                                    0
                                                                       0.000
195
       IOPAD
                                      IOPAD
                                               0
                                                   0
                                                      0.000
                                                               0
                                                                   0
                                 >
                                                                      0.000
144
       cs_nnd2n02c
                               02c
                                          NAND
                                                   3
                                                          0.000
                                                                 432
                                                       0
                                                                        0.000
 17
      cs_nnd2n04c
                               04c
                                          NAND
                                                  3
                                                      0.000
                                                                 51
                                     >
                                                                       0.000
 1
      cs_nnd2n10c
                              10c
                                         NAND
                                                  8
                                                      0.000
                                    >
                                                                 8
                                                                      0.000
 4
      cs nnd2n12c
                              12c
                                    >
                                         NAND
                                                 12
                                                      0
                                                          0.000
                                                                 48
                                                                       0
                                                                          0.000
 19
      cs nnd3n02c
                               02c
                                         NAND
                                                  4
                                                      0
                                                          0.000
                                                                 76
                                    >
                                                                          0.000
                                                                       0
 3
      cs nnd2n03c
                              03c
                                         NAND
                                                         0.000
                                    >
                                                  3
                                                      0
                                                                 9
                                                                      0
                                                                         0.000
 5
      cs_nnd4n03c
                              03c
                                    >
                                         NAND
                                                  5
                                                      0
                                                         0.000
                                                                 25
                                                                      0.000
```

```
0.000
                                                           0.000
                                                                    8
                                                                        0
                                          NAND
                                                   4
                                                        0
                              03c
                                     >
    cs nnd3n03c
2
                                                                    33
                                                                          0
                                                                             0.000
                                                   11
                                                            0.000
                                          NAND
                                                        0
                               11c
                                     >
3
    cs_nnd2n11c
                                                                             0.000
                                                                          0
                                          NAND
                                                   19
                                                        0
                                                            0.000
                                                                    114
                               14c
6
    cs nnd2n14c
                                     >
                                                                          0
                                                                             0.000
                                                   15
                                                        0
                                                            0.000
                                                                    15
                                          NAND
                               13c
                                     >
    cs_nnd2n13c
1
                                                                            0.000
                                                                    6
                                                                         0
                                          NAND
                                                   6
                                                        0
                                                           0.000
                               07c
                                     >
1
    cs nnd3n07c
                                                                             0.000
                                                            0.000
                                                                    38
                                                                          0
                                                   19
                                                         0
                                          NAND
                               14e
                                     >
2
    cs_nnd2n14e
                                                                         0
                                                                            0.000
                                                        0
                                                           0.000
                                                                    8
                                          NAND
                                                   4
                               07c
                                     >
2
    cs nnd2n07c
                                                                             0.000
                                                   20
                                                         0
                                                            0.000
                                                                    20
                                                                          0
                                          NAND
                               14b
    cs nnd2n14b
                                     >
1
                                                         0
                                                            0.000
                                                                    22
                                                                          0
                                                                             0.000
                                                   22
                                          NAND
                               12b
                                     >
     cs nnd3n12b
1
                                                                    40
                                                                          0
                                                                             0.000
                                                            0.000
                                                         0
                                          NAND
                                                   20
                               10c
                                     >
2
     cs nnd4n10c
                                                                         0
                                                                            0.000
                                                            0.000
                                                                    7
                                          NAND
                                                   7
                                                        0
                               08c
                                     >
1
     cs_nnd2n08c
                                                                         0.000
                                                                    12
                                                           0.000
                                                        0
                               05c
                                          NAND
                                                   6
                                     >
2
     cs nnd3n05c
                                                                            0.000
                                                                         0
                                                                    4
                                          NAND
                                                   4
                                                        0
                                                            0.000
                               05c
     cs nnd2n05c
                                     >
1
                                                                          0
                                                            0.000
                                                                    12
                                                                             0.000
                                          NAND
                                                   12
                                                         0
                               10c
                                     >
     cs_nnd3n10c
1
                                                                            0.000
                                                                    4
                                                                        0
                                                   4
                                                        0
                                                           0.000
                              03c
                                    >
                                          NAND
     cs_nnd2f03c
1
                                                                             0.000
                                                         0
                                                            0.000
                                                                    10
                                                                          0
                               07c
                                     >
                                          NAND
                                                   10
     cs nnd3z07c
1
                                                   8
                                                        0
                                                           0.000
                                                                    16
                                                                             0.000
                                          NAND
     cs_nnd4v06c
                               06c
                                     >
2
                                                                   24
                                                   3
                                                       0
                                                           0.000
                                                                        0
                                                                            0.000
                                          NOR
                               02c
                                     >
8
     cs nor2n02c
                                                   3
                                                       0
                                                           0.000
                                                                   9
                                                                        0
                                                                           0.000
                                           NOR-
                               04c
3
     cs nor2n04c
                                     >
                                                       0
                                                           0.000
                                                                   4
                                                                        0
                                                                           0.000
                                                   4
                                           NOR
                               03c
                                     >
     cs_nor3n03c
1
                                                           0.000
                                                                   12
                                                                         0
                                                                            0.000
                                                  12
                                                        0
                                           NOR
                               12c
                                     >
1
     cs_nor2n12c
                                                                         0
                                                                             0.000
                                                        0
                                                           0.000
                                                                    16
                                           NOR
                                                  16
                                     >
     cs nor3n10e
                               10e
1
                                                                   11
                                                                         0
                                                                           -0.000
                                                        0
                                                           0.000
                                                  11
                                           NOR
                               11c
                                     >
"1"
     cs_nor2n11c ---
                                                                  120
                                                                         0
                                                                            0.000
                                                           0.000
                                                  2
                                                       0
                                           NOT
                               01c
                                     >
60
     cs_invvn01c
                                                                           0.000
                                                                  24
                                                                        0
                                                       0
                                                          0.000
                                          NOT
                                                  6
                              11c
                                    >
· 4
     cs invvn11c
                                                                  28
                                                                        0
                                                                           0.000
                                                  4
                                                       0
                                                          0.000
                              10c
                                    >
                                          NOT
7
     cs_invvn10c
                                                                            0.000
                                                                  126
                                                                         0
                                                       0
                                                          0.000
                                                   6
                               12c
                                           NOT
21
     cs_invvn12c
                                                                        0.000
                                                                  24
                                                  4
                                                          0.000
                              09c
                                    >
                                          NOT
     cs invvn09c
6
                                                           0.000
                                                                  100
                                                                            0.000
                                                   2
                                                       0
                               07c
                                     >
                                           NOT
     cs_invvn07c
50
                                                                   50
                                                                        0
                                                                            0.000
                                                       0
                                                           0.000
                               15c
                                    >
                                          NOT
                                                  10
     cs invvn15c
5
                                                                            0.000
                                                  8
                                                       0
                                                          0.000
                                                                  48
                                                                        0
                              13c
                                          NOT
                                     >
6
     cs invvn13c
                                                                            0.000
                                                  28
                                                       0.
                                                           0.000
                                                                   28
                                                                        .0
                                          NOT
                              19b
                                    >
     cs -invvv19b
1
                                                                  12
                                                                        0
                                                                            0.000
                                                  2
                                                          0.000
                                          NOT
                                                       0
                              06c
                                     >
6
     cs invvn06c
                                                                        0 .
                                                                           0.000
                                                                   16
                                          NOT
                                                  4
                                                       0
                                                          0.000
                              08c
                                     >
4
     cs invvn08c
                                                          0.000
                                                                   10
                                                                        0
                                                                            0.000
                                           NOT
                                                  2
                                                       0
                              02c
                                     >
5
     cs invvn02c
                                                                            0.000
                                                          0.000
                                                                   24
                                                                        0
                                                  8
                                                       0
                                           NOT
                              14c
                                     >
.3
     cs invvn14c ...
                                                                            0.000
                                                                   20
                                                                         0
                                                   2
                                                       0
                                                           0.000
                                           NOT
                               04c
      cs invvn04c
                                     >
10
                                                  2
                                                       0
                                                          0.000
                                                                   16
                                                                        0
                                                                            0.000
                                           NOT
     cs_invvn05c
                               05c
                                     >
 8
                                                                            0.000
                                                       0
                                                           0.000
                                                                   25
                                                                         0
                                                  25
                               19c
                                           NOT
                                     >
 1
     cs invvn19c
                                                                   14
                                                                         0
                                                                            0.000
                                           NOT
                                                  14
                                                        0
                                                           0.000
                               16c
                                     >
 1
     cs invvn16c
                                                           0.000
                                                                   2
                                                                        0
                                                                           0.000
                                                  2
                                                       0
                                           NOT
                               01e
                                     >
 1
     cs_invvn01e
                                                                   28
                                                                         0
                                                                            0.000
                                                           0.000
                                           OAL
                                                  14
                                                        0
                                10c
                                      >
 2
     cs_oa21n10c
                                                                            0.000
                                                  18
                                                        0
                                                           0.000
                                                                   18
                                                                         0
                                           OAI
                                10c
     cs oa22n10c
                                      >
 1
                                                  25
                                                        0
                                                           0.000
                                                                   550
                                                                         -.0
                                                                            - 0.000
                                           REG
22
      cl invvn07d
                               07d
                                     >
                                                           0.000
                                                                   300
                                                                          0
                                                                             0.000
                                                  25
                                                        0
                                           REG
                               07c
                                     >
12
      cl invvn07c
                                                                              0.000
                                                                    468
                                                                           0
                                                   26
                                                         0
                                                            0.000
                                           REG
                               07c
                                     >
      cl nnd2n07c
18
                                                                   25
                                                                        0
                                                                            0.000
                                                 25
                                                       0
                                                           0.000
                              05c
                                          REG
     cl_invvn05c
                                    >
 1
                                                                   264
                                                                          0
                                                                             0.000
                                                           0.000
                                                        0
                               07c
                                           REG
                                                  33
                                     >
 8
     cl_ao22n07c
                                                                   350
                                                                          0
                                                                             0.000
                                                        0
                                                           0.000
                                           REG
                                                  25
      cl_invvn06d
                               06d
14
                                     >
                                                                         0
                                                                            0.000
                                                        0
                                                           0.000
                                                                   25
                                                  25
                              05d
                                     >
                                           REG
      cl_invvn05d
 1
                                                                             0.000
                                                                    58
                                                                          0
                                           REG
                                                  29
                                                        0
                                                            0.000
                               07c
                                     >
 2
      cl_nnd3n07c
                                                        0
                                                           0.000
                                                                   26
                                                                         0
                                                                             0.000
                                           REG
                                                  26
                               06c
                                     >
 1
      cl_nor2n06c
                                                                             0.000
                                                   30
                                                        0
                                                            0.000
                                                                    30
                                                                          0
                                     >
                                           REG
                               07c
 1
      cl ao21n07c
                                                       0
                                                           0.000
                                                                   50
                                                                         0
                                                                            0.000
                                          REG
                                                  25
                              06c
 2
      cl invvn06c
                                    >
                                                        0
                                                            0.000
                                                                    30
                                                                          0
                                                                             0.000
                                                   30
                                           REG
                               07c
      cl oa21n07c
```

```
1
   cb_mode_block
                         A > SEQUENTIAL 70 0 0.000 70
                                                             0.000
6
   cb_clk_32_1
                           > SEQUENTIAL
                                        80
                                             0 0.000 480
                                                           0.000
1
   cs_xbn2n01b
                        01b
                                 XNOR
                                        8
                                            0.000
                                                     8
                                                         0.000
   cs_xbo2n01d
1
                        01d
                                 XOR
                                       8
                                                     8
                                           0.000
                                                        0
                                                           0.000
```

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of			
Levels	Out	put	
0	1	*	
1	55	50* plus *****	
2	1	*	
3	8	*****	
4	1	*	
10	3	***	
11	1	*	
12	3	***	
44.44			

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
 2:
      20
     1
 3
       3 ****
      10
       3
       1
 10
 12
      - 1
 14
 15
       9
 16
 17
       14
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
----- 0 2 **
```

```
940
             900* plus ****
 1
       97
 2
       42
 3
 4
       17
 5
       7
 6
       11
       3
 7
 8
       3
        3
 13
 14
        16
 20
        1
[End of measure]
[measure]: Execution time was 0.7 seconds.
      > repower_paths FUZZY(0.02)
initial slack is -1955
after repower paths slack is -1955
      > critical {repower(SCORE(ALL ),FASTEST ,NO_VIOLATIONS)...
critical( repower(SCORE(ALL ), FASTEST , NO_VIOLATIONS),
repower(SCORE(ALL),FASTEST,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1955.13 Avg: -181.15
maximum area for proto box IDCDSUC is 4655
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting FASTEST mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.15
ArrayNum: 6 ArrayMax: 919
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
       > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:03:06 1999
Part: IDCDSUC
                                       EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                    Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                                 Max. Endpoints: 3
Sort Field: Slack
                         Abbreviation Comparison/Description
 Cause of Slack
                                     Slack due to a point downstream on path
                          SlkCont
 Slack Continuation
                                     ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
                           RAT
                                          ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 Clock Gating Setup
                          ClkGSet
ARRIVAL TIME + ADJUST )
```

Clock Gating Hold ARRIVAL TIME + AD. Clock Tree Pulse Wi	JUST)
TRAILING EDGE) Setup	Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST ) Hold	Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST ) EndOfCycle	EndOfC ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST) ClockPulseWidth	CIkPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE) ClockSeparation	ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION > CLOCK2
ARRIVAL TIME + ADJ Loop	ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST ) Arrival Time Limiting	( CONTRACTOR TO THE PROPERTY OF THE PROPERTY O
	ender dissertandity due to failed test
Num/ Test PinName	LimitedAT/ Delay/ Failed Test/
NetName	E Phase AT Slack Slew CL FO Cell P Func T.Adj
***	
1 dcd_succ_last_t	1 R C3+R 2954 -1955 3847 1011 1 PO 0
dcd_succ_last_t1	
RAT	$^{\circ}$
> BOX714/OUT	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1	
> BOX714/IN	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&0	
> C167/y 0 dcd_succ_last_t1&0	R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
> C167/a	
1862 N675	F C3+R 1092 -1955 55 139 4 cs_invvn 01c NOT
>{a} C2738/y	F C3+R 1092 -1955 55 139 4 cs_nnd2n 14b NAND
0 N675	1002 1003 55 109 4 CS_IIIIUZII 14D NAND
> C2738/a-	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
29 last_cycle	TOO TOO THO PANED
>{b} C2487/y	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND
0 last_cycle	
> C2487/b	F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
29 N1587	F 00 B 4004 4005
> C1952/y N1587	F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
> C1952/a	
10 num_dcd_cyl&0(1)	R C3+R 1024 -1955 80 319 1 cs_invvv 19b NOT
> BOX679/OUT	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1)	TOTAL TODA OF STATE TOPAL
> BOX679/IN	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1)	
> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+R 1024 -1955 80 319 1 Pl 0

dcd_succ_last_t1 RAT > BOX714/OUT	999 0 F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0	F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
> C167/y 0 dcd_succ_last_t1&0	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
> C167/a 1436 N675	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
>{a} C2738/y 0 N675	R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
> C2738/b 56 N1692	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
0 N1692	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND
> C2725rwr/a 56 N1479	R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND
>{c} C2721rwr/y 0 N1479	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
C2721nur/c	F C3+R 994 -1645 125 95 2 cs nnd3n 12b NAND
102 N1497 >{d} C2709rwr/y 0 N1497	F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
> C2709rwr/c	H C3+H 898 -1045 137 66 2 CS_101311 106 NON
>{e} C2885/y	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
> C2885/d	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
73 N1997 >{f} C2886/y	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND  F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND  F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
> C2886/a	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
23 op_serialize&0> BOX638/OUT	R C3+R 802 -1645 80 124 2 IOPAD IOPAD
	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
op_serialize > op_serialize op_serialize	R C3+R 802 -1645 80 124 2 PI 0
3 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2431 -1432 3912 1011 1 PO 0
RAT > BOX716/OUT	999 R C3+R 2431 -1432 3912 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1> BOX716/IN	R C3+R 2431 -1432 3912 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0 >{a} C2393/y	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0> C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6> gbfocell_6/y gbfonet_6	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0

```
----> gbfocell 6/a
                            R C3+R
                                         410 -1432 217
                                                          43 1 cs invvn 09c NOT
64 N2031
---->{b} C2162/y
                               R C3+R
                                         410 -1432
                                                     217
                                                          43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b
                               F C3+R
                                        303 -1432
                                                    57
                                                         49 3 cs_nnd3n 02c NAND
107 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n
                                     FC3+R
                                               303 -1432
                                                           57 49 3 cl_invvn 07d SRL
0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2
                                   R C3+
                                            160
                                                  N/C
                                                        60 222 13 cl invvn 07d SRL
143 slow_mode.c2_1
----> slow_mode.clockblock/c2
                                    R C3+
                                             160
                                                   N/C
                                                         60 222 13 cb clk 32 1 LCB
0 slow_mode.c2_1
       > write_end_point_report -points 10
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:03:06 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                  EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38 Max. Slack: -1.13427E+38
Sort Field: Slack
                           Max. Endpoints: 10
Cause of Slack Abbreviation Comparison/Description
                 Slack Continuation SlkCont Slack due to a point downstream on path
Required Arrival Time
                                ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                       RAT
Asserted Required Arrival Time AssrtRAT
                                     ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
Clock Gating Setup
                       CIKGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
Clock Gating Hold
                      ClkGHld
                                 ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width
                        CIKTPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
Setup
                   Setup
                            ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST)
Hold
                  Hold
                           ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST)
EndOfCycle
                     EndOfC
                               ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST)
ClockPulseWidth
                      CIkPW
                                ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
ClockSeparation
                      ClkSep
                                ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
                  ALTest
                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
Arrival Time Limiting
                      ATLimit
                                Slack discontinuity due to failed test
 Num/
                               LimitedAT/
                                                                Delay/ Failed Test/
 Test PinName
                               E Phase
                                         AT Slack Slew CL FO Cell
                                                                       P Func T.Adi
NetName
```

loot #1	R C3+R 2954 -1955 3847 1011 1 PO 0
1 dcd_succ_last_t1 dcd_succ_last_t1	0 IODAD
RAT	999 R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
> BOX714/OUT	1055 0047 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1 > BOX714/IN	
0 dcd_succ_last_t1&0	R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
> C167/y 0 dcd_succ_last_t1&0	139 4 cs invvn 01c NOT
> C167/a	F COTTI 1002
1862 N675	F C3+11 100-
>{a} C2738/y 0 N675	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
> C2738/a	74 109 1 cs nnd2n 14e NAND
29 last_cycle >{b} C2487/y	H COTIL 1000
0 last_cycle	F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
> C2487/b 29 N1587	F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
> U1952/y	F COTIT TO THE STATE OF NOT
N1587	R C3+R 10241955 80 319 1 cs_invv 1951401
10 num_dcd_cyl&0(1)	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD IOPAD
> BOX679/OUT	10FAD 10PAD
() hum_dcd_cyico(:/-	D C3+H:1022
num_dcd_cyl(1)	R C3+R 1024 -1955 80 319 1 Pl 0
> num_dcd_cyl(1) num_dcd_cyl(1)	
nuni_ucc	F C21B 2644 -1645 2362 1011 1 PO 0
a ded succ last t1	F C3+R 2644 -1645 2362 1011 1 PO 0
dcd_succ_last_t1	999 I DOPAD IOPAD
RAT	F C3+R 2644 -1645 2362 1011 1161718
BOX714/OUT 0 dcd_succ_last_t1	F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
> BOX714/IN	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0 > C167/y	F C3+R 2644 -1645 2362 1011 1 35
0_dcd_succ_last_t1&0	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
> C167/a 1436 N675	100 4045 92 139 4 cs nnd2n 14b NAND
>{a} C2738/y	H COTIL 1200
0 N675 > C2738/b	F COAN TIVE
56 N1692	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND
>{b} C2725rwr/y	149 166 2 cs nnd2n 14e NAND
0 N1692 > C2725rwr/a	R COTI
56 N1479	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
>{c} C2721rwr/y 0 N1479	125 95 2 cs nnd3n 12b NAND
> C2721rwr/c	F C3+R 994 -1645 125 95 2 55_555
102 N1497	

(1)	
>{d} C2709rwr/y 0 N1497	F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
> C2709rwr/c 96 N1781	R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR
>{e} C2885/y 0 N1781	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
> C2885/d 73 N1997	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
>{f} C2886/y 0 N1997	F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
> C2886/a 23 op_serialize&0	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
O op_serialize&0	R C3+R 802 -1645 80 124 2 IOPAD IOPAD
> BOX638/IN op_serialize	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
> op_serialize op_serialize	R C3+R 802 -1645 80 124 0 B
3 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2431 -1432 3912 1011 1 PO 0
RAT	999
> BOX716/OUT	R C3+R 2431 -1432 - 2010 - 4044
> ROY716/IN	999 R C3+R 2431 -1432 3912 1011 1 IOPAD IOPAD
0 iu reset on c t180	R C3+R 2431 -1432 3912 1011 1 IOPAD IOPAD  R C3+R 2431 -1432 3912 1044 3 IOPAD IOPAD  R C3+R 2431 -1432 3912 1044 3 cs. nnd2n 020 NAND
>{a} C2393/y	D CO D TOTA S IOPAD IOPAD
0 iu_reset_op_c_t1&0 > C2393/a	OZC NAND
1958 gbfonet_6	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
gbfonet_6	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
64 N2031	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
>{b} C2162/y 0 N2031 > C2162/b	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
107 rcvry_reset a	F C3+R 303 -1432 57 49 3 cs nnd3n 020 NAND
> rcvry_reset.reg_n.lat_0/l2_ou 0 rcvry_reset_q	t_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
> rcvry_reset.reg_n.lat_0/c2 143 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 ch clk 23 1 1 05
51 NET1056	F C3+R 2675 -1366 103 92 3 cl_invvn 07c SRL
Setup local_milli_t2.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
>{a} BOX789/y 0 NET1056	F C3+R 2675 -1366 103 92 3 cs_nnd3z 07c NAND
> BOX789/b	B C3+B 2000 1000
55 NET1054	R C3+R 2620 -1366 139 36 1 cs_nnd3z 07c NAND

> BOX785/a		>{b} BOX785/y	R C3+R	2620 -1366	139 36 1 cs_nnd2f 03c NAND
>{c} C2555/y			F C3+R	2542 -1366	116 19 1 cs_nnd2f 03c NAND
> C2555/b R C3+R 2431 -1366 3912 1044 3 cs_ao12n 03c AOI 110 iu_reset_op_c_t1&0>(d) C2393/y R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND 0 iu_reset_op_c_t1&0> C2393/a F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND 1958 gbfonet_6> gbfocell_6/y F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0 gbfonet_6> gbfocell_6/a R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT 64 N2031>{e} C2162/y R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT 0 N2031> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND 107 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cs_invvn 07d SRL 143 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1			F C3+R	2542 -1366	116 19 1 cs_ao12n 03c AOI
>{d} C2393/y R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND 0 iu_reset_op_c_t1&0> C2393/a F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND 1958 gbfonet_6> gbfocell_6/y F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0 gbfonet_6> gbfocell_6/a R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT 64 N2031>{e} C2162/y R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND 107 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL 0 rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 143 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1			R C3+R	2431 -1366	3912 1044 3 cs_ao12n 03c AOI
> C2393/a			R C3+R	2431 -1432	3912 1044 3 cs_nnd2n 02c NAND
> gbfocell_6/y			F C3+R	473 -1432	78 137 3 cs_nnd2n 02c NAND
gbfonet_6> gbfocell_6/a R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT 64 N2031>{e} C2162/y R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND 107 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 143 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1			F C3+R	473 -1432	78 137 3 cs_invvn 09c NOT 0
64 N2031>{e} C2162/y R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND 107 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 143 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1		gbfonet_6	R C3+R		
0 N2031> C2162/b F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND 107 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 143 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	·	64 N2031			_
107 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_out_n		0 N2031			·
0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C _60 222 13 cl_invvn 07d SRL 143 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C _60_ 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1		107 rcvrv reset q			• .
143 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1		0 rcvry reset q		· · · · · ·	· ·
0 slow_mode.c2_1		143 slow_mode.c2_1			e gan a gama a a a a a a a a a a a a a a a a
	amount of the second		нс	3+ 100 F	W/O"*OU 222 13 CD_CIK_32_1, LCD

gragi kirkeraki u uzuma a a a	0 slow_mode.c2_1	•		
	***	en entreme .	<del>-</del> -	, , , , , , , , , , , , , , , , , , ,
The second secon	5 local_milli_t1.reg_n.lat_0/a 51 NET1056	F C3+1	R 2675 -136	66 103 92 3 cl_invvn 07c SRL
	Setup local_milli_t1.reg_n.lat_0/c1	F C	3- 160	60 238 14 cl_invvn 07c
	1200 slow_mode.c1_4 >{a} BOX789/y	F C3+R	26751366	103 92 3 cs_nnd3z 07c NAND
	0 NET1056 > BOX789/b	R C3+R	2620 -1366	139 36 1 cs_nnd3z 07c NAND
	55 NET1054 >{b} BOX785/y	R C3+R	2620 -1366	139 36 1 cs_nnd2f 03c NAND
	0 NET1054 > BOX785/a 78 N1866	F C3+R	2542 -1366	116 19 1 cs_nnd2f 03c NAND
	78 N1866 >{c} C2555/y 0 N1866	FC3+R	2542 -1366	116 19 1 cs_ao12n 03c AOI
	> C2555/b 110 iu_reset_op_c_t1&0	R C3+R	2431 -1366	3912 1044 3 cs_ao12n 03c AOI
	>{d} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2431 -1432	3912 1044 3 cs_nnd2n 02c NAND
	> C2393/a 1958 gbfonet_6	FC3+R	473 -1432	78 137 3 cs_nnd2n 02c NAND
	> gbforiet_0> gbfocell_6/y gbfonet_6	F C3+R	473 -1432	78 137 3 cs_invvn 09c NOT 0
	> gbfocell_6/a 64 N2031	R C3+R	410 -1432	217 43 1 cs_invvn 09c NOT
	>{e} C2162/y 0 N2031	R C3+R	410 -1432	217 43 1 cs_nnd3n 02c NAND
	> C2162/b	F C3+R	303 -1432	57 49 3 cs_nnd3n 02c NAND

	0 rcvry_reset_q > rcvry_reset.reg_n.lat_0/c2 143 slow_mode.c2_1	_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	0 slow_mode.c2_1	
	51 NET1056	F C3+R 2675 -1366 103 92 3 cl_invvn 07c SRL F C3- 160 60 238 14 cl_invvn 07c 1200
	slow_mode.c1_2	
	>{a} BOX/89/y 0 NET1056	F C3+R 2675 -1366 103 92 3 cs_nnd3z 07c NAND
	> BOX789/b 55 NET1054	R C3+R 2620 -1366 139 36 1 cs_nnd3z 07c NAND
	>{b} BOX785/y 0 NET1054	R C3+R 2620 -1366 139 36 1 cs_nnd2f 03c NAND
	> BOX785/a	F C3+R 2542 -1366 116 19 1 cs_nnd2f 03c NAND
v 1 *** *	78 N1866 >{c} C2555/y	F C3+R 2542 -1366 116 19 1 cs_ao12n 03c AOI
en en samen ge	0 N1866 > C2555/b	R C3+R 2431 -1366 3912 1044 3 cs_ao12n 03c AOI
	-110 iu_reset_op_c_t1&0	- R C3+R 2431 -1432 3912 1044 3 cs nnd2n 02c NAND
Photo 1	2UZ393/d	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
	1958 gbfonet_6 > gbfocell_6/y	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
	gbfonet_6 > gbfocell_6/a	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
	64 N2031 >{e} C2162/y 0 N2031	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
	> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
,	> rcvry_reset_reg_n.lat_0/l2_out_	_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
	0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 143 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	7 local_milli_t2.reg_n.lat_0/a 5 NET1056	R C3+R 2591 -1236 165 92 3 cl_invvn 07c SRL
	Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056	R C3+R 2591 -1236 165 92 3 cs_nnd3z 07c NAND
	> BOX789/a 80 N639	F C3+R 2511 -1236 107 32 1 cs_nnd3z 07c NAND
	>{b} C2466/y 0 N639	F C3+R 2511 -1236 107 32 1 cs_nnd2n 02c NAND

> C2466/b	R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
80 iu_reset_op_c_t1&0	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
>{c} C2393/y 0 iu_reset_op_c_t1&0	N C3+N 2431 - 1432 3912 1044 3 C3_1110211 02C 14/110
> C2393/a	F C3+R 473 -1432 78 137 3 cs_nnd2n 02c NAND
1958 gbfonet_6	
> gbfocell_6/y	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
gbfonet_6	
> gbfocell_6/a	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
64 N2031	The state of the s
>{d} C2162/y	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
0 N2031 > C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
> C2162/b 107 rcvry_reset_q	F C3+N 303 -1432 37 49 3 65_IIIIddii 026 IVAI4D
> rcvrv reset reg n lat 0/12 out	_n F C3+R 303 -1432 57 49 3 cl_invvn 07d SRL
0 rcvrv reset a	
> rcvry reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
1.40 alow mode of 1	·
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
9 local milli t1 reg n lat 0/a	R C3+R 2591 -1236 165 92 3 cl_invvn 07c SRL
5 NET1056	11 00+1(1) 255 ( ) 1200 ( ) 100
Setup local milli t1 reg n lat 0/c1	F C3- 160 60 238 14 cl_invvn 07c
1000	
>{a} BOX789/y	R C3+R - 2591 1236 - 165 92 3 cs_nnd3z 07c NAND
0 NET1056	F C3+R 2511 -1236 107 32 1 cs_nnd3z 07c NAND
	F C3+R 2511 -1236 107 -32 1 cs_nnd3z 07c NAND
80 N639	E.CO. D. 0511 1006 107 20 1 00 and 2n 020 NAND
∵>{b} C2466/y ○ N639	F.C3±R 2511 -1236 107::: 32 1:cs_nnd2n 02c NAND
> C2466/b	R C3+R 2431 -1236 3912 1044 3 cs_nnd2n 02c NAND
80 iu_reset_op_c_t1&0	THOUGHT Prof. (200 gold 197) o to_man.
>{c} C2393/y	R C3+R 2431 -1432 3912 1044 3 cs_nnd2n 02c NAND
0 iu reset op c t1&0	
> C2393/a	F C3+R 473 -1432 78137 3 cs_nnd2n 02c NAND
1958 gbfonet_6	
> gbfocell_6/y	F C3+R 473 -1432 78 137 3 cs_invvn 09c NOT 0
gbfonet_6	D 00 D 440 4400 047 40 4 as insure 000 NOT
> gbfocell_6/a	R C3+R 410 -1432 217 43 1 cs_invvn 09c NOT
64 N2031	R C3+R 410 -1432 217 43 1 cs_nnd3n 02c NAND
>{d} C2162/y 0 N203 <del>1</del>	N C3+N 410 1402 217 40 1 C3_1111d011 02014/110
> C2162/b	F C3+R 303 -1432 57 49 3 cs_nnd3n 02c NAND
107 rcvry_reset_q	7 00111 000 110 <u>1</u> 0, 10 0 00_1mas.
> rcvry_reset.reg_n.lat_0/l2_out	t n FC3+R 303 -1432 57 49 3 cl_invvn 07d SRL
0 rcvrv reset a	
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
143 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	

	5 NET1056						
	Setup local_milli.reg_n.lat_0/c1	FC3	160	60	238 14 cl_invvn	07c 1200	
	slow_mode.c1_2 >{a} BOX789/y	D CO. D	0504 4000	40-			
	0 NET1056	H C3+H	2591 -1236	165	92 3 cs_nnd3z	07c NAND	
	> BOX789/a	F C3+R	2511 -1226	107	32 1 cs_nnd3z	OZ- NAND	
	80 N639	7 00+11	2311 -1230	107	32 1 CS_111U32	U/C NAIND	
	>{b} C2466/y	FC3+R	2511 -1236	107	32 1 cs_nnd2n	02c NAND	
	0 N639				02 1 00_mu2n	02014/1/18	
	> C2466/b	R C3+R	2431 -1236	3912	1044 3 cs_nnd2n	02c NAND	
	80 iu_reset_op_c_t1&0						
	>{c} C2393/y	R C3+R	2431 -1432	3912	1044 3 cs_nnd2n	02c NAND	
	0 iu_reset_op_c_t1&0> C2393/a	F C3+R	470 4400	70 40	27.0		
	1958 gbfonet_6	r Co+n	4/3 -1432	78 13	37 3 cs_nnd2n 0	2C NAND	
	> gbfocell_6/y	FC3+R	473 -1432	78 13	37 3 cs_invvn 09	9c NOT 0	
	abfonet 6		170 1702	, ,	01 0 03_INVVII 03	SCINOT U	
	> gbfocell_6/a	R C3+R	410 -1432	217	43 1 cs_invvn 0	9c NOT	
	64 N2031	. 4			* · ·	•	
All the second s	>{d} C2162/y	R C3+R	410 -1432	217	43_1 cs_nnd3n	02c NAND	
	0 N2031	F CO. D					
	> C2162/b 107 rcvry_reset_q	FC3+R	303 -1432	.57 .4	9 3 cs_nnd3n _02	2c NAND	or per series of
the state of the s	> rcvry_reset.reg_n.lat_0/l2_out	n FC	3±B 303 -	1/32		un 07d CDI :	A A SACRET A SACRET
10 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0_rcvry_reset_q		01112	1402	. 37 . 49. 3.CI_IIIV	AIÍOLA SUL	And the state of the second
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	> rcvry_reset.reg_n.lat_0/c2	R C3 <sub>1</sub>	160 N/C	60	222 13 cl invvn	07d SRL	
A second	1/3 clow mode of 1				the second of th		-
a management	> slow_mode.clockblock/c2	R C	3+ 160 N	/C 6	0 222 13 cb_clk_	32_1 LCB	to the contract of the contrac
	0 slow_mode.c2_1	د بیروس سامه که دستندههمای	est me en	٠, .		e Kristiji ji sem makan si majerine	
	#Betake 1 take the court of						
The state of the s	10 iu_reset_op_c_t1	F C3+R	2130 -1131	2719	1011 1 PO	wing or o	and the second s
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*	RAT	999			0		4 - 44
	iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1	F C3+R	2130 -1131	2719	9 1011 1 IOPAD	IOPAD	
•	0 iu_reset_op_c_t1&0	F C3+H	2130 -1131	2719	1044 3 IOPAD	IOPAD	
	>{a} C2393/y	F C3+R	2130 -1131	2710 -	1044 3 cs_nnd2n	OOO NIAND	
	0 iu_reset_op_c_t1&0	. 50171		_, 13	TOTT U CO_IIIIUZII	OZU NAND	
	> C2393/a	R C3+R	451 -1131	118 13	37 3 cs_nnd2n (	D2c NAND	
	1679 gbfonet_6						
	> gbfocell_6/y	R C3+R	451 -1131	118 1	37 3 cs_invvn 0	9c NOT	
	0 gbfonet_6	F.00 F	070 445				
	> gbfocell_6/a 81 N2031	F C3+R	370 -1131	158 4	l3 1 cs_invvn 09	C NOT	
	>{b} C2162/y	F C3+R	370 -1131	158 4	12 1 00 00000 0	NO ALABID	
	0 N2031	, OUTIT	0/0 -1101	100 4	13 1 cs_nnd3n 0	IZC NAND	
	_	R C3+R	290 -1131	46 49	9 3 cs_nnd3n 02	C NAND	
	81 rcvry_reset_q			"			
	> rcvry_reset.reg_n.lat_0/l2_out_	n RC	3+R 290 -1	1131	46 49 3 cl_inv	n 07d SRL	
	0 rcvry_reset_q	_ = -					
	> rovry ropot roa m lot 0/-0	R C3+	160 N/C	^^	000 10 al imano	074 CDI	
	> rcvry_reset.reg_n.lat_0/c2	11 007	100 14/0	, 60	222 13 cl_invvn	U/a SHL	
	130 slow_mode.c2_1> slow_mode.clockblock/c2	R C3			222 13 cl_invvn ) 222 13 cb_clk_:		

## 0 slow\_mode.c2\_1 > measure The model <IDCDSUC> has: 122 Primary Inputs 73 **Primary Outputs Primary BIDIs** 0 1142 Signals 919 Gate Count 1757 Connections ... Master REG Bits 83 Slave REG Bits 83 4655 Internal Area External Area 0 0.523051 Gates/Connects **Fanout Count** 1757 Average Fanout 1.538529 Avg Tech Box Size = 5.065288 Tech Box Size Stddev = 0.010915 0.000000 Power \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\* 767 Real signals 544 Real boxes --1382----Real connections == 2149 Real LSTs 8.556985 Real ICells/box Real LSTs/box 3.950368 Real nets/box 1.409926 Cell Total T

Each		. Cell										
Гуре С	nt	Boxname	 Power	Level	Func	tion	Int	Ext	Power	Int	Ext	Power
6	CS_	_ao22n03c	 03c	>	AOI	6	0	0.000	36		0.000	
- 2	CS	_ao12n03c	 03c	>	AOI	4	0	0.000	8	0 0	.000	
1	CS	_ao12n10c	10c	>	AOI	12	0	0.000	12		0.000	
1	CS	_ao22n04c	04c	>	AOI	6	0	0.000	6		.000	
1	CS	_ao22n10c	10c	>	AOI	18	0	0.000	18		0.000	
1	CS.	_ao12n05c	05c	>	AOI	6	0	0.000	6		0.000	
180	В	RKPT	>	BR	KPT	0	0	0.000	-		.000	
195	10	OPAD	>	IOF	PAD .	0	0 (	0.000	0 0		000	
144	С	s_nnd2n02c	02c	>	NAN		-	0.0			0.00	
17	CS	_nnd2n04c	04c	>	NAN		•	0.00		0	0.000	)
1	CS	_nnd2n10c	10c	>	NAND		_			0	0.000	_
4	CS	_nnd2n12c	12c	>	NAND		2 (	0.00				
19	CS	_nnd3n02c	02c	>	NAN[	) 4	4 (	0.00		0		
3	CS	_nnd2n03c	03c	>	NAND					0	0.000	
5	CS	_nnd4n03c	03c	>	NAND	5				0	0.000	
2	CS	_nnd3n03c	03c	>	NAND	)· 4				0	0.000	
3	CS	_nnd2n11c	11c	>	NAND	1	1 (	0.00				
6	CS	_nnd2n14c	14c	>	NAND			0.00				
1	CS	_nnd2n13c	13c	>	NANE			0.00				
1	cs	_nnd3n07c	07c	>	NAND	) 6	6 (	0.00	0 6	0	0.000	

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The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# o	f	
Levels	Out	put
0	1	*
1	55	50* plus *****
2	1	*
3	8	*****
4	1	*
10	3	***
11	1	*
12	3	***

The Histogram Of Paths From Primary Inputs Or Registers To Registers

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
6
                  11
            8
                  3
           13
                  3
           14
                  16
           20
                   1
          [End of measure]
          [measure]: Execution time was 0.6 seconds.
                  > randsim q
          >>1: randsim( g ):
                  > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE OFF...
                  > noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
          repower: setting SCORE option to ALL.
          repower: setting LOWEST_NOT_EQUAL mode.
          repower: setting NO_VIOLATIONS option.
          -1955.13 Avg: -181.15
 maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.15
          -1955.13 Avg: -181.15
[noncritical]: noncritical applied to boxes with slack > 0.00
       [noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
[Indictitical], Number of Boxes processed is c.
-1955.13 Avg: -181.07

[BD-500026]: repower was applied 5 times.

[repower]: Execution time was 5.4 seconds.

> to_parm MARGIN(10000000)

> bufmatch ESTIMATED,TWO_LEVEL,NO_VIOLATIONS.
         | >>]: Itorbox( dbufmatch(ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
| [BD-500000]: bufmatch CMVC version 1.30 compiled on Apr 13 1999 at 18:22:32
                                    setting ESTIMATED option.
          setting TWO_LEVEL option.
          setting NO_VIOLATIONS option.
          -1955.13 Avg: -181.07
          [BD-500302]: 2 pins in 1 trees swapped, 9 trees tried
          -1955.13 Avg: -181.05
          [bufmatch]: Execution time was 0.1 seconds.
                > fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}
          >>]: ltorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
          setting ACTUAL option.
          setting ONE_LEVEL option.
          setting NO_VIOLATIONS option.
          -1955.13 Avg: -181.05
          [BD-500300]: 2 pins on 1 gates swapped.
          -1955.13 Avg: -181.08
          [fanmatch]: Execution time was 3.6 seconds.
                   > get_default_delay_synlimit
                    > tc_parm OFFSET(0)
                  > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
          [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
          [tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
          [tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
```

```
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > quick tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
>>]: [quick]:( tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1955.13 Avg: -181.08
[tdual_correct]: CMVC version 1.8 compiled on Mar 31 1999 at 11:35:12.
[tdual_correct]: setting SCORE option to ALL.
[tdual_correct]: setting RE_POWER option.
[tdual_correct]: setting INC mode.
[tdual_correct]: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.08
Selected 398 critical boxes of 919 total.
[quick]: Number of boxes to process is 398.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -181.08
[tdual_correct]: applied 0 times
       > tc_parm OFFSET(0)
       > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > reset_critical_slack_limit
Avg: -181.08
the current slack to -1955.1339
-1955.13 Avg: -181.08
resetting the current slack to -1955.1339
         > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS));
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
setting SCORE option to ALL.
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.08
ArrayNum: 6 ArrayMax: 919
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
Itswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
         > tc_parm REGALL
         > repower_paths FUZZY(0.02)
initial slack is -1955
 after repower paths slack is -1955
         > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS), re...
 critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS),
 repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
 -1955.13 Avg: -181.08
 maximum area for proto box IDCDSUC is 4655
 repower: setting SCORE option to ALL.
 repower: setting INC mode.
```

```
repower: setting NO VIOLATIONS option.
         repower: setting SCORE option to ALL.
         repower: setting INC mode.
         repower: setting NO_VIOLATIONS option.
         -1955.13 Avg: -181.08
        ArrayNum: 6 ArrayMax: 919
        [BD-500026]: repower was applied 0 times.
        [repower]: Execution time was 0.1 seconds.
        [BD-500026]: repower was applied 0 times.
        frepowerl: Execution time was 0.1 seconds.
        [BD-502000]: Called transforms 12 times and applied 0 of them.
                  > compare_critical_slack limit
        -1955.13 Avg: -181.08
        comparing new slack -1955.1339 to saved slack -1935.5825
               > write_end_point_report -points 3 -paths 1
        [ET-0018]: >Begin...New EndPoint Report
                for file /tmp/end_point_report..92476.
        [ET-0019]: <End.....New Endpoint Report.
        Sun Apr 18 22:03:36 1999
Part : IDCDSUC
Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
Max. Slack: 1.13427E+38
Sort Field: Slack
Max. Endpoints: 3
Cause of Slack
Abbreviation Comparison/Description
    Slack Continuation
                                  SlkCont Slack due to a point downstream on path
                                 RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
    Required Arrival Time
       Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
       TIME)
        Clock Gating Setup
                                  CIKGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
       ARRIVAL TIME + ADJUST )
         Clock Gating Hold
                                  ClkGHld
                                              ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
        ARRIVAL TIME + ADJUST )
         Clock Tree Pulse Width
                                    CIKTPW
                                                ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
        TRAILING EDGE)
         Setup
                                        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                             Setup
        ADJUST)
         Hold
                             Hold
                                       ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
        ADJUST )
         EndOfCycle
                                EndOfC
                                            ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
        ADJUST)
         ClockPulseWidth
                                  ClkPW
                                             ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
        TRAILING EDGE)
         ClockSeparation
                                 ClkSep
                                            ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
        ARRIVAL TIME + ADJUST )
                             ALTest
                                        ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
        CLOCK + ADJUST )
         Arrival Time Limiting
                                 ATLimit
                                            Slack discontinuity due to failed test
          Num/
                                            LimitedAT/
                                                                                 Delay/ Failed Test/
          Test PinName
                                            E Phase AT Slack Slew CL FO Cell
                                                                                         P Func T.Adi
        NetName
```

2954 -1955 3847 1011 1 PO R C3+R 1 dcd succ\_last\_t1 dcd\_succ\_last\_t1 999 RAT 2954 -1955 3847 1011 1 IOPAD **IOPAD** R C3+R ----> BOX714/OUT 0 dcd\_succ\_last\_t1 2954 -1955 3847 1011 1 IOPAD **IOPAD** RC3+R ---> BOX714/IN 0 dcd\_succ\_last\_t1&0 2954 -1955 3847 1011 1 cs\_invvn 01c NOT RC3+R ----> C167/y 0 dcd succ\_last\_t1&0 139 4 cs\_invvn 01c NOT 1092 -1955 55 FC3+R ----> C167/a 1862 N675 139 4 cs\_nnd2n 14b NAND FC3+R 1092 -1955 ---->{a} C2738/y 0 N675 71 108 1 cs\_nnd2n 14b NAND 1063 -1955 R C3+R ----> C2738/a 29 last\_cycle 108 1 cs\_nnd2n 14e NAND 1063 -1955 7.1 R C3+R ---->{b} C2487/y 0 last\_cycle 140 3 cs\_nnd2n 14e NAND FC3+R 1034 - - 1955 ---> C2487/b 29 N1587 140 3 cs\_invvv 19b NOT 0 32 1034 -1955 FC3+R ----> C1952/y N1587 19b NOT 1024 -1955 80 319 1 cs\_invvv R C3+R ----> C1952/a 10 num\_dcd\_cyl&0(1) R C3+R 1024 -1955 80 319 1 IOPAD IOPAD ----> BOX679/OUT 0 num\_dcd\_cyl&0(1) R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0 ----> BOX679/IN num\_dcd\_cyl(1) 1024 -1955 80 319 1 Pl R C3+R ----> num\_dcd\_cyl(1) num\_dcd\_cyl(1) 2644 -1645 2362 1011 1 PO 0 F C3+R 2 dcd\_succ\_last\_t1 dcd succ last\_t1 999 . 0 RAT 2644 -1645 2362 1011 1 IOPAD IOPAD FC3+R ----> BOX714/OUT 0 dcd\_succ\_last\_t1 2644 -1645 2362 1011 1 IOPAD **IOPAD** FC3+R ----> BOX714/IN 0 dcd\_succ\_last\_t1&0 2644 -1645 2362 1011 1 cs\_invvn 01c NOT FC3+R ----> C167/y 0 dcd\_succ\_last\_t1&0 92 139 4 cs\_invvn 01c NOT 1208 -1645 R C3+R ----> C167/a 1436 N675 139 4 cs\_nnd2n 14b NAND RC3+R 1208 -1645 ---->{a} C2738/y 0 N675 76 159 3 cs\_nnd2n 14b NAND 1152 -1645 F C3+R ----> C2738/b 56 N1692 159 3 cs\_nnd2n 14e NAND 76 FC3+R 1152 -1645 ---->{b} C2725rwr/y 0 N1692 14e NAND 166 2 cs\_nnd2n 1097 -1645 148 R C3+R ----> C2725rwr/a 56 N1479 166 2 cs\_nnd3n 12b NAND 1097 -1645 148 R C3+R ---->{c} C2721rwr/y

FC3+R

994 -1645

125 95 2 cs\_nnd3n 12b NAND

0 N1479

----> C2721rwr/c 102 N1497

>{d} C2709rwr/y 0 N1497	FC3+R	994 -1645	125	95 2 cs_nor3r	10e NOR
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>{e} C2885/y	D CO. D	000 4045	40=		
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> C2885/d	E 00 - D	005 4045			
73 N1997	FC3+R	825 -1645	44 ;	50 1 cs_nnd4n	10c NAND
>{f} C2886/y	F C3+R	005 4045	4.4		
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> gbfocell_6/y	FC3+R	473 -1432	78 - 1	37 3 cs_invvn	09c NOT 0
1958 gbfonet_6> gbfocell_6/y gbfonet_6> gbfocell_6/a 64 N2031		The second of th			
> gbfocell_6/a	R C3+R	410 -1432	217	43 1 cs_invvn	09c NOT
>{b} C2162/y	R C3+R	410 -1432	217	43 1 cs_nnd3n	02c NAND
0 142001				*	
> C2162/b	F C3+R	303 -1432	57 4	9 3 cs_nnd3n	02c NAND
107 rcvry_reset_q					
> rcvry_reset.reg_n.lat_0/l2_out	_n FC	3+R 303 -	1432	57 49 3 cl_in	vvn 07d SRL
0 rcvry_reset_q	D 00	400 111			
> rcvry_reset.reg_n.lat_0/c2 143 slow_mode.c2_1	R C34	+ 160 N/C	60 ز	222 13 cl_invv	n 07d SRL
> slow_mode.clockblock/c2	D 00	400 11			
0 slow_mode.c2 1	R C	3+ 160 N	/C 6	0 222 13 cb_cll	k_32_1 LCB
					•
> nextbox chklegal					
[					
>>]: nextbox( chklegal );					
4					

<sup>&</sup>gt;>]: nextbox( chklegal );

<sup>[</sup>BD-40000]: chklegal CMVC version 1.2.1.12 compiled on Apr 8 1999 at 05:03:03

<sup>[</sup>BD-41212]: (E) Gate 'slow\_mode.clockblock' is bound to cell 'cb\_clk\_32\_1' which is not a proper parent. [BD-41212]: (E) Gate 'slow\_mode.clockblock\_1' is bound to cell 'cb\_clk\_32\_1' which is not a proper parent.

<sup>[</sup>BD-41212]: (E) Gate 'slow\_mode.clockblock\_2' is bound to cell 'cb\_clk\_32\_1' which is not a proper

```
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_3' is bound to cell 'cb_clk_32_1' which is not a proper
[BD-41212]: (E) Gate 'slow_mode.clockblock_4' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_5' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41200]: No illegal DOT gates found.
[BD-41202]: No illegal pin drops found.
       > nextnet chklegal
>>1: nextnet( chklegal );
[BD-41206]: No illegal pin drops found.
[BD-41204]: No illegally dotted nets found.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/late_area.tcl
         > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
         > noncritical repower(SCORE(FAST),LOWEST_NOT_EQUAL,NO_VIOL...
repower: setting SCORE option to FAST.
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1955.13 Avg: -181.08
maximum area for proto box IDCDSUC is 4655
--1955.13 Avg: -181.08
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -181.07
[BD-500026]: repower was applied 1 times.
[BD-500287]: score changed to OUT 0 of 0 times
[repower]: Execution time was 5.3 seconds.
     > bufmatch ESTIMATED,TWO_LEVEL,NO_VIOLATIONS
>>]: Itorbox( dbufmatch(ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
 -1955.13 Avg: -181.07
 [BD-500302]: 0 pins in 0 trees swapped, 9 trees tried
 -1955.13 Avg: -181.07
 [bufmatch]: Execution time was 0.1 seconds.
         > fanmatch {ACTUAL ,ONE_LEVEL,NO_VIOLATIONS}
 >>]: Itorbox( dfanmatch(ACTUAL ,ONE_LEVEL,NO_VIOLATIONS) );
 setting ACTUAL option.
 setting ONE_LEVEL option.
 setting NO_VIOLATIONS option.
 -1955.13 Avg: -181.07
 [BD-500300]: 0 pins on 0 gates swapped.
 -1955.13 Avg: -181.07
 [fanmatch]: Execution time was 3.6 seconds.
         > get_default_delay_synlimit
            > get_default_delay_synlimit
             > tc parm OFFSET(0)
           > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
 [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
```

```
[tc_parm]: [set benefit per unit cost]: benefit units is 0.000172
             [tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
             [tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
             [tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
                      > quick tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
             >>]: [quick]:( tdual_correct(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
             -1955.13 Avg: -181.07
             [tdual_correct]: setting SCORE option to ALL.
             [tdual correct]: setting RE POWER option.
             [tdual_correct]: setting INC mode.
             [tdual_correct]: setting NO VIOLATIONS option.
             -1955.13 Avg: -181.07
             maximum area for proto box IDCDSUC is 4655
             -1955.13 Avg: -181.07
            [quick]: Number of boxes to process is 398.
[quick]: Number of boxes processed is 0.
             Selected 398 critical boxes of 919 total.
         -1955.13 Avg: -181.07
                     ect]: applied 0 times
> tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
           [tdual_correct]: applied 0 times
> compare_critical_slack_limit
       -1955.13 Avg. -181.07
        comparing new slack -1955.1339 to saved slack -1935.5825
             > get_default_synlimit
                > get_default_synlimit
> get_default_synlimit
                     > get_default_synlimit
                     > get_default_synlimit
                     > get default synlimit
                     > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE OFF...
                     > noncritical onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO ...
             [onebuff]: setting SCORE option to ALL.
             [onebuff]: setting RE_POWER option.
             [onebuff]: setting LOWEST mode.
             [onebuff]: setting WORST option.
            [onebuff]: setting NO_VIOLATIONS option.
             -1955.13 Avg: -181.07
             maximum area for proto box IDCDSUC is 4655
             -1955.13 Avg: -181.07
             [noncritical]: noncritical applied to boxes with slack > 0.00
             [noncritical]: Number of boxes to process is 919.
             [noncritical]: Number of boxes processed is 0.
             -1955.13 Avg: -181.07
             [onebuff]: was applied 0 times
                     > noncritical dinv(SCORE(ALL), RE_POWER, LOWEST, WORST, NO_VIO...
             setting SCORE option to ALL.
             setting RE_POWER option.
```

```
setting LOWEST mode.
setting WORST option.
setting NO_VIOLATIONS option.
-1955.13 Avg: -181.07
maximum area for proto box IDCDSUC is 4655
-1955.13 Avg: -181.07
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 919.
[noncritical]: Number of boxes processed is 0.
-1955.13 Avg: -192.43
[BD-500500]: Moved 15 sinks and removed 10 inverters.
        > get_default_synlimit
        > get_default_synlimit
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/time_redund.tcl
          > is parm no_tech_redund
            > str_parm tgfs_effort
            > is_parm no_tech_redund
            > is parm remove_redundant_regs ....
             > make_constants_in nonreg_only
         > ignore_trivial_expansions EQNVIEW
            > expansions_from_tib EQNVIEW
             > expansions_from_eqn EQNVIEW
             > copy_def_to_proto EQNVIEW
            > apply decide_boolean(EQNVIEW)
generated 1 paths in 70 milliseconds
  > apply Hstructure(TRULE_BASE_AUTOGEN)
generated 1 paths in 40 milliseconds
           > gen_nonreg_tib_expns TIB_EXPANSIONS
     > gen_nonreg_tib_expris tro__...
> apply Hunstructure()
            > expandable_name
            > set_nochange
                 > constmod
             > is_parm keep_bad_pgroups
                 > bad_pgroups_expandable
                 > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(TRULE_BASE_AUTOGEN)) );
>>1: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 909 objects as matching keyword criteria.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1132 signals, 909 usage boxes and 1747 connections.
[simple expand]: Modfied 0 gates.
                  > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
```

```
VIEW(TIB_EXPANSIONS)));
   >>]: nextbox( SASname(RESTORE) );
   [synsasname]: Restored 0 BRKPT net names
   [synsasname]: Restored 189 REG and SEQUENTIAL output net names
   [synsasname]: Execution time was 0.0 seconds.
   [BD-354200]: Selected 0 out of 909 objects as matching keyword criteria.
   >>]: nextbox( SASname(PROTECT) );
   [synsasname]: Protected 180 BRKPT net names
  [synsasname]: Protected 189 REG and SEQUENTIAL output net names
  [synsasname]: Execution time was 0.0 seconds.
  [sweep]: sweep deleted 0 signals and 0 usage boxes.
                            The model has 1132 signals, 909 usage boxes and 1747 connections.
  [simple_expand]: Modfied 0 gates.
                      > headless
  [headless]: Removed 0 boxes
  [sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1132 signals, 909 usage boxes and 1747 connections.
                      > cleanse1
  Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                            The model has 1132 signals, 909 usage boxes and 1747 connections.
  >>]: nextbox( invrem(),onein(),twoin() );
using pattern information

[BD-40600]: Removed 0 double inverters.

[invrem]: Execution time was 0.0 seconds.

[BD-40500]: Removed 0 noninverting buffers.

[BD-40501]: Changed 0 gates to inverters.
  [onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
  [sweep]: sweep deleted 0 signals and 0 usage boxes.
                            The model has 1132 signals, 909 usage boxes and 1747 connections.
  >>]: nextbox( twoin() );
  [BD-40550]: Removed 0 redundant pins.
  [twoin]: Execution time was 0.0 seconds.
                    > nochange
                 > set_nochange
                 > apply {Hstructure( TRULE_BASE_AUTOGEN TIB_EXPANSIONS)}
  generated 1 paths in 60 milliseconds
                 > rtolbox {Htgfsredund( 100 )}
  >>]: rtolbox( Htgfsredund( 100 ) );
  [BD-330500]: Out of 2359 faults found 0 redundancies, eliminated 0, could not decide 0 in 1 seconds.
                 > apply Hunstructure()
                 > nochange
               > DeleteAllProtosUnderView TIB_EXPANSIONS
  [SRULE-17175]: Deleted 0 Proto Boxes
               > randsim q
  >>]: randsim(q);
               > randsim q
```

```
>>]: randsim(q);
              > is_parm keep_bad_pgroups
               > copyinfo
               > fix_bad_pgroups
[BD-82400]: Added 0 terminators, deleted 0 pins and tied 0 pins.
              > basetype
>>]: nextbox_with_test( test_syn_hide(!HIDE_MAP),genmark );
[test_syn_hide]: Number of objects selected was 909 of 909 checked.
>>]: nextnet( geninv );
             > copyinfo
              > nextbox {mapprim, mapterm}
>>]: nextbox( mapprim, mapterm );
[mapprim]: Execution time was 0.0 seconds.
[BD-83600]: 0 terminators processed 0 dummy nets removed.
              > cleanse
Removed-0-boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 1132 signals, 909 usage boxes and 1747 connections.
>>]: nextbox( invrem(),onein(),twoin() );
using pattern information
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
etej: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 1132 signals, 909 usage boxes and 1747 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 1132 signals, 909 usage boxes and 1747 connections.
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
              > nextbox tchname(NOERR)
>>]: nextbox( tchname(NOERR) );
NOERR option set
[BD-85300]: Looked at 909 gates, bound 0, 0 had hints.
[tchname]: Execution time was 0.0 seconds.
Pattern hint flag is inactive
              > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                           The model has 1132 signals, 909 usage boxes and 1747 connections.
 >>1: nextbox( invrem(),onein(),twoin() );
 using pattern information
```

```
[BD-40600]: Removed 0 double inverters.
            [invrem]: Execution time was 0.0 seconds.
            [BD-40500]: Removed 0 noninverting buffers.
            [BD-40501]: Changed 0 gates to inverters.
            [onein]: Execution time was 0.0 seconds.
            [BD-40550]: Removed 0 redundant pins.
            [twoin]: Execution time was 0.0 seconds.
            [cte]: Removed 0 boxes.
            [cte]: Execution time was 0.0 seconds.
           [sweep]: sweep deleted 0 signals and 0 usage boxes.
                               The model has 1132 signals, 909 usage boxes and 1747 connections.
           [cleanup]: 0 boxes disconnected
           [sweep]: sweep deleted 0 signals and 0 usage boxes.
                               The model has 1132 signals, 909 usage boxes and 1747 connections.
           >>]: nextbox( twoin() ):
           [BD-40550]: Removed 0 redundant pins.
           [twoin]: Execution time was 0.0 seconds.
                     > copyinfo
            > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...
           [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
           [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
> reset_key_slack_limit TIME_REDUND
           -1955.13 Avg: -192.43
           resetting keyed current slack to -1955.1339
                       > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
           critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
           -1955.13 Avg: -192.43
           maximum area for proto box IDCDSUC is 4635
           setting SCORE option to ALL.
           setting ACTUAL option.
           setting TWO_LEVEL option.
           setting NO_VIOLATIONS option.
           -1955.13 Avg: -192.43
           ArrayNum: 6 ArrayMax: 909
           [BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
           [tswap]: Execution time was 0.0 seconds.
           [BD-502000]: Called transforms 6 times and applied 0 of them.
                      > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}
           critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS) );
           -1955.13 Avg: -192.43
           maximum area for proto box IDCDSUC is 4635
           repower: setting SCORE option to ALL.
           repower: setting INC mode.
           repower: setting NO_VIOLATIONS option.
```

```
-1955.13 Avg: -192.43
ArrayNum: 6 ArrayMax: 909
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
            > compare_key_slack_limit TIME_REDUND
-1955.13 Avg: -192.43
comparing keyed new slack -1955.1339 to keyed saved slack -1935.5825
            > delete key slack limit TIME_REDUND
            > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
>>1: [quick]:( onebuff(SCORE(ALL), RE_POWER, INC, NO_VIOLATIONS) );
-1955.13 Avg: -192.43
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting INC mode.
[onebuff]: setting NO_VIOLATIONS option.
-1955.13 Avg: -192.43
maximum area for proto box IDCDSUC is 4635
[quick]: Number of boxes to process is 909.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -192.43
[onebuff]: was applied 0 times
            > quick dinv(SCORE(ALL), RE_POWER, INC, NO_VIOLATIONS)
>>]: [quick]:( dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1955.13 Avg: -192.43
setting SCORE option to ALL.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
-1955.13 Avg: -192.43
maximum area for proto box IDCDSUC is 4635
[quick]: Number of boxes to process is 909.
[quick]: Number of boxes processed is 0.
-1955.13 Avg: -188.21
[BD-500500]: Moved 5 sinks and removed 3 inverters.
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/opt_delay.tcl
              > syntrace
               > logic_report
Model Summary of Network 'IDCDSUC'
            Input Ports:
                          122
            Output Ports: 73
            Bidi Ports:
                         0
            Gates:
                         906
            Nets:
                        1127
            Connections: 1671
            Sequential Area: 2726
            Total Area:
```

Cell Distribution of Network 'IDCDSUC'

Count Cell Function Area TotalArea

1	cs_ao12n05c	AOI	6	6	
1	cs_ao22n04c	AOI	6	6	
1	cs_ao12n10c	AOI	12	12	
1	cs_ao22n10c	IOA	18	18	
2	cs_ao12n03c	AOI	4	8	
6	cs_ao22n03c	IOA	6	36	
180	BRKPT	BRKPT	0	0	
195	IOPAD	IOPAD	0	0	
17	cs_nnd2n04c		3	51	
3	cs_nnd2n11c	NAND	11	33	
1	cs_nnd2n05c	NAND	4	4	
1	cs_nnd2n08c	NAND	7	7	
2	cs_nnd3n05c	NAND	6	12	
6	cs_nnd2n14c	NAND	19	114	
1.	cs_nnd2n10c	NAND	. 8	8	
2	cs_nnd4v06c	NAND	8	16	
<u></u>	cs_nnd2n13c	NAND	15	15	
1	cs_nnd3z07c	NAND	10	10	
1	cs_nnd3n07c	NAND		6	en i na spojekama jiha ku ji ku ili kure 45 inak sidamin na 1964 ke ke ke jiji
1	cs_nnd2f03c	NAND	4.	4	
4	cs_nnd2n12c	NAND	12	48	
	cs_nnd3n02c	NAND	4	76	
2	cs_nnd2n14e		19	38	
144	cs_nnd2n02c			432	
3	cs_nnd2n03c	NAND			The second secon
	cs_nnd3n10c-		12	12	
	cs_nnd4n03c	NAND		25	The state of the state of the company of the state of the
The man to provide a second contract to the contract to	cs_nnd2n07c	NAND	4	8	oli vil 1990 – 1990 <del>– 1990 – </del>
**************************************	cs_nnd2n14b	NAND	20		and the control of th
2	cs_nnd3n03c	NAND	4	8.	
1	cs_nnd3n12b	NAND	22	22	
2	cs_nnd4n10c	NAND	20	40	The state of the s
. 1	cs_nor2n12c	NOR	. 12	12	
1	cs_nor3n03c	NOR	4	4	
1	cs_nor3n10e	NOR	16	16	
8	cs_nor2n02c	NOR	3	24	to the stage of consistency and the stage of the constraint of the stage of the sta
3	cs_nor2n04c	NOR	3	9	
1	cs_nor2n11c	NOR	11	11	
6	cs_invvn13c	NOT	8	48	
1	cs_invvv19b	NOT	28	28	
7			2		•
4	cs invvn06c	NOT		14	
	cs_invvn06c	NOT NOT		14 16	
3	cs_invvn08c	NOT	4	16	
3	cs_invvn08c cs_invvn02c	NOT NOT	4 2	16 6	
3	cs_invvn08c cs_invvn02c cs_invvn14c	NOT NOT NOT	4 2 8	16 6 24	
3 8	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c	NOT NOT NOT NOT	4 2 8 2	16 6 24 16	
3 8 8	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c	NOT NOT NOT NOT NOT	4 2 8 2 2	16 6 24 16 16	
3 8 8 46	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c cs_invvn07c	NOT NOT NOT NOT NOT	4 2 8 2 2 2	16 6 24 16 16 92	
3 8 8 46 7	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c cs_invvn07c cs_invvn10c	NOT NOT NOT NOT NOT NOT	4 2 8 2 2 2 4	16 6 24 16 16 92 28	
3 8 8 46 7 1	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c cs_invvn07c cs_invvn10c cs_invvn01e	NOT NOT NOT NOT NOT NOT NOT	4 2 8 2 2 2 4 2	16 6 24 16 16 92 28 2	
3 8 8 46 7 1 54	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c cs_invvn07c cs_invvn10c cs_invvn01e cs_invvn01c	NOT NOT NOT NOT NOT NOT NOT NOT	4 2 8 2 2 2 4 2 2	16 6 24 16 16 92 28 2 108	
3 8 8 46 7 1 54 22	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c cs_invvn07c cs_invvn10c cs_invvn01e cs_invvn01c cs_invvn01c	NOT NOT NOT NOT NOT NOT NOT NOT NOT	4 2 8 2 2 4 2 2 6	16 6 24 16 16 92 28 2 108 132	
3 8 8 46 7 1 54	cs_invvn08c cs_invvn02c cs_invvn14c cs_invvn04c cs_invvn05c cs_invvn07c cs_invvn10c cs_invvn01e cs_invvn01c	NOT NOT NOT NOT NOT NOT NOT NOT	4 2 8 2 2 2 4 2 2	16 6 24 16 16 92 28 2 108	

```
60
                   NOT
                              10
      cs_invvn15c
                                     18
  3
     cs invvn11c
                   NOT
                               6
                    OAI
                              18
                                     18
     cs_oa22n10c
  1
                                     28
  2
      cs oa21n10c
                    OAI
                              14
                               26
                                     468
  18
      cl_nnd2n07c
                    REG
      cl_invvn05c
                   REG
                              25
                                     25
  1
     cl ao22n07c
                    REG
                              33
                                     264
  8
      cl_invvn06d
                   REG
                              25
                                     350
  14
                              25
                                     25
      cl invvn05d
                   REG
  1
      cl_nnd3n07c
                    REG
                              29
                                     58
  2
                              25
                                     300
  12
      cl_invvn07c
                   REG
      cl_nor2n06c
                   REG
                              26
                                     26
                   REG
                              25
                                     550
  22
      cl invvn07d
                    REG
                              30
                                     30
      cl_ao21n07c
  1
  2
                              25
                                     50
      cl_invvn06c
                   REG
                                     30
      cl_oa21n07c
                    REG
                              30
  1
      cb_mode_block SEQUENTIAL
                                    70
                                           .70
  1
                    SEQUENTIAL 80
                                         480
  6
      cb clk 32 1
                    XNOR
                                       8 -
  1
      cs_xbn2n01b
      cs xbo2n01d
                    XOR ..... 8 ........8.....
             > write_end_point_report -points 3
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end_point_report..92476.--
[ET-0019]: <End....New Endpoint Report.
Sun Apr 18 22:03:52 1999
Part: IDCDSUC
Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                 Max. Slack: 1.13427E+38
Sort Field: Slack
                              Max. Endpoints: 3
Cause of Slack
                      Abbreviation Comparison/Description
                        SlkCont
                                  Slack due to a point downstream on path
 Slack Continuation
                                  ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
                        RAT
 Asserted Required Arrival Time AssrtRAT.....( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
                                   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 Clock Gating Setup
                        ClkGSet
ARRIVAL TIME + ADJUST )
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                        ClkGHld
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                          CIKTPW
                                     ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
                             ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
 Setup
ADJUST)
                            ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 Hold
                   Hold
ADJUST)
                                 ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                      EndOfC
 EndOfCycle
ADJUST)
                        CIkPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 ClockPulseWidth
TRAILING EDGE)
                                  ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ClockSeparation
                       ClkSep
ARRIVAL TIME + ADJUST )
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 Loop
                   ALTest
```

CLOCK + ADJUST )
Arrival Time Limiting

**ATLimit** 

Slack discontinuity due to failed test

	<b>-</b>	The Elimit Clark discontinuity due to failed test
	Num/	LimitedAT/ Delay/ Failed Test/
	Test PinName	E Phase AT Slack Slew CL FO Cell P Func T.Adj
	NetName	the same state of the same sta
	1 dod suce leet #1	D.CO. D
	1 dcd_succ_last_t1 dcd_succ_last_t1	R C3+R 2954 -1955 3847 1011 1 PO 0
	RAT	999
	> BOX714/OUT	<b>B B B B B B B B B B</b>
	0 dcd_succ_last_t1	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
	> BOX714/IN	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1&0	TOTAL TOTAL TOTAL
	> C167/y	R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	100 100 100 100 100 100 100 100 100 100
•	> C167/a	F C3+R 1092 -1955 55 139 4 cs_invvn 01c NOT
	1862 N675	
ي ديد سند .	>{a} C2738/y	F C3+R 1092 -1955 55 139 4 cs_nnd2n 14b NAND
	0 N675	
	> C2738/a	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14b NAND
	29 last_cycle	
	>{b} C2487/y	R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND
	0 last_cycle	
	> C2487/b > N1587	F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	> C1952/y	E C2 D 1024 1055
	N1587	F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
	> C1952/a	R C3+R 1024 -1955 80 319 1 cs_invvv 19b NOT
and the care	10 num_dcd_cyl&0(1)	19D NOT
men and the same of	> BOX679/OUT	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
	0 num_dcd_cyl&0(1)	그는 그들 가는 하는 사람들은 사람들이 되었다. 그는 사람들은 그리고 하는 사람들이 되었다.
	> BOX679/IN	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
	num_dcd_cyl(1)	
	> num_dcd_cyl(1)	R C3+R 1024 -1955 80 319 1 PI 0
	num_dcd_cyl(1)	A distribution of the state of
	2 dcd_succ_last_t1	E CO. D. 0044 4045 0000 4044 4 DO
	dcd_succ_last_t1	F C3+R 2644 -1645 2362 1011 1 PO 0
	RAT	999 0
	> BOX714/OUT	F 00 B
	0 dcd_succ_last_t1	F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
	> BOX714/IN	F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1&0	TOTAL
	> C167/y	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	
	> C167/a	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
	1436 N675	
	>{a} C2738/y	R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
	0 N675	
	> C2738/b	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
	56 N1692 >{b} C2725rwr/y	E CO. D. 4450 4045 TO 170 O
	>{U} OZ/Z3(WI/Y	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND

	0 N1692	R C3+R	1007 1645	1/0	166 2 cs_nnd2n	14e NAND
	> C2725rwr/a	n Co+n	1097 -1045	140	100 2 05_1110211	146 INVIND
	56 N1479	D 00 D	4007 4045	140	166 0 as and0n	105 NAND
	>{c} C2721rwr/y	R C3+R	1097 -1645	148	166 2 cs_nnd3n	I IZD NAND
	0 N1479					401 NAND
	> C2721rwr/c	F C3+R	994 -1645	125	95 2 cs_nnd3n	120 NANU
	102 N1497					
	>{d} C2709rwr/y	F C3+R	994 -1645	125	95 2 cs_nor3n	10e NOR
	0 N1497					
	> C2709rwr/c	R C3+R	898 -1645	137	68 2 cs_nor3n	10e NOR
	96 N1781					
	>{e} C2885/y	R C3+R	898 -1645	137	68 2 cs_nnd4n	10c NAND
	0 N1781					
	> C2885/d	F C3+R	825 -1645	44 5	50 1 cs_nnd4n 1	0c NAND
	73 N1997					
	>{f} C2886/y	F C3+R	825 -1645	44 5	50 1 cs_nnd2n 1	4c NAND
	0 N1997					
	> C2886/a	R C3+R	802 -1645	80 1	24 2 cs_nnd2n	14c NAND
	23 op_serialize&0		• •			
٠.	> BOX638/OUT	R C3+F	8021645	80	124 2 IOPAD	IOPAD
	0 op serialize&0	•	•			• •
	> BOX638/IN	R C3+R	802 -1645	80	124 2 IOPAD	IOPAD- 0
	op_serialize					* ABOUT
	> op_serialize	R C3+R	802 -1645	80 1	124 2 Pl	0
-	op_serialize					*********************************
٠.	> op_serialize op_serialize					
•						
	3 iu reset op c t1	R C3+R	2610 - 1611	391	2 1011 1 PO	
	3 iu reset op c t1	R C3+R	2610 - 1611	391	2 1011 1 PO	
• • • • • • • • • • • • • • • • • • • •	3 iu reset op c t1	R C3+R	2610 - 1611	391	2 1011 1 PO	
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT	R C3+R	2610 - 1611	391	2 1011 1 PO	
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1	R C3+R 999 R C3+F	2610 <sup>-</sup> -1611 3 2610 -161	391	2 1011 1 PO 0 12 1011 1 IOPAE	) IOPAD
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 BAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN	R C3+R 999 R C3+F	2610 <sup>-</sup> -1611 3 2610 -161	391	2 1011 1 PO 0 12 1011 1 IOPAE	) IOPAD
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0	R C3+R 999 R C3+F R C3+R	2610 -1611 3 2610 -161 2610 -1611	391; 1 39 3912	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD	O IOPAD
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y	R C3+R 999 R C3+F R C3+R	2610 -1611 3 2610 -161 2610 -1611	391; 1 39 3912	2 1011 1 PO 0 12 1011 1 IOPAE	O IOPAD
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0	999 R C3+F R C3+R R C3+R	2610 -1611 2610 -161 2610 -1611 2610 -1611	3912 1 39 3912 3912	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r	IOPAD IOPAD O2c NAND
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a	999 R C3+F R C3+R R C3+R	2610 -1611 2610 -161 2610 -1611 2610 -1611	3912 1 39 3912 3912	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD	IOPAD IOPAD O2c NAND
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 2043 gbfonet_6	999 R C3+F R C3+R R C3+R F C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611	391; 1 39 3912 3912 96 1	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n	IOPAD IOPAD O2c NAND
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a	999 R C3+F R C3+R R C3+R F C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611	391; 1 39 3912 3912 96 1	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r	IOPAD IOPAD O2c NAND
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 2043 gbfonet_6> gbfocell_6/y gbfonet_6	999 R C3+F R C3+R R C3+R F C3+R F C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611	391; 1 39 3912 3912 96 1	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 0	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 2043 gbfonet_6> gbfocell_6/y	999 R C3+F R C3+R R C3+R F C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611	391; 1 39 3912 3912 96 1	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 2043 gbfonet_6> gbfocell_6/y gbfonet_6	999 R C3+F R C3+R R C3+R F C3+R F C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611	391; 1 39 3912 3912 96 1 96 1 217	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O9c NOT
	3 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 2043 gbfonet_6> gbfocell_6/y gbfonet_6> gbfocell_6/a	999 R C3+F R C3+R R C3+R F C3+R F C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611	391; 1 39 3912 3912 96 1 96 1 217	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 0	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O9c NOT
		999 R C3+F R C3+R R C3+R F C3+R F C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611	391; 1 39 3912 3912 96 1 96 1 217 217	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn 43 1 cs_nnd3n	IOPAD IOPAD 1 02c NAND 02c NAND 09c NOT 0 09c NOT
		999 R C3+F R C3+R R C3+R F C3+R F C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611	391; 1 39 3912 3912 96 1 96 1 217 217	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn	IOPAD IOPAD 1 02c NAND 02c NAND 09c NOT 0 09c NOT
		999 R C3+F R C3+R R C3+R F C3+R F C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611 358 -1611	3912 3912 3912 96 1 96 1 217 217	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn 43 1 cs_nnd3n 216 5 cs_nnd3n	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND
		999 R C3+F R C3+R R C3+R F C3+R F C3+R R C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611 358 -1611	3912 3912 3912 96 1 96 1 217 217	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn 43 1 cs_nnd3n	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND
		999 R C3+F R C3+R R C3+R F C3+R F C3+R R C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611 358 -1611	3912 3912 3912 96 1 96 1 217 217 144 2	2 1011 1 PO 0 12 1011 1 IOPAL 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn 43 1 cs_nnd3n 216 5 cs_nnd3n 144 216 5 cl_ii	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND O2c NAND O2c NAND O2c NAND
		999 R C3+F R C3+R R C3+R F C3+R F C3+R R C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611 358 -1611	3912 3912 3912 96 1 96 1 217 217 144 2	2 1011 1 PO 0 12 1011 1 IOPAE 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn 43 1 cs_nnd3n 216 5 cs_nnd3n	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND
		999 R C3+R R C3+R R C3+R F C3+R R C3+R R C3+R R C3+R	2610 -1611 2610 -1611 2610 -1611 2610 -1611 568 -1611 490 -1611 490 -1611 358 -1611	3912 3912 3912 96 1 96 1 217 217 144 2	2 1011 1 PO 0 12 1011 1 IOPAL 1044 3 IOPAD 1044 3 cs_nnd2r 96 6 cs_nnd2n 196 6 cs_invvn 43 1 cs_invvn 43 1 cs_nnd3n 216 5 cs_nnd3n 144 216 5 cl_ii	IOPAD IOPAD O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND O9c NOT O2c NAND O2c NAND

----> slow\_mode.clockblock/c2 0 slow\_mode.c2\_1 R C3+ 160 N/C 60 222 13 cb\_clk\_32\_1 LCB

<sup>&</sup>gt; tc\_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE\_OFF...

> noncritical repower(SCORE(FAST),LOWEST\_NOT\_EQUAL,NO\_VIOL...

repower: setting SCORE option to FAST.

repower: setting LOWEST\_NOT\_EQUAL mode.

repower: setting NO\_VIOLATIONS option.

-1955.13 Avg: -188.21

maximum area for proto box IDCDSUC is 4614

-1955.13 Avg: -188.21

[noncritical]: noncritical applied to boxes with slack > 0.00

[noncritical]: Number of boxes to process is 906. [noncritical]: Number of boxes processed is 0.

-1955.13 Avg: -188.21

[BD-500026]: repower was applied 0 times.

[BD-500287]: score changed to OUT 0 of 0 times

[repower]: Execution time was 5.1 seconds.

> syntrace

> logic\_report

## Model Summary of Network 'IDCDSUC'

Input Ports: 122
Output Ports: 73
Bidi Ports: 0
Gates: 906
Nets: 1127
Connections: 1671

Sequential Area: 2726 Total Area: 4614

## Cell Distribution of Network 'IDCDSUC'

Cour	it Cell -	Hunction	Area	TotalArea	
				•••	
1	cs_ao12n05c	AOI	6	6	· · · · · · · · · · · · · · · · · · ·
· 1	cs_ao22n04c	AOI	6	6	
1	cs_ao12n10c	AOI	12	12	
1	cs_ao22n10c	AOI	18	18	
2	cs_ao12n03c	AOI	4	8	· · · · · · · · · · · · · · · · · · ·
6	cs_ao22n03c	AOI	6	36	
180	BRKPT	BRKPT	0	0	
195	IOPAD	IOPAD	0	0	
17	cs_nnd2n04c	NAND	3	51	
3	cs_nnd2n11c	NAND	11	33	
1	cs_nnd2n05c	NAND	4	4	
1	cs_nnd2n08c	NAND	7	7	
2	cs_nnd3n05c	NAND	6	12	
6	cs_nnd2n14c	NAND	19	114	
1	cs_nnd2n10c	NAND	8	8	
2	cs_nnd4v06c	NAND	8	16	
1	cs_nnd2n13c	NAND	15	15	
1	cs_nnd3z07c	NAND	10	10	•
1	cs_nnd3n07c	NAND	6	6	
1	cs_nnd2f03c	NAND	4	4	
4	cs_nnd2n12c	NAND	12	48	
19	cs_nnd3n02c	NAND	4	76	

```
38
                    NAND
                                19
2
    cs_nnd2n14e
                                       432
     cs_nnd2n02c
                     NAND
                                 3
144
                    NAND
                                3
                                       9
3
    cs_nnd2n03c
                                12
                                       12
                    NAND
1
    cs_nnd3n10c
                    NAND
                                5
                                       25
5
    cs_nnd4n03c
                                4
                                       8
2
    cs_nnd2n07c
                    NAND
                                       20
                                20
 1
    cs nnd2n14b
                    NAND
2
    cs_nnd3n03c
                    NAND
                                4
                                       8
                                       22
                    NAND
                                22
 1
    cs_nnd3n12b
                                20
                                       40
2
    cs_nnd4n10c
                    NAND
                               12
                                      12
                   NOR
 1
    cs_nor2n12c
                               4
                                      4
                   NOR
 1
    cs_nor3n03c
                   NOR
                               16
                                      16
 1
    cs_nor3n10e
                   NOR
                               3
                                     24
    cs_nor2n02c
 8
                               3
                                      9
                   NOR
 3
    cs_nor2n04c
                                      11
                   NOR
                               11
 1
    cs_nor2n11c
                   NOT
                               8
                                     48
 6
    cs_invvn13c
                                     28
                              28
                   NOT
 1
    cs invvv19b
                               2 .
                   NOT
                                    -14
 7
    cs_invvn06c
                   NOT
                               4.....
                                     16
 4
    cs invvn08c
                               2
 3
                                     6
    cs invvn02c
                   NOT
                               8
                                     24
 3
     cs_invvn14c
                   NOT
                               2
 8
     cs_invvn04c
                   NOT
                                     16
                               2 -- 16
 8
     cs_invvn05c
                   NOT
                               2
                                     92
46
     cs_invvn07c
                   NOT
 7
     cs_invvn10c
                   NOT
                                     28
                   NOT
                               2
                                     .2
 1
     cs_invvn01e::
54.
     cs_invvn01c
                   NOT
                                     108
22
     cs_invvn12c
                   NOT
                               6
                                    - 132
                   NOT
                               4
                                     24
 6
     cs_invvn09c
                                     14
 1
     cs invvn16c
                   NOT:
                              14
                              10
                                     60
                   NOT
 6
     cs_invvn15c
                                     18
                               6
 3
                   NOT
     cs invvn11c
     cs_oa22n10c
                    OAL
                               18
                                      18
 1
                                      28
 2
                    OAI
                               14
     cs_oa21n10c
                               26
                                      468
18
     cl nnd2n07c
                    REG
                                     25 .
 1.
     cl_invvn05c
                   REG
                              25 .
                               33
                                     264
 8
     cl_ao22n07c
                   REG
                              25
                                     350
                   REG
 14
     cl_invvn06d
                                     25
     cl_invvn05d
                   REG
                              25
 1
                               29
                                      58
                   REG
 2
     cl_nnd3n07c
                                     300
                              25
 12
     cl_invvn07c
                   REG
     cl_nor2n06c
                   REG
                              26
                                     26
 1
22
                   REG
                               25
                                     550
     cl_invvn07d
                               30
                                      30
     cl_ao21n07c
                    REG
 1
                              25
                                     50
 2
     cl_invvn06c
                   REG
                                      30
                    REG
                               30
 1
     cl_oa21n07c
     cb_mode_block
                                     70
                                            70
 1
                     SEQUENTIAL
     cb_clk_32_1
                    SEQUENTIAL
                                   80
                                          480
 6
                                 8
                                        8
     cs_xbn2n01b
                    XNOR
 1
                                8
                                       8
                    XOR
 1
     cs_xbo2n01d
```

> write\_end\_point\_report -points 3
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end point\_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:03:58 1999

Part: IDCDSUC

Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Cause of Slack

Max. Endpoints: 3
Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path

Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

TIME)

Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

ARRIVAL TIME + ADJUST )

Clock Gating Hold CIKGHID (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK

ARRIVAL TIME + ADJUST )

Clock Tree Pulse Width ClkTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE)

Setup Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +

ADJUST)

Hold Hold (DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +

ADJUST)

ADJUST)

ClockPulseWidth ClkPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE)

ClockSeparation ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2

ARRIVAL TIME + ADJUST)

Loop ALTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM

CLOCK + ADJUST ).

Arrival Time Limiting ATLimit Slack discontinuity due to failed test

Num/ LimitedAT/ Delay/ Failed Test/
Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj
NetName

1 dcd\_succ\_last\_t1 R C3+R 2954 -1955 3847 1011 1 PO 0 dcd\_succ\_last\_t1 RAT 999 ----> BOX714/OUT R C3+R 2954 -1955 3847 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1 ----> BOX714/IN R C3+R 2954 -1955 3847 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1&0 ----> C167/y R C3+R 2954 -1955 3847 1011 1 cs\_invvn 01c NOT 0 dcd\_succ\_last\_t1&0 ----> C167/a FC3+R 55 139 4 cs\_invvn 01c NOT 1092 -1955 1862 N675 ---->{a} C2738/y FC3+R 1092 -1955 55 139 4 cs\_nnd2n 14b NAND 0 N675 ----> C2738/a R C3+R 1063 -1955 71 108 1 cs\_nnd2n 14b NAND 29 last\_cycle ---->{b} C2487/y R C3+R 1063 -1955 71 108 1 cs\_nnd2n 14e NAND

	0 last_cycle	E 00 D 4004 4055 00 440 0 as middle 440 NAND
	> C2487/b	F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
	29 N1587	= 00 = 1001 1077 00 110 0 == invest 10b NOT 0
	> C1952/y	F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
	N1587	= 55 = 1551 10== 00 040 4 55 invest 40h NOT
	> C1952/a	R C3+R 1024 -1955 80 319 1 cs_invvv 19b NOT
	10 num_dcd_cyl&0(1)	IODAD IODAD
	> BOX679/OUT	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
	0 num_dcd_cyl&0(1)	
	> BOX679/IN	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
	num_dcd_cyl(1)	7 00 D 1004 1055 00 010 1 DI 0
		R C3+R 1024 -1955 80 319 1 PI 0
	num_dcd_cyl(1)	
	2 ded suce last t1	F C3+R 2644 -1645 2362 1011 1 PO 0
	2 UCU_SUCC_IASI_CI	F 03th 20th 10to 2002 10th 110
	dcd_succ_last_t1 RAT	999
	POY71//OUT	999 F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
	O ded area lost ti	
•	> BOX714/IN	F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
		1 00711 2077 1070 2002 1077 1.5.7.5
	0 dcd_succ_last_t1&0 > C167/y	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
•	0 dcd_succ_last_t1&0	F COTH 2011 1010 2002 1011 1 00
	> C167/a	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
	1436 N675	11 OOT11 1 1200 1 1040 1 02 1 100 1 35
		R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
	>{a} C2738/y 0 N675	
***	> C2738/b	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
	EO N4000	
	>{b} G2725rwr/y	F C3+R 1152 -1645 76 159 3 cs_nnd2n- 14e NAND
	0 N1692	
	> C2725rwr/a	R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND
•	56 N1479	
	>{c} C2721rwr/y	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
	0 N1479	
	> _C2721rwr/c	F C3+R 994 -1645 125 95 2 cs_nnd3n 12b NAND
	102 N1497	
	>{d} C2709rwr/y	F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
	0 N1497	
	> C2709rwr/c	R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR
	96 N1781	
	>{e} C2885/y	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
	0 N1781	
	> C2885/d	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
	73 N1997	
	>{f} C2886/y	F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
	0 N1997	
	> C2886/a	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
	23 op_serialize&0	
	> BOX638/OUT	R C3+R 802 -1645 80 124 2 IOPAD IOPAD
	0 op_serialize&0	
	> BOX638/IN	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
	op_serialize	
	> op_serialize	R C3+R 802 -1645 80 124 2 PI 0
1		

op	se	ria	lize

op_serialize	
3 iu_reset_op_c_t1	R C3+R 2610 -1611 3912 1011 1 PO 0
iu_reset_op_c_t1	
RAT	999 0
> BOX716/OUT	R C3+R 2610 -1611 3912 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	
> BOX716/IN	R C3+R 2610 -1611 3912 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	
>{a} C2393/y	R C3+R 2610 -1611 3912 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	500 B
> C2393/a	F C3+R 568 -1611 96 196 6 cs_nnd2n 02c NAND
2043 gbfonet_6	E 00 B
> gbfocell_6/y	F C3+R 568 -1611 96 196 6 cs_invvn 09c NOT
gbfonet_6> gbfocell_6/a	D.CO. D. 400 4044 047 40.4 ;
78 N2031	R C3+R 490 -1611 217 43 1 cs_invvn 09c NOT
>{b} C2162/y	D.CO.D. 400 4014 047 40 4 40
0 N2031	R C3+R 490 -1611 217 43 1 cs_nnd3n 02c NAND
> C2162/h	F C3+R 358 -1611 144 216 5 cs_nnd3n 02c NAND
132 rcvry_reset_q	1 COTT 1 COTT 144 2 TO 5 CS_TITIOSIT U2C NAME
	2_out_n F C3+R 358 -1611 144 216 5 cl_invvn 07d
SRL 0 rcvry_reset_q	u
> rcvry_reset.reg n.lat 0/c	2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 Slow mode.c2 1	
> slow_mode.clockblock/c2	P C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	
> write_end_point_repor	t -points 3 -paths 1
[ET-0018]: >BeginNew EndPo	oint Report
for file /tmp/end_point_r	
[ET-0019]: <endnew endpoi<="" td=""><td>пт нероп.</td></endnew>	пт нероп.
0 4 10.00.00 =0.1000	

Sun Apr 18 22:03:58 1999

Part: IDCDSUC

Mode: Late Mode / Nominal **EDA EinsTimer EndPoint Report** 

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

Slack Continuation SIkCont Slack due to a point downstream on path Required Arrival Time RAT

( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

TIME)

**Clock Gating Setup** ClkGSet ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

ARRIVAL TIME + ADJUST )

Clock Gating Hold ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK CIkGHId

ARRIVAL TIME + ADJUST )

Clock Tree Pulse Width **CIKTPW** ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE )

Setup Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +

ADJUST)

Hold	Hold (D	ATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST) EndOfCycle ADJUST) ClockPulseWidth TRAILING EDGE)	EndOfC	( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
	ClkPW	( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
ClockSeparation  ARRIVAL TIME + AD	ClkSep	( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
Loop CLOCK + ADJUST)	ALTest (	DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
Arrival Time Limiting	ATLimit	Slack discontinuity due to failed test
Num/ Test PinName NetName		LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
1 dcd_succ_last_dcd_succ_last_t1	<u>t</u> 1	R C3+R 2954 -1955 3847 1011 1 PO 0
RAT> BOX714/OUT		999 0 R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1 > BOX714/IN	* .	R C3+R 2954 -1955 3847 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&> C167/y	0	R C3+R 2954 -1955 3847 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&> C167/a		F C3+R 1092 -1955 55 139 4 cs_invvn 01c NOT
1862 N675 >{a} C2738/y		F C3+R 1092 -1955 55 139 4 cs_nnd2n 14b NAND
0 N675 > C2738/a	· ·	R C3+R 1063 -1955—71—108 1 cs_nnd2n 14b NAND
29 last_cycle >{b} C2487/y		R C3+R 1063 -1955 71 108 1 cs_nnd2n 14e NAND
0 last_cycle > C2487/b		F C3+R 1034 -1955 32 140 3 cs_nnd2n 14e NAND
29 N1587 > C1952/y		F C3+R 1034 -1955 32 140 3 cs_invvv 19b NOT 0
N1587 > C1952/a		R C3+R 1024 -1955 80 319 1 cs_invvv 19b NOT
10 num_dcd_cyl&0(* > BOX679/OUT		R C3+R 1024 -1955 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1) > BOX679/IN	)	R C3+R 1024 -1955 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1)> num_dcd_cyl( num_dcd_cyl(1)	1)	R C3+R 1024 -1955 80 319 1 Pl 0
2 dcd_succ_last dcd_succ_last_t1	_t1	F C3+R 2644 -1645 2362 1011 1 PO 0
RAT> BOX714/OUT		999 . 0 F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1 > BOX714/IN		F C3+R 2644 -1645 2362 1011 1 IOPAD IOPAD
0 dcd_succ_last_t18	XU	

	> C167/y	F C3+R 2644 -1645 2362 1011 1 cs_invvn 01c NOT
	0 dcd_succ_last_t1&0	_
	> C167/a	R C3+R 1208 -1645 92 139 4 cs_invvn 01c NOT
	1436 N675	
	>{a} C2738/y	R C3+R 1208 -1645 92 139 4 cs_nnd2n 14b NAND
	0 N675	
	> C2738/b	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14b NAND
	56 N1692	
	>{b} C2725rwr/y	F C3+R 1152 -1645 76 159 3 cs_nnd2n 14e NAND
	0 N1692	D.00 D. 1007 1045 140 100 0
	> C2725rwr/a 56 N1479	R C3+R 1097 -1645 148 166 2 cs_nnd2n 14e NAND
	>{c} C2721rwr/y	D.CO.D. 1007 1045 140 400 0 as anadon 40 NAND
	0 N1479	R C3+R 1097 -1645 148 166 2 cs_nnd3n 12b NAND
	> C2721rwr/c	F C3+R 994 -1645 125 95 2 cs nnd3n 12b NAND
	102 N1497	F C3+R 994 -1645 125 95 2 cs_nnd3n 12b NAND
		F C3+R 994 -1645 125 95 2 cs_nor3n 10e NOR
*	0 N1497	1 00+11 334 -10+3 125 35 2 CS_1101311 10e NON
	> C2709rwr/c	R C3+R 898 -1645 137 68 2 cs_nor3n 10e NOR
	96 N1781	13 90 17 00 10 10 10 10 2 03_101011 100 NOT
, <del>, , , , , , , , , , , , , , , , , , </del>	>{e} C2885/y	R C3+R 898 -1645 137 68 2 cs_nnd4n 10c NAND
	0 N1781	
	> C2885/d	F C3+R 825 -1645 44 50 1 cs_nnd4n 10c NAND
	73 N1997	
	>{f} C2886/y	F C3+R 825 -1645 44 50 1 cs_nnd2n 14c NAND
the second of the large second	0 N1997	
	> C2886/a	R C3+R 802 -1645 80 124 2 cs_nnd2n 14c NAND
and the second second	23 OD Serialize&U	The state of the s
The State of the Country of the Coun	0. op. opriolite 9.0	R.C3+R 802 -1645 80 124 2 IOPAD IOPAD
	O Op_serialize&U	R C3+R 802 -1645 80 124 2 IOPAD IOPAD 0
	> on serialize	B C3+B 802 -1645 80 124 2 DI 0
	op serialize	R C3+R 802 -1645 80 124 2 Pl 0
	3 iu_reset_op_c_t1	R C3+R 2610 -1611 3912 1011 1 PO 0
	iu_reset_op_c_t1	R C3+R 2610 -1611 3912 1011 1 PO 0
	RAT	999 0
	> BOX716/OUT	R C3+R 2610 -1611 3912 1011 1 IOPAD IOPAD
	0 iu_reset_op_c_t1	
	> BOX716/IN	R C3+R 2610 -1611 3912 1044 3 IOPAD IOPAD
	0 iu_reset_op_c_t1&0	D 00 D 0040 4044 0040 4044 0
	>{a} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2610 -1611 3912 1044 3 cs_nnd2n 02c NAND
	> C2393/a	E C2 D
	2043 gbfonet_6	F C3+R 568 -1611 96 196 6 cs_nnd2n 02c NAND
	> gbfocell_6/y	F C3+R 568 -1611 96 196 6 cs_invvn 09c NOT 0
	gbfonet_6	F C3+R 568 -1611 96 196 6 cs_invvn 09c NOT 0
	> gbfocell_6/a	R C3+R 490 -1611 217 43 1 cs_invvn 09c NOT
	78 N2031	
	>{b} C2162/y	R C3+R 490 -1611 217 43 1 cs_nnd3n 02c NAND
	0 N2031	
	> C2162/b	F C3+R 358 -1611 144 216 5 cs_nnd3n 02c NAND
	132 rcvry_reset_q	

```
----> rcvry_reset.reg_n.lat_0/l2_out_n
                                       FC3+R
                                                  358 -1611 144 216 5 cl invvn 07d
        0 rcvry_reset_q
SRL
                                     R C3+
                                                     N/C
                                                            60 222 13 cl_invvn 07d SRL
----> rcvrv reset.reg n.lat 0/c2
                                               160
198 slow_mode.c2_1
                                      R C3+
                                                160 N/C 60 222 13 cb_clk_32_1 LCB
---> slow_mode.clockblock/c2
0 slow_mode.c2_1
      > is parm new_assert
       > set slew prop ON
[set_slew_prop]: Setting slew propagation to 1 (ON)
       > tc_parm {CHK_SINKSLEW(Y)}
      > tc_parm SLEW_LIM(100)
       > tc_parm CAP_LIM(100)
      > critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...
critical(
repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
ATIONS), fantom(LIMITED), faninv(LIMITED));
-1873.06 Avg: -169.23
maximum area for proto box IDCDSUC is 4614
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
setting SCORE option to ALL. setting ACTUAL option.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
fantom: Found 152 valid buffers or inverters.
[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.
[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
                                              -1873.06 Avg: -169.23
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
frepowerl: Execution time was 0.1 seconds.
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.2 seconds.
[BD-500700]: Added 0 buffers.
[fantom]: Execution time was 0.0 seconds.
[BD-500701]: Added 0 inverters.
[faninv]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 24 times and applied 0 of them.
      > nextbox synexpand(XPANDVIEW)
>>]: nextbox( synexpand(XPANDVIEW) );
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1129 signals, 906 usage boxes and 1744 connections.
>>1: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
```

```
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
 [synsasname]: Execution time was 0.0 seconds.
 [synexpand]: expanded 0 boxes
         > reset_critical_slack_limit
 -1873.06 Avg: -169.23
 resetting the current slack to -1873.0634
         > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
 critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
 -1873.06 Avg: -169.23
 maximum area for proto box IDCDSUC is 4614
 setting SCORE option to ALL.
 setting ESTIMATED option.
 setting TWO_LEVEL option.
 setting NO_VIOLATIONS option.
 -1873.06 Avg: -169.23
 ArrayNum: 6 ArrayMax: 906
 [BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
 [tswap]: Execution time was 0.0 seconds.
 [BD-502000]: Called transforms 6 times and applied 0 of them.
        > tc_parm REGALL
        > repower_paths FUZZY(0.02)
 initial slack is -1873
 after repower paths slack is -1873
after repower paths slack is -1873

> critical {repower(SCORE(ALL),INC_,NO_VIOLATIONS), re...

critical( repower(SCORE(ALL),INC_,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1873.06 Avg: -169.73
maximum area for proto box IDCDSUC is 4606
repower: setting SCORE option to ALL.
repower: setting INC mode...
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1873.06 Avg: -169.73
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.2 seconds.
[BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.2 seconds.
 [BD-502000]: Called transforms 12 times and applied 0 of them.
        > compare_critical_slack_limit
-1873.06 Avg: -169.73
comparing new slack -1873.0634 to saved slack -1854.3328
          > reset_critical_slack_limit
 -1873.06 Avg: -169.73
resetting the current slack to -1873.0634
          > quick tswap(SCORE(ALL),ACTUAL,ONE_LEVEL)
>>]: [quick]:( tswap(SCORE(ALL),ACTUAL,ONE_LEVEL) );
-1873.06 Avg: -169.73
setting SCORE option to ALL.
setting ACTUAL option.
setting ONE_LEVEL option.
maximum area for proto box IDCDSUC is 4606
```

```
[quick]: Number of boxes to process is 906.
[quick]: Number of boxes processed is 0.
-1865.06 Avg: -167.73
[BD-500304]: 52 pins swapped on 30 gates and 0 gates cloned.
[tswap]: Execution time was 5.6 seconds.
          > tc_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),R...
[tc parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc parm]: [set benefit per unit cost]: weight is 4.000000
[tc parm]: =======
*****POU92000-0107US1***** code invocation
[tc parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
          > critical repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPER...
critical( repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPERED_PIN_SWAP) );
-1865.06 Avg: -167.73
maximum area for proto box IDCDSUC is 4606
repower: setting SCORE option to ALL.
repower: setting TAPERED_PIN_SWAP option.
Number of paths is 5
[BD-500278]: (W) Timing inconsistency box C2738
old slack = -1865.0580, new slack = -1866.9469
after reset, slack = -1866.9469
[BD-500278]: (W) Timing inconsistency box C2721rwr
old slack = -1858.8082, new slack = -1863.1361
after reset, slack = -1863.1361
[BD-500278]: (W) Timing inconsistency box C2885
old slack = -1838.0586, new slack = -1843.3768
after reset, slack = -1843.3768
Number of paths is 5
[BD-502005]: The transform 1 reported a slack of--1828.6331, but made the worst slack worse
-1866.9470 from -1865.0580.
                                   Number of paths is 5
[BD-500026]: repower was applied 9 times.
Number of Tapered Cells = 11
[repower]: Execution time was 4.7 seconds.
[BD-502000]: Called transforms 66 times and applied 9 of them.
           > critical repower(SCORE(ALL),NO_VIOLATIONS)
critical( repower(SCORE(ALL),NO_VIOLATIONS) );
-1859.99 Avg: -165.68
maximum area for proto box IDCDSUC is 4654
repower: setting SCORE option to ALL.
repower: setting NO_VIOLATIONS option.
Number of paths is 5
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.2 seconds.
[BD-502000]: Called transforms 24 times and applied 0 of them.
```

```
> critical repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(...
    critical( repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(BETA)) );
    -1859.99 Avg: -165.68
    maximum area for proto box IDCDSUC is 4654
    repower: setting SCORE option to ALL.
    repower: setting NO_VIOLATIONS option.
   Number of paths is 5
   [BD-500026]: repower was applied 7 times.
   [repower]: Execution time was 2.6 seconds.
   [BD-502000]: Called transforms 46 times and applied 7 of them.
               > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFF...
               > noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
   repower: setting SCORE option to ALL.
   repower: setting LOWEST_NOT_EQUAL mode.
   repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -165.35
maximum area for proto box IDCDSUC is 4653
-1859.99 Avg: -165.35
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1859.99 Avg: -164.52
[BD-500026]: repower was applied 12 times.
[repower]: Execution time_was 7.3 seconds.
> tc_parm MARGIN(10000000)
              > compare_critical_slack_limit
   -1859.99 Avg: -164.52
   comparing new slack -1859.9940 to saved slack -1854.3328
            > tc_parm OFFSET(0)
            > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),WE...
   [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
   [tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
   [tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
   [tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
   [tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
            > nextbox tkern
   >>]: nextbox( tkern );
   [tkern]: (W) No AND def - tkern will not apply.
   [tkern]: generated patterns for 0 nets
            > nextbox powerize
   >>]: nextbox( powerize );
   [BD-85000]: Changed power level of 0 patterns, added 0 patterns.
            > quick trecover(SCORE(ALL), RE_POWER, INC, PUSH, SORT_PINS, NO...
```

```
>>]: [quick]:( trecover(SCORE(ALL),RE_POWER,INC,PUSH,SORT_PINS,NO1FAN,NO_VIOLATIONS) );
-1859.99 Avg: -164.52
[trecover]: setting SCORE option to ALL.
[trecover]: setting RE_POWER option.
[trecover]: setting INC mode.
[trecover]: setting PUSH option.
[trecover]: setting SORT_PINS option.
Itrecover]: setting NO1FAN option.
[trecover]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.52
maximum area for proto box IDCDSUC is 4653
-1859.99 Avg: -164.52
Selected 384 critical boxes of 906 total.
[quick]: Number of boxes to process is 384.
[quick]: Number of boxes processed is 0.
-1859.99 Avg: -164.52
Pattern hint flag is inactive
[cleanup]: 0 boxes disconnected
[trecover]: 300 boxes checked 0 recovered
[trecover]: Execution time was 0.0 seconds.
         > reset_critical_slack_limit
-1859.99 Avg: -164.52
resetting the current slack to -1859.9940
         > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
-1859.99 Avg: -164.52
maximum area for proto box IDCDSUC is 4653
setting SCORE option to ALL. setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1859.99 Avg: -164.52
ArrayNum: 6 ArrayMax: 906
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
         > tc parm REGALL
         > repower_paths FUZZY(0.02)
initial slack is -1860
after repower paths slack is -1860
         > critical {repower(SCORE(ALL),INC,NO_VIOLATIONS), repower...
critical( repower(SCORE(ALL),INC,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
 -1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.3 seconds.
```

```
[BD-500026]: repower was applied 0 times.
 [repower]: Execution time was 0.3 seconds.
 [BD-502000]: Called transforms 12 times and applied 0 of them.
         > compare_critical_slack_limit
 -1859.99 Avg: -164.32
 comparing new slack -1859.9940 to saved slack -1841.3940
        > write_end_point_report -points 3 -paths 1
 [ET-0018]: >Begin...New EndPoint Report
        for file /tmp/end_point_report..92476.
 [ET-0019]: <End....New Endpoint Report.
 Sun Apr 18 22:06:39 1999
 Part: IDCDSUC
 Mode: Late Mode / Nominal
                                     EDA EinsTimer EndPoint Report
 Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
 Min. Slack: -1.13427E+38
                                 Max. Slack: 1.13427E+38
 Sort Field: Slack
                               Max. Endpoints: 3
  Cause of Slack
                       Abbreviation Comparison/Description
  Slack Continuation
                                   Slack due to a point downstream on path
                        SlkCont
  Required Arrival Time
                         RAT .
                                 ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
  Asserted Required Arrival Time AssrtRAT
                                       ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 TIME)
  Clock Gating Setup
                         ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                        CIKGHID (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width CIKTPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
Setup
                    Setup ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 ADJUST)
- Hold
                   Hold -
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
 EndOfCycle
                      EndOfC
                                 ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST )
 ClockPulseWidth
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                        CIkPW
TRAILING EDGE )
 ClockSeparation
                        ClkSep
                                  ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
 Loop
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                    ALTest
CLOCK + ADJUST )
 Arrival Time Limiting
                        ATLimit
                                  Slack discontinuity due to failed test
  Num/
                                  LimitedAT/
                                                                    Delay/ Failed Test/
  Test PinName
                                            AT Slack Slew CL FO Cell
                                 E Phase
                                                                           P Func T.Adi
NetName
    1 dcd_succ last t1
                                  R C3+R
                                            2859 -1860 3626 1011 1 PO
                                                                                     0
dcd_succ_last_t1
RAT
                                    999
----> BOX714/OUT
                                   RC3+R
                                             2859 -1860 3626 1011 1 IOPAD
                                                                                 IOPAD
0 dcd_succ_last_t1
----> BOX714/IN
                                 R C3+R
                                           2859 -1860 3626 1011 1 IOPAD
                                                                               IOPAD
0 dcd_succ_last t1&0
```

> C167/y	R C3+R	2859 -1860	3626	1011 1 cs_invvn	01c NOT	
0 dcd_succ_last_t1&0 > C167/a	FC3+R	1079 -1860	30	139 4 cs_invvn	01c NOT	
1780 N675 >{a} C2738/y	F C3+R	1079 -1860	30	139 4 cs_nnd2w	14b NAND	
0 N675 > C2738/a	R C3+R	1057 -1860	36	111 1 cs_nnd2w	14b NAND	
22 last_cycle >{b} C2487/y	R C3+R	1057 -1860	36	111 1 cs_nnd2w	14e NAND	
0 last_cycle > C2487/a	F C3+R	1035 -1860	21	142 3 cs_nnd2w	14e NAND	
23 N1587 > C1952/y	F C3+R	1035 -1860	21	142 3 cs_invvv	19b NOT	0
N1587 > C1952/a	R C3+R	1024 -1860	80	319 1 cs_invvv	19b NOT	
11 num_dcd_cyl&0(1) > BOX679/OUT	R C3-	⊦R 1024 -18	B60	80 319 1 IOPAD	IOPAD	
0 num_dcd_cyl&0(1) > BOX679/IN	R C3+F	1024 -186	i0 8	319 1 IOPAD	IOPAD	0
num_dcd_cyl(1)> num_dcd_cyl(1)	R C3+	R 1024 -18	360	80 319 1 Pl	0	
num dod ovd/1)				·····		
. 🛶 kirisi - mala mata		· •	·	•	4 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	

<del>-</del> - • - • - •	R C3+R 2671 -1672 3658 1011 1 PO 0
iu_reset_op_c_t1	999
> BOX716/OUT	R C3+R 2671 -1672 3658_1011 1 IOPAD IOPAD
0 ju reset op c t1	والمراجع والمناهلة والمناهلة والمناهلة والمناهل والمناهل والمناهل والمناهل والمناهل والمناهل والمناهل والمناهل
> BOX716/IN	R C3+R 2671 -1672 3658 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	D 00 D : :0074 : 4070 : 0000 : 4044 0 co and0n : :000 NAND
. (,,	R:C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0 > C2393/a	F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND
2104 gbfonet_6	1 00+11 500 1072 100 100 0 00_1110211 020 10 100
> gbfocell_6/y	F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6	and the second of the second o
> gbfocell_6/a	R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
77 N2031	
>{b} C2162/y	R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND
0 N2031	F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND
> C2162/b 132 rcvry_reset_q	F C3+N 336 -1072 144 216 3 65_1116511 626 14A165
> rcvry_reset.reg_n.lat_0/l2_out	n F C3+R 358 -1672 144 216 5 cl_invvn 07d
SRL 0 rcvry_reset_q	
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	

```
---->{a} BOX789/v
                                  FC3+R
                                           2922 -1612
                                                      96
                                                          92 3 cs nnd3z 07c NAND
      0 NET1056
      ----> BOX789/a
                                  RC3+R
                                          2862 -1612
                                                      120
                                                          60 NET1054
      ---->{b} BOX785/v
                                  R C3+R
                                           2862 -1612
                                                      120
                                                           32 1 cs_nnd2f 03c NAND
      0 NET1054
      ----> BOX785/a
                                  FC3+R
                                          2781 -1612
                                                     158
                                                          81 N1866
      ---->{c} C2555/y
                                 FC3+R
                                          2781 -1612
                                                     158
                                                          19 1 cs_ao12n 03c AOI
      0 N1866
      ----> C2555/b
                                 RC3+R
                                         2671 -1612
                                                    3658 1044 3 cs_ao12n 03c AOI
      110 iu_reset_op_c_t1&0
      ---->{d} C2393/y
                                 RC3+R
                                          2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
      0 iu_reset_op_c_t1&0
      ----> C2393/a
                                 FC3+R
                                          566 -1672
                                                    109 196 6 cs_nnd2n 02c NAND
      2104 gbfonet 6
      ----> abfocell 6/v
                                 FC3+R
                                          566 -1672
                                                    109
                                                        196 6 cs_invvn 09c NOT
     0 abfonet 6
     ----> gbfocell 6/a
                                 RC3+R
                                          490 -1672
                                                    206
                                                         43 1 cs_invvn .09c NOT
     77 N2031
     ---->{e} C2162/y
                                 RC3+R
                                          490 -1672
                                                         43 1 cs_nnd3n 02c NAND
                                                    206
     0 N2031
     ----> C2162/b
                                 FC3+R
                                         358 -1672 144 216 5 cs_nnd3n 02c NAND
     132 rcvry_reset_q
     ---> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R
                                               358 -1672 144 216 5 cl_invvn 07d
     SRL
             0 rcvry_reset_q
                                R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
          rcvry_reset.reg_n.lat_0/c2
     ---->
198 slow_mode.c2_1
----> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
 0 slow_mode.c2_1
```

```
> hide -no_clear -cells { cs_ao12f cs_ao12g cs_ao12n cs_ao...
```

<sup>&</sup>gt; hide -no\_clear -cells { cs\_ao21n cs\_ao21v cs\_ao22n cs\_ao...

<sup>&</sup>gt; hide -no\_clear -cells { cs\_buffe }

<sup>&</sup>gt; hide -no\_clear -cells { cs\_invvn cs\_invvv }

<sup>&</sup>gt; hide -no\_clear -cells { cs\_nnd2f cs\_nnd2g cs\_nnd2n cs\_nn...

<sup>&</sup>gt; hide -no\_clear -cells { cs\_nnd3f cs\_nnd3g cs\_nnd3h cs\_nn...

<sup>&</sup>gt; hide -no\_clear -cells { cs\_nnd4n cs\_nnd4v }

<sup>&</sup>gt; hide -no\_clear -cells { cs\_nor2f cs\_nor2g cs\_nor2n cs\_no...

<sup>&</sup>gt; hide -no\_clear -cells { cs\_nor3f cs\_nor3g cs\_nor3h cs\_no...

<sup>&</sup>gt; hide -no\_clear -cells { cs\_oa12f cs\_oa12g cs\_oa12n cs\_oa...

<sup>&</sup>gt; hide -no\_clear -cells { cs\_oa21n cs\_oa21v }

<sup>&</sup>gt; hide -no\_clear -cells { cs\_oa22n cs\_oa22v }

<sup>&</sup>gt; hide -no\_clear -cells { cs\_xbn2n cs\_xbn2v }

<sup>&</sup>gt; hide -no\_clear -cells { cs\_xbo2n cs\_xbo2v }

<sup>&</sup>gt; find cell cs\_\*

<sup>&</sup>gt; hide -no\_clear -cells {cs\_ao12f03b cs\_ao12f03c cs\_ao12f0...

<sup>&</sup>gt; find cell cs\_buffe\*

<sup>&</sup>gt; hide -no\_clear -cells {cs\_buffe01a cs\_buffe02a cs\_buffe0...

<sup>&</sup>gt; hide -clear -cells { "cs\_invvn" }

<sup>&</sup>gt; find cell cs\_invvn\*c

<sup>&</sup>gt; hide -clear -cells {cs\_invvn01c cs\_invvn02c cs\_invvn03c ...

<sup>&</sup>gt; hide -clear -cells { "cs\_nnd2n" }

<sup>&</sup>gt; find cell cs nnd2n\*c

```
> hide -clear -cells { "cs_nnd3n" }
        > find cell cs_nnd3n*c
        > hide -clear -cells {cs_nnd3n02c cs_nnd3n03c cs_nnd3n04c ...
        > hide -clear -cells { "cs_nnd4n" }
         > find cell cs nnd4n*c
        > hide -clear -cells {cs nnd4n03c cs_nnd4n04c cs_nnd4n05c ...
        > hide -clear -cells { "cs_nor2n" }
        > find cell cs_nor2n*c
         > hide -clear -cells {cs_nor2n02c cs_nor2n03c cs_nor2n04c ...
         > hide -clear -cells { "cs_nor3n" }
        > find cell cs_nor3n*c
        > hide -clear -cells {cs_nor3n03c cs_nor3n04c cs_nor3n05c ...
         > hide -clear -cells { "cs_ao12n" }
        > find cell cs_ao12n*c
         > hide -clear -cells {cs_ao12n03c cs_ao12n04c cs_ao12n05c ...
         > hide -clear -cells { "cs ao21n" }
         > find cell cs_ao21n*c
         > hide -clear -cells {cs_ao21n03c cs_ao21n04c cs_ao21n05c ...
        > hide -clear -cells { "cs_ao22n" }
> find cell cs_ao22n*c
         > hide -clear -cells {cs_ao22n03c cs_ao22n04c cs_ao22n05c ...
         > hide -clear -cells { "cs_oa12n" }
         > find cell cs_oa12n*c
         > hide -clear -cells {cs_oa12n03c cs_oa12n04c cs_oa12n05c ...
      > hide -clear -cells { "cs_oa21n" }
> find cell cs_oa21n*c
         > hide -clear -cells {cs_oa21n03c cs_oa21n04c cs_oa21n05c ...
         > hide -clear -cells { "cs_oa22n" }
> find cell cs_oa22n*c
        > find cell cs_oa22n*c
      -> hide -clear -cells {cs_oa22n03c cs_oa22n04c cs_oa22n05c ...
         > hide -clear -cells { "cs_buffe" }
       > find cell cs_buffe*
         > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
         > hide -clear -cells { "cs_xbo2n" }
         > find cell cs_xbo2n*c
         > hide -clear -cells {cs_xbo2n01c cs_xbo2n02c cs_xbo2n03c...
         > hide -clear -cells { "cs_xbn2n" }
         > find cell cs_xbn2n*c
         > hide -clear -cells {cs_xbn2n01c cs_xbn2n02c cs_xbn2n03c ...
        > scritflow {trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMP...
[critflow]: trestructure_tree( MAX_INPUTS( 4 ) MAX_DECOMPOSE( 4 ) SORT_PINS CHECK_INPUTS
MIN INPUTS(2))
[Hpattern]: (W) Unable to build pattern for 'AND1 (AND)'
[trestructure]: Thresholds: Inputs=2 Slack=-0.000
[trestructure]: MaxInputs=4 MaxDecompose=4 DoubleInverters=true
[trestructure]: SortPins=true ReduceArea=false
[trestructure]: Checklnputs=true PartialTrees=false
[trestructure]: IgnoreHideFlags=false TibOnly=false
[trestructure]: MatchEffort=2 DebugNet=none
[critflow]: Critical Slack = -1859.994
[padnet]: Added 9 IOPADs.
>>]: nextbox( genmark() );
```

> hide -clear -cells {cs\_nnd2n02c cs\_nnd2n03c cs\_nnd2n04c ...

```
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 24 signals, 14 usage boxes and 22 connections.
[unpadnet]: Removed 9 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                          The model has 13 signals, 3 usage boxes and 11 connections.
[Hdecompose]: Inserted 11 pairs of double inverters.
[cleanup]: 46 boxes disconnected
[sweep]: sweep deleted 35 signals and 8 usage boxes.
                          The model has 20 signals, 10 usage boxes and 18 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input num_dcd_q(1)
[trestructure]: (W) Covering is invalid due to electrical violation at input num dcd a(0)
[trestructure]: (W) Covering is invalid due to electrical violation at input ia_to_if_q
[trestructure]: (W) Covering is invalid due to electrical violation at input mia_to_if_q
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() ):
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                          The model has 22 signals, 14 usage boxes and 20 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 4 boxes disconnected
[sweep]: sweep deleted 4 signals and 0 usage boxes.
                         The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 5 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 32 signals and 2 usage boxes.
```

```
The model has 13 signals, 5 usage boxes and 11 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input ireg_valid&0
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 7 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
finvreml: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 20 signals, 12 usage boxes and 18 connections.
[unpadnet]: Removed 7 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
                         The model has 11 signals, 3 usage boxes and 9 connections.
[Hdecompose]: Inserted 9 pairs of double inverters.
[cleanup]: 50 boxes disconnected
[sweep]: sweep deleted 31 signals and 6 usage boxes.
                         The model has 18 signals, 10 usage boxes and 16 connections.
Itrestructure: (W) Covering is invalid due to electrical-violation at input op_cmp_raw&0
[trestructure]: (W) Covering is invalid due to electrical violation at input frc_blk_1cyc_q
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 3 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 8 signals, 4 usage boxes and 6 connections.
[unpadnet]: Removed 3 IOPADs.
[cleanup]: 0 boxes disconnected
```

```
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 5 signals, 1 usage boxes and 3 connections.
[Hdecompose]: Inserted 3 pairs of double inverters.
[cleanup]: 7 boxes disconnected
[sweep]: sweep deleted 6 signals and 0 usage boxes.
                        The model has 5 signals, 1 usage boxes and 3 connections.
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 4 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: weep deleted 0 signals and 0 usage boxes.
    The model has 12 signals, 7 usage boxes and 10 connections.
[unpadnet]: Removed 4 IOPADs.
Icleanupl: 2 boxes disconnected
[cleanup]: 2 boxes disconnected [sweep]: sweep deleted 2 signals and 0 usage boxes.
The model has 6 signals, 1 usage boxes and 4 connections.
[Hdecompose]: Inserted 4 pairs of double inverters.
[cleanup]: 16 boxes disconnected
[sweep]: sweep deleted 12 signals and 2 usage boxes.
                       The model has 8 signals, 3 usage boxes and 6 connections.
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[padnet]: Added 4 IOPADs.
>>]: nextbox( genmark() );
>>]: nextnet( geninv() );
>>]: nextbox( twoin() onein() invrem() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 14 signals, 9 usage boxes and 12 connections.
[unpadnet]: Removed 4 IOPADs.
[cleanup]: 2 boxes disconnected
[sweep]: sweep deleted 2 signals and 0 usage boxes.
```

```
The model has 8 signals, 3 usage boxes and 6 connections.
[Hdecompose]: Inserted 2 pairs of double inverters.
[cleanup]: 11 boxes disconnected
[sweep]: sweep deleted 8 signals and 5 usage boxes.
                        The model has 10 signals, 5 usage boxes and 8 connections.
[trestructure]: (W) Covering is invalid due to electrical violation at input blk_mcend_q
[ET-0112]: Deleting timing for design: TRESTRUCT, analysis mode:default, and below.
[trestructure]: Rebuilt 0 logic trees
[trestructure]: Execution time was 22.9 seconds.
         > sweep
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1129 signals, 906 usage boxes and 1744 connections.
         > hide -clear -cells { "cs_invvn" }
         > find cell cs_invvn*
         > hide -clear -cells {cs_invvn01b cs_invvn01c cs_invvn01d ...
         > hide -clear -cells { "cs_nnd2n" }
         > find cell cs_ nnd2n*
         > hide -clear -cells {cs_nnd2n02b cs_nnd2n02c cs_nnd2n02d ...
         > hide -clear -cells { "cs_nnd3n" }
> find cell cs_nnd3n*
         > find cell cs_nnd3n*
         > hide -clear -cells {cs_nnd3n02b cs_nnd3n02c cs_nnd3n02d ...
         > hide -clear -cells { "cs_nnd4n" }
> find cell cs_nnd4n*
         > find cell cs_nnd4n*
         > hide -clear -cells {cs_nnd4n03b cs_nnd4n03c cs_nnd4n03d ...
       > hide -clear -cells { "cs_nor2n" }
         > find cell cs_nor2n*
         > hide -clear -cells {cs_nor2n02b cs_nor2n02c cs_nor2n02d ...
         > hide -clear -cells { "cs_nor3n" }
> find cell cs_nor3n*
         > hide -clear -cells {cs_nor3n03b cs_nor3n03c cs_nor3n03d ...
         > hide -clear -cells { "cs_ao12n" }
         > find cell cs_ao12n*
         > hide -clear -cells {cs_ao12n03b cs_ao12n03c cs_ao12n03d ...
         > hide -clear -cells { "cs ao21n" }
         > find cell cs_ao21n*
         > hide -clear -cells {cs_ao21n03b cs_ao21n03c cs_ao21n03d ...
         > hide -clear -cells { "cs_ao22n" }
         > find cell cs_ao22n*
         > hide -clear -cells {cs_ao22n03b cs_ao22n03c cs_ao22n03d ...
         > hide -clear -cells { "cs oa12n" }
         > find cell cs_oa12n*
         > hide -clear -cells {cs_oa12n03b cs_oa12n03c cs_oa12n03d ...
         > hide -clear -cells { "cs_oa21n" }
         > find cell cs_oa21n*
         > hide -clear -cells {cs oa21n03b cs_oa21n03c cs_oa21n03d ...
         > hide -clear -cells { "cs_oa22n" }
         > find cell cs oa22n*
         > hide -clear -cells {cs_oa22n03b cs_oa22n03c cs_oa22n03d ...
         > hide -clear -cells { "cs_buffe" }
         > find cell cs buffe*
         > hide -clear -cells {cs_buffe01a cs_buffe02a cs_buffe03a ...
         > hide -clear -cells { "cs_xbo2n" }
```

> find cell cs\_xbo2n\*

```
> hide -clear -cells {cs_xbo2n01b cs_xbo2n01c cs_xbo2n01d ...
 > hide -clear -cells { "cs_xbn2n" }
 > find cell cs xbn2n*
 > hide -clear -cells {cs_xbn2n01b cs_xbn2n01c cs_xbn2n01d ...
  > hide -clear -cells { cs_ao12f }
  > find cell cs_ao12f*
  > hide -clear -cells {cs_ao12f03b cs_ao12f03c cs_ao12f03d ...
  > hide -clear -cells { cs_nnd2f cs_nnd2w }
  > find cell cs_nnd2f*
  > hide -clear -cells {cs_nnd2f02b cs_nnd2f02c cs_nnd2f02d ...
 > find cell cs nnd2w*
 > hide -clear -cells {cs_nnd2w02b cs_nnd2w02c cs_nnd2w02d ...
 > hide -clear -cells { cs_nnd3f cs_nnd3h cs_nnd3w cs_nnd3y }
 > find cell cs nnd3f*
 > hide -clear -cells {cs_nnd3f02b cs_nnd3f02c cs_nnd3f02d ...
 > find cell cs nnd3h*
 > hide -clear -cells {cs_nnd3h02b cs_nnd3h02c cs_nnd3h02d ...
 > find cell cs_nnd3w*
 > hide -clear -cells {cs_nnd3w02b cs_nnd3w02c cs_nnd3w02d ...
 > find cell cs_nnd3y*
 > hide -clear -cells {cs_nnd3y02b cs_nnd3y02c cs_nnd3y02d ...
 > hide -clear -cells { cs_nor2f cs_nor2w }
 > find cell cs_nor2f*
 > hide -clear -cells {cs_nor2f02b cs_nor2f02c cs_nor2f03b ...
 > find cell cs_nor2w*
 > hide -clear -cells {cs_nor2w02b cs_nor2w02c cs_nor2w02d ...
 > hide -clear -cells { cs_nor3f cs_nor3h }
 > find cell cs nor3f*
 > hide -clear -cells {cs_nor3f03b cs_nor3f03c cs_nor3f03d ...
 > find cell cs_nor3h*
> hide -clear -cells {cs_nor3h03b cs_nor3h03c cs_nor3h03d ...
 > hide -clear -cells { cs_oa12f }
 > find cell cs_oa12f*
 > hide -clear -cells {cs_oa12f03b cs_oa12f03c cs_oa12f03d ...
 > hide -clear -cells { "cs_invvv" }
 > find cell cs_invvv*
 > hide -clear -cells {cs_invvv01b cs_invvv01c cs_invvv01d ...
 > hide -clear -cells { cs_ao12v cs_ao12g }
 > find cell cs_ao12v*
 > hide -clear -cells {cs_ao12v03b cs_ao12v03c cs_ao12v03d ...
 > find cell cs ao12g*
 > hide -clear -cells {cs_ao12g03b cs_ao12g03c cs_ao12g03d ...
 > hide -clear -cells { cs_nnd2v cs_nnd2g cs_nnd2x }
 > find cell cs_nnd2v*
 > hide -clear -cells {cs_nnd2v02b cs_nnd2v02c cs_nnd2v02d ...
 > find cell cs_nnd2g*
 > hide -clear -cells {cs_nnd2g02b cs_nnd2g02c cs_nnd2g02d ...
 > find cell cs_nnd2x*
 > hide -clear -cells {cs_nnd2x02b cs_nnd2x02c cs_nnd2x02d ...
 > hide -clear -cells { cs_nnd3v cs_nnd3g cs_nnd3i cs_nnd3x...
 > find cell cs nnd3v*
 > hide -clear -cells {cs_nnd3v02b cs_nnd3v02c cs_nnd3v02d ...
 > find cell cs nnd3a*
 > hide -clear -cells {cs_nnd3g02b cs_nnd3g02c cs_nnd3g02d ...
 > find cell cs nnd3i*
```

```
> hide -clear -cells {cs nnd3i02b cs_nnd3i02c cs_nnd3i02d ...
          > find cell cs nnd3x*
          > hide -clear -cells {cs_nnd3x02b cs_nnd3x02c cs_nnd3x02d ...
          > find cell cs nnd3z*
          > hide -clear -cells {cs_nnd3z02b cs_nnd3z02c cs_nnd3z02d ...
          > hide -clear -cells { cs_nnd4v }
          > find cell cs_nnd4v*
          > hide -clear -cells {cs_nnd4v03b cs_nnd4v03c cs_nnd4v03d ...
          > hide -clear -cells { cs_nor2v cs_nor2g cs_nor2x }
          > find cell cs nor2v*
          > hide -clear -cells {cs_nor2v02b cs_nor2v02c cs_nor2v02d ...
          > find cell cs_nor2g*
          > hide -clear -cells {cs_nor2g02b cs_nor2g02c cs_nor2g03b ...
          > find cell cs_nor2x*
          > hide -clear -cells {cs_nor2x02b cs_nor2x02c cs_nor2x02d ...
          > hide -clear -cells { cs_nor3v cs_nor3g cs_nor3i }
          > find cell cs_nor3v*
          > hide -clear -cells {cs nor3v03b cs_nor3v03c cs_nor3v03d ...
          > find cell cs nor3a*
          > hide -clear -cells {cs_nor3g03b cs_nor3g03c cs_nor3g03d ...
          > find cell cs nor3i*
          > hide -clear -cells {cs nor3i03b cs_nor3i03c cs_nor3i03d ...
          > hide -clear -cells { cs_oa12v cs_oa12g }
          > find cell cs_oa12v*
          > hide -clear -cells {cs_oa12v03b cs_oa12v03c cs_oa12v03d ...
          > find cell cs oa12g*
         > hide -clear -cells {cs_oa12g03b cs_oa12g03c cs_oa12g03d....
       > tc_parm OFFSET(0)
      > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1)
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
        > critical texpao(SCORE(ALL), PUSH, RE_POWER, FASTEST, SORT_PI...
critical( texpao(SCORE(ALL), PUSH, RE_POWER, FASTEST, SORT_PINS, NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
-1859.99 Avg: -164.32
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[texpao]: applied 0 times
[texpao]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
          > critical texpand(SCORE(ALL),PUSH,RE_POWER,INC,SORT_PINS,...
critical(
texpand(SCORE(ALL), PUSH, RE_POWER, INC, SORT_PINS, SIMILAR, VIEW(TRULE_BASE_AUTOGEN)
,NO_VIOLATIONS));
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
[texpand]: setting SCORE option to ALL.
[texpand]: setting PUSH option.
[texpand]: setting RE_POWER option.
[texpand]: setting INC mode.
```

```
[texpand]: setting SORT_PINS option.
                  [texpand]: setting SIMILAR option.
                  [texpand]: explicit VIEWs used.
                  [texpand]: setting NO_VIOLATIONS option.
                  -1859.99 Avg: -164.32
                  [texpand]: TRULE view TRULE_BASE_AUTOGEN was found.
                  -1859.99 Avg: -164.32
                  ArrayNum: 6 ArrayMax: 906
                  Pattern hint flag is inactive
                  [cleanup]: 0 boxes disconnected
                  [texpand]: Execution time was 0.0 seconds.
                  [BD-502600]: 0 gates checked and 0 expanded.
                  [BD-502000]: Called transforms 6 times and applied 0 of them.
                               > tc parm REGALL
                               > critical repower(SCORE(ALL),INC,NO_VIOLATIONS)
                  critical( repower(SCORE(ALL),INC,NO_VIOLATIONS) );
                  -1859.99 Avg: -164.32
                 maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1859 99 Avg: -164.32
repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
> echo {doing last techredund}

doing last techredund
> traceset {syntrace HOWMANY}
[traceset]: trace string = syntrace HOWMANY
[tracing]: set trace variable syntrace to 20
> str_parm tgfs_effort
> is_parm no_tech_redund
> is_parm remove_redundant_regs
                           > is_parm no_tech_redund
> is_parm remove_redundant_regs
                             > make_constants_in nonreg_only
                           > ignore_trivial_expansions EQNVIEW
                            > expansions_from_tib EQNVIEW
                             > expansions_from_eqn EQNVIEW
                             > copy_def_to_proto EQNVIEW
                             > apply decide boolean(EQNVIEW)
                  generated 1 paths in 70 milliseconds
                           > apply Hstructure(EQNVIEW)
                  generated 1 paths in 30 milliseconds
                           > gen_nonreg_tib_expns TIB_EXPANSIONS
                           > apply Hunstructure()
                           > expandable name
                                  > set_nochange
                                   > constmod
                                  > is_parm keep_bad_pgroups
                                    > bad_pgroups_expandable
                                  > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
                  >>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
                  VIEW(EQNVIEW))):
```

```
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 906 objects as matching keyword criteria.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                      The model has 1129 signals, 906 usage boxes and 1744 connections.
[simple_expand]: Modfied 0 gates.
            > nextbox_with_test {test_key( SYN_H_modified_box ) simpl...
>>]: nextbox_with_test( test_key( SYN_H_modified_box ) simple_expand( PREFIX( HTGFS )
VIEW(TIB_EXPANSIONS)));
>>1: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[BD-354200]: Selected 0 out of 906 objects as matching keyword criteria.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes:
                      The model has 1129 signals, 906 usage boxes and 1744 connections.
[simple_expand]: Modfied 0 gates.
> headless
[headless]: Removed 0 boxes
[sweep]; sweep deleted 0 signals and 0 usage boxes.
                       The model has 1129 signals, 906 usage boxes and 1744 connections.
             > cleanse1
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1129 signals, 906 usage boxes and 1744 connections.
>>1: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1129 signals, 906 usage boxes and 1744 connections.
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
            > nochange
```

```
> set_nochange
         > apply {Hstructure( EQNVIEW TIB_EXPANSIONS)}
generated 1 paths in 60 milliseconds
         > rtolbox {Htgfsredund( 100 )}
>>]: rtolbox( Htgfsredund( 100 ) );
[BD-330500]: Out of 2890 faults found 0 redundancies, eliminated 0, could not decide 0 in 2 seconds.
         > apply Hunstructure()
         > nochange
        > DeleteAllProtosUnderView TIB_EXPANSIONS
[SRULE-17175]: Deleted 5 Proto Boxes
        > randsim q
>>1: randsim(q);
       > randsim q
>>]: randsim( q );
    > copyinfo
> fix_bad_pgroups
824001: Added 0 terminators delicated 6
[BD-82400]: Added 0 terminators, deleted 0 pins and tied 0 pins.
       > basetype
l
>>]: nextbox_with_test( test_syn_hide(!HIDE_MAP),genmark );
[test_syn_hide]: Number of objects selected was 906 of 906 checked.
>>]: nextnet( geninv );
> copyinfo
> nextbox {mapprim, mapterm}
[ >>]: nextbox( mapprim, mapterm ); [mapprim]: Execution time was 0.0 seconds.
[BD-83600]: 0 terminators processed 0 dummy nets removed.
       > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1129 signals, 906 usage boxes and 1744 connections.
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                       The model has 1129 signals, 906 usage boxes and 1744 connections.
[cleanup]: 0 boxes disconnected
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                      The model has 1129 signals, 906 usage boxes and 1744 connections.
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
```

```
[twoin]: Execution time was 0.0 seconds.
       > nextbox tchname(NOERR)
>>1: nextbox( tchname(NOERR) );
NOERR option set
[BD-85300]: Looked at 906 gates, bound 0, 0 had hints.
[tchname]: Execution time was 0.0 seconds.
Pattern hint flag is inactive
       > cleanse
Removed 0 boxes[sweep]: sweep deleted 0 signals and 0 usage boxes.
                      The model has 1129 signals, 906 usage boxes and 1744 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
[BD-40500]: Removed 0 noninverting buffers.
[BD-40501]: Changed 0 gates to inverters.
[onein]: Execution time was 0.0 seconds.
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
[cte]: Removed 0 boxes.
[cte]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                      The model has 1129 signals, 906 usage boxes and 1744 connections.
[sweep]: weep deleted 0 signals and 0 usage boxes.
The model has 1129 signals, 906 usage boxes and 1744 connections.

[
>>]: nextbox( twoin() );
[BD-40550]: Removed 0 redundant pins.
[twoin]: Execution time was 0.0 seconds.
       > has_children CONSTANT
         > tiegen FOLIM(8)
       > tc_parm WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),RE...
[tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
       > compare_key_slack_limit TIME_REDUND
-1859.99 Avg: -164.32
comparing keyed new slack -1859.9940 to keyed saved slack
> reset_key_slack_limit TIME_REDUND
-1859.99 Avg: -164.32
resetting keyed current slack to -1859.9940
         > critical tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS)
critical( tswap(SCORE(ALL),ACTUAL,TWO_LEVEL,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
setting SCORE option to ALL.
setting ACTUAL option.
setting TWO LEVEL option.
```

```
setting NO_VIOLATIONS option.
      -1859.99 Avg: -164.32
      ArrayNum: 6 ArrayMax: 906
      [BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
      [tswap]: Execution time was 0.1 seconds.
      [BD-502000]: Called transforms 6 times and applied 0 of them.
                      > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS)}
     -1859.99 Avg: -164.32
     maximum area for proto box IDCDSUC is 4664
     repower: setting SCORE option to ALL.
     repower: setting INC mode.
     repower: setting NO VIOLATIONS option.
     -1859.99 Avg: -164.32
     ArrayNum: 6 ArrayMax: 906
     [BD-500026]: repower was applied 0 times.
     [repower]: Execution time was 0.0 seconds.
     [BD-502000]: Called transforms 6 times and applied 0 of them.
                   > compare_key_slack_limit TIME_REDUND
     -1859.99 Avg: -164.32
     comparing keyed new slack -1859.9940 to keyed saved slack -1841.3940
                   > delete_key_slack limit TIME REDUND
                   > quick onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
   >>]: [quick]:( onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
                                                and the control of th
   [onebuff]: setting SCORE option to ALL:
[onebuff]: setting RE_POWER option.
    [onebuff]: setting INC mode.
  [onebuff]: setting NO_VIOLATIONS option.
    maximum area for proto box IDCDSUC is 4664
[quick]: Number of boxes to process is 906.
[quick]: Number of boxes processed is 0.
-1859 99 Avg: -164.32
     -1859.99 Avg: -164.32
     [onebuff]: was applied 0 times
               > quick dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS)
     >>]: [quick]:( dinv(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS) );
     -1859.99 Avg: -164.32
      setting SCORE option to ALL.
      setting RE POWER option.
     setting INC mode.
     setting NO_VIOLATIONS option.
     -1859.99 Avg: -164.32
     maximum area for proto box IDCDSUC is 4664
     [quick]: Number of boxes to process is 906.
     [quick]: Number of boxes processed is 0.
     -1859.99 Avg: -164.32
     [BD-500500]: Moved 0 sinks and removed 0 inverters.
                 > critical repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCO...
     repower(SCORE(ALL),INC,NO_VIOLATIONS),clone(SCORE(ALL),ACTUAL,RE_POWER,INC,NO_VIOL
     ATIONS), fantom(LIMITED), faninv(LIMITED));
     -1859.99 Avg: -164.32
```

```
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
setting INC mode.
setting NO_VIOLATIONS option.
fantom: Found 152 valid buffers or inverters.
[BD-500718]: fantom too many buffers and/or inverters 152, may slow down optimizations.
[BD-500704]: (W) No noninverting buffers in technology, serial buffer insertion will not be done.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.0 seconds.
IBD-5001001: 0 parallel copies of gates were made.
[clone]: Execution time was 0.1 seconds.
[BD-500700]: Added 0 buffers.
[fantom]: Execution time was 0.0 seconds.
[BD-500701]: Added 0 inverters.
[faninv]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 24 times and applied 0 of them.
      > nextbox synexpand(XPANDVIEW)
>>]: nextbox( synexpand(XPANDVIEW) );
l >>]: nextbox( SASname(RESTORE) ); [synsasname]: Restored a REVET
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[sweep]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                        The model has 1129 signals, 906 usage boxes and 1744 connections.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names:
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
        > reset_critical_slack_limit
-1859.99 Avg: -164.32
resetting the current slack to -1859.9940
        > critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
setting SCORE option to ALL.
setting ESTIMATED option.
setting TWO_LEVEL option.
setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
Itswapl: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
```

```
> tc_parm REGALL
         > repower_paths FUZZY(0.02)
initial slack is -1860
after repower paths slack is -1860
         > critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS), re...
critical( repower(SCORE(ALL ), INC , NO VIOLATIONS).
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[repower]: Execution time was 0.3 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them
[BD-502000]: Called transforms 12 times and applied 0 of them.

> compare_critical_slack_limit
-1859.99 Avg: -164.32 comparing new slack -1859.9940 to saved slack -1841.3940 > tc_parm {SLEW_LIM(120), CAP_LIM(120), SINK_LIM(120)}
       > tc_parm {SLEW_LIM(120),CAP_LIM(120), SINK_LIM(120)}
> critical onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),...
onebuff(SCORE(ALL),RE_POWER,INC,NO_VIOLATIONS),dinv(SCORE(ALL),RE_POWER,INC,NO_VI
OLATIONS) );
-1859.99 Avg: -164.32
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting INC mode.
[onebuff]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
setting SCORE option to ALL.
setting RE_POWER option.
setting INC mode.
setting NO VIOLATIONS option.
-1859.99 Avg: -164.32
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[onebuff]: was applied 0 times
[BD-500500]: Moved 0 sinks and removed 0 inverters.
[BD-502000]: Called transforms 12 times and applied 0 of them.
       > tc_parm {SLEW_LIM(100), CAP_LIM(100), SINK_LIM(100)}
       > critical clone(SCORE(ALL), ACTUAL, RE_POWER, FASTEST, NO_VIO...
critical( clone(SCORE(ALL), ACTUAL, RE_POWER, FASTEST, NO_VIOLATIONS) );
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
setting SCORE option to ALL.
setting ACTUAL option.
setting RE_POWER option.
```

```
setting FASTEST mode.
setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
ArrayNum: 6 ArrayMax: 906
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
            > pushxor NUM_CLUSTERS(8)
            > write end point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
             for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:08:17 1999
Part: IDCDSUC
                                                                        EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                                                  Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                                                             Max. Endpoints: 3
Sort Field: Slack
                                              Abbreviation Comparison/Description
  Cause of Slack
  Slack Continuation SlkCont
Required Arrival Time RAT
                                                                     Slack due to a point downstream on path
                                                                ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
  Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
                                                                                                                             and the authorized of the state of the state
TIME)
                                                                       ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
  Clock Gating Setup
                                                 ClkGSet
ARRIVAL TIME + ADJUST )
                                                                      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
  Clock Gating Hold
                                                ClkGHld
                                                                          المراوية والأخرافين المحتمد فيها والأفطير وماريا والمراوي المبدر أجراز الأناب المحاربين ليبد ويديا
ARRIVAL TIME + ADJUST)
                                                    CIKTPW: ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
  Clock Tree Pulse Width
TRAILING EDGE)
                                        Setup ---- ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
  Setup
ADJUST)
                                                          ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                                       Hold
  Hold
ADJUST)
                                             EndOfC
                                                                    ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
  EndOfCycle
ADJUST..)...
                                                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                                                 CIkPW
   ClockPulseWidth
 TRAILING EDGE )
                                                                     ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
                                                ClkSep
   ClockSeparation
 ARRIVAL TIME + ADJUST )
                                                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                                        ALTest
  Loop
 CLOCK + ADJUST )
                                                                     Slack discontinuity due to failed test
   Arrival Time Limiting
                                                ATLimit
                                                                                                                                          Delay/ Failed Test/
     Num/
                                                                    LimitedAT/
                                                                                          AT Slack Slew CL FO Cell
                                                                                                                                                         P Func T.Adj
     Test PinName
                                                                    E Phase
 NetName
                                                                                          2859 -1860 3626 1011 1 PO
                                                                                                                                                                             0
                                                                      R C3+R
        1 dcd_succ_last_t1
 dcd_succ_last_t1
                                                                          999
 RAT
                                                                                            2859 -1860 3626 1011 1 IOPAD
                                                                                                                                                                     IOPAD
                                                                       R C3+R
 ----> BOX714/OUT
```

0 dcd\_succ\_last\_t1

> BOX714/IN 0 dcd_succ_last_t1&0	R C3+R	R 2859 -1860 3626 1011 1 IOPAD IOPAD
> C167/y	R C3+R	2859 -1860 3626 1011 1 cs_invvn 01c NOT
0 dcd_succ_last_t1&0 > C167/a 1780 N675	F C3+R	1079 -1860 30 139 4 cs_invvn 01c NOT
>{a} C2738/y 0 N675	FC3+R	1079 -1860 30 139 4 cs_nnd2w 14b NAND
> C2738/a 22 last_cycle	R C3+R	1057 -1860 36 111 1 cs_nnd2w 14b NAND
>{b} C2487/y 0 last_cycle	R C3+R	1057 -1860 36 111 1 cs_nnd2w 14e NAND
> C2487/a 23 N1587	FC3+R	1035 -1860 21 142 3 cs_nnd2w 14e NAND
> C1952/y N1587	F C3+R	1035 -1860 21 142 3 cs_invvv 19b NOT 0
> C1952/a 11 num_dcd_cyl&0(1)	R C3+R	1024 -1860 80 319 1 cs_invvv 19b NOT
> BOX679/OUT	R C3+	R 1024 -1860 80 319 1 IOPAD IOPAD
> BOX679/IN	R C3+R	1024 -1860 80 319 1 IOPAD IOPAD 0
> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+	R 1024 -1860 80 319 1 PI 0

2 iu reset op c t1	R C3+R	2671 -1672 3658 1011 1 PO 0
iu-reset op c t1		و المراجع المر
RAT	999	e de la grafia e de la compartica ferrancia. O fortilla de la compartica del compartica de la compartica de la compartica de la compartica del compartica de la compartica del compartica de la compartica del compartica del compartica de la compartica del compartica de la compartica del compartica d
> BOX716/OUT	R C3+R	R 2671 -1672 3658 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1.		
> BOX716/IN	R C3+R	2671 -1672 3658 1044 3 IOPAD IOPAD
U_lu_reset_op_c_t1&U		And the second s
>{a} C2393/y	R C3+R	2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	•	
> C2393/a	F C3+R	566 -1672 109 196 6 cs_nnd2n 02c NAND
2104 gbfonet_6		The second secon
> gbfocell_6/y	F C3+R	566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6		
> gbfocell_6/a	R C3+R	490 -1672 206 43 1 cs_invvn 09c NOT
77 N2031	5.00.5	400 4000 400 400 400 400 400 400 400 40
>{b} C2162/y	H C3+H	490 -1672 206 43 1 cs_nnd3n 02c NAND
0 N2031	F 00 B	000 1000 111 010 5
> C2162/b	FC3+R	358 -1672 144 216 5 cs_nnd3n 02c NAND
132 rcvry_reset_q	- 50	20. D 050 4070 444 040 5 1 1 07 1
> rcvry_reset.reg_n.lat_0/l2_out	_n FC	C3+R 358 -1672 144 216 5 cl_invvn 07d
SRL 0 rcvry_reset_q	П СО.	400 N/O 00 000 40 d to 07 LODI
> rcvry_reset.reg_n.lat_0/c2	R C3+	+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1> slow_mode.clockblock/c2	B Co	2. 160 N/C 60 000 10 ch all 00 1 LOD
0 slow_mode.c2_1	. n Ca	3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 3low_III0de.02_1	·	

<sup>50</sup> NET1056

	Setup local_milli_t2.reg_n.lat_0/c1	FC	3- 160	60	238 14 cl_invvn	07c
> BOX789/a		F C3+R	2922 -1612	96	92 3 cs_nnd3z	07c NAND
>{b} BOX785/y	> BOX789/a	R C3+R	2862 -1612	120	32 1 cs_nnd3z	07c NAND
> BOX785/a	>{b} BOX785/y	R C3+R	2862 -1612	120	32 1 cs_nnd2f	03c NAND
> (c) C2555/y F C3+R 2781 -1612 158 19 1 cs_ao12n 03c AOI 0 N1866> C2555/b R C3+R 2671 -1612 3658 1044 3 cs_ao12n 03c AOI 110 iu_reset_op_c_t1&0> (d) C2393/y R C3+R 2671 -1672 3658 1044 3 cs_ao12n 02c NAND 0 iu_reset_op_c_t1&0> C2393/a F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND 2104 gbfonet_6> gbfocell_6/y F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT 0 gbfonet_6> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77 N2031> (e) C2162/y R C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset_q R C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q R C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q R C3+R 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1 R C3+R 160 N/C 60 222 13 cb_clk_82_1 LCB 0 slow_mode.c2_1	> BOX785/a	F C3+R	2781 -1612	158	19 1 cs_nnd2f	03c NAND
> C2555/b R C3+R 2671 -1612 3658 1044 3 cs_ao12n 03c AOI 110 iu_reset_op_c_t1&0  >{d} C2393/y R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND 0 iu_reset_op_c_t1&0  > C2393/a F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND 2104 gbfonet_6  > gbfocell_6/y F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT 0 gbfonet_6  > gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77 N2031  >{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031  > C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q  > rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1  > slow_mode.c2_1  > slow_mode.c2_1  > slow_mode.c2_1  > LC2555/b R C3+ 160 N/C 60 222 13 cb_clk_82_1 LCB  > C2162/b R C3+ 160 N/C 60 222 13 cb_clk_82_1 LCB  > R C3+ 160 N/C 60 222 13 cb_clk_82_1 LCB  > R C3+ 160 N/C 60 222 13 cb_clk_82_1 LCB	>{c} C2555/y	F C3+R	2781 -1612	158	19 1 cs_ao12n	03c AOI
>{d} C2393/y R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND 0 iu_reset_op_c_t1&0> C2393/a F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND 2104 gbfonet_6> gbfocell_6/y F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT 0 gbfonet_6> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77 N2031>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND> 132 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> C2555/b	R C3+R	2671 -1612	3658	1044 3 cs_ao12n	03c AOI
> C2393/a	>{d} C2393/y	R C3+R	2671 -1672	3658	1044 3 cs_nnd2r	n 02c NAND
> gbfocell_6/y F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT 0 gbfonet_6> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77 N2031> {e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> C2393/a	F C3+R	566 -1672	109 1	196 6 cs_nnd2n	02c NAND
> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77 N2031>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> gbfocell_6/y	F C3+R	566 -1672	109	196 6 cs_invvn	09c NOT
>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> gbfocell_6/a	R C3+R	490 -1672	206	43 1 cs_invvn (	09c NOT
O N2031> C2162/b	>{e} C2162/y	R C3+R	490 -1672	206	43 1 cs_nnd3n	02c NAND
> rcvry_reset.reg_n.lat_0/l2_out_n	> C2162/b	F C3+R	358 -1672	144 2	216 5 cs_nnd3n	02c NAND ····
> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> rcvry_reset.reg_n.lat_0/l2_out	_n_ F	C3+R 358 -	1672	144 216 5 cl_ii	nvvn 07d
> slow_mode.clockblock/c2 - R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> rcvry_reset.reg_n.lat_0/c2	R C3	3+ 160 N/0	C 60	) 222 13 cl_invvr	07d SRL
	> slow_mode.clockblock/c2 0 slow_mode.c2_1			••		- · · · · · · · · · · · · · · · · · · ·

```
> tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),RELATIVE_OFF...
       > noncritical onebuff(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_...
[onebuff]: setting SCORE option to ALL.
[onebuff]: setting RE_POWER option.
[onebuff]: setting LOWEST mode.
[onebuff]: setting WORST option.
[onebuff]: setting NO_VIOLATIONS option.
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
-1859.99 Avg: -164.32
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1859.99 Avg: -164.32
[onebuff]: was applied 0 times
       > noncritical dinv(SCORE(ALL),RE_POWER,LOWEST,WORST,NO_VIO...
setting SCORE option to ALL.
setting RE_POWER option.
setting LOWEST mode.
setting WORST option.
```

setting NO\_VIOLATIONS option.

```
-1859.99 Avg: -164.32
maximum area for proto box IDCDSUC is 4664
-1859.99 Avg: -164.32
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1859.99 Avg: -164.32
[BD-500500]: Moved 0 sinks and removed 0 inverters.
       > write_end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:08:18 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                    EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                Max. Slack: 1.13427E+38
Sort Field: Slack
                              Max. Endpoints: 3
 Cause of Slack
                       Abbreviation Comparison/Description
 Slack Continuation
                       SlkCont
                                  Slack due to a point downstream on path
 Required Arrival Time
                       RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Asserted Required Arrival Time AssrtRAT
                                       ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
 Clock Gating Setup
                        ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                     CIKGHID (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
Clock Tree Pulse Width
                          CIKTPW: (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
Setup
                    Setup COCK ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST)
 Hold
                            ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                   Hold
ADJUST)
 EndOfCycle
                      EndOfC
                                 ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST)
 ClockPulseWidth
                        ClkPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
                       ClkSep
 ClockSeparation
                                  ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
 Loop
                   ALTest
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST)
 Arrival Time Limiting
                       ATLimit
                                  Slack discontinuity due to failed test
  Num/
                                 LimitedAT/
                                                                   Delay/ Failed Test/
  Test PinName
                                 E Phase
                                            AT Slack Slew CL FO Cell
                                                                           P Func T.Adj
NetName
    1 dcd_succ_last_t1
                                  R C3+R
                                            2859 -1860 3626 1011 1 PO
                                                                                    0
dcd_succ_last_t1
RAT
                                    999
----> BOX714/OUT
                                   R C3+R
                                            2859 -1860 3626 1011 1 IOPAD
                                                                                IOPAD
```

0 dcd\_succ\_last\_t1

> BOX714/IN	R C3+R	2859 -186	0 362	6 1011 1 IOPAD	IOPAD
0 dcd_succ_last_t1&0> C167/y	R C3+R	2859 -1860	3626	1011 1 cs_invvn	01c NOT
0 dcd_succ_last_t1&0 > C167/a	F C3+R	1079 -1860	30	139 4 cs_invvn	01c NOT
1780 N675	F C3+R	1079 -1860	30	139 4 cs_nnd2w	14h NAND
>{a} C2738/y 0 N675					
> C2738/a 22 last_cycle	R C3+R	1057 -1860	36	111 1 cs_nnd2w	14b NAND
>{b} C2487/y	R C3+R	1057 -1860	36	111 1 cs_nnd2w	14e NAND
0 last_cycle > C2487/a	F C3+R	1035 -1860	21	142 3 cs_nnd2w	14e NAND
23 N1587 > C1952/y	F C3+R	1035 -1860	21	142 3 cs_invvv	19b NOT 0
N1587	-				
> C1952/a 11 num_dcd_cyl&0(1) ~	R C3+R			319 1 cs_invvv	• •
> BOX679/OUT 0 num_dcd_cyl&0(1)	R C3	R 1024 -18	360	80 319 1 IOPAD	IOPAD
> BOX679/IN	R C3+R	1024 -186	0 80	319 1 IOPAD	IOPAD 0
num_dcd_cyl(1) > num_dcd_cyl(1)	R C3+	R 1024 -18	860 8	30 319 1 PI	0 -
num_dcd_cyl(1)		1			

or • • • • • • • • • • • • • • • • • • •					
2 iu_reset_op_c_t1	R C3+R	267.1	-1672 36	58 1011 1 PO	
iu_reset_op_c_t1				ag i lina an amang magament	ren i i da ue. Sent
RAT	999			0.00	
> BOX716/OUT	R C3+R	2671	1672 3	658 1011 1 IOPA	DIOPAD
0 iu_reset_op_c_t1		4		este survivo a la marchia	100.0
> BOX716/IN	R C3+R	2671	-1672 365	8 1044 3 IOPAD	IOPAD
0 iu_reset_op_c_t1&0		•			
>{a} C2393/y	R C3+R	2671 -	1672 3658	3 1044 3 cs_nnd2	2n 02c NAND
0 iu_reset_op_c_t1&0					
> C2393/a	F C3+R	566 -16	572 109	196 6 cs_nnd2n	02c NAND
2104 gbfonet_6					
> gbfocell_6/y	F C3+R	566 -10	672 109	196 6 cs_invvn	09c NO1
0 gbfonet_6					
> gbfocell_6/a	R C3+R	490 -1	672 206	43 1 cs_invvn	09c NO1
77 N2031					
>{b} C2162/y	R C3+R	490 -1	672 206	43 1 cs_nnd3n	02c NAND
0 N2031					
> C2162/b	F C3+R	358 -16	672 144	216 5 cs_nnd3n	02c NAND
132 rcvry_reset_q					
> rcvry_reset.reg_n.lat_0/l2_out	_n FC	C3+R	358 -1672	144 216 5 cl_	_invvn 07d
SRL 0 rcvry_reset_q					
> rcvry_reset.reg_n.lat_0/c2	R C3	+ 160	N/C	60 222 13 cl_inv	vn 07d SRL
198 slow_mode.c2_1					
> slow_mode.clockblock/c2	RC	3+ 16	60 N/C	60 222 13 cb_c	ik_32_1 LCB
0 slow_mode.c2_1		•			
***************************************					

<sup>3</sup> local\_milli\_t2.reg\_n.lat\_0/a 50 NET1056

	Setup local_milli_t2.reg_n.lat_0/c1 1200 slow_mode.c1_4	FC	3- 160	60	238 14 cl_invvn	07c
> BOX789/a	>{a} BOX789/y	F C3+R	2922 -1612	96	92 3 cs_nnd3z	07c NAND
>{b} BOX785/y	> BOX789/a	R C3+R	2862 -1612	120	32 1 cs_nnd3z	07c NAND
81 N1866>{c} C2555/y		R C3+R	2862 -1612	120	32 1 cs_nnd2f	03c NAND
0 N1866> C2555/b		F C3+R	2781 -1612	158	19 1 cs_nnd2f	03c NAND
110 iu_reset_op_c_t1&0>{d} C2393/y R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND 0 iu_reset_op_c_t1&0> C2393/a F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND 2104 gbfonet_6> gbfocell_6/y F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT 0 gbfonet_6> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77 N2031>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	0 N1866	F C3+R	2781 -1612	158	19 1 cs_ao12n	03c AOI
2104 gbfonet_6> gbfocell_6/y	110 iu reset on c t180					
2104 gbfonet_6> gbfocell_6/y	>{d} C2393/y 0 iu_reset_op_c_t1&0	R C3+R				
0 gbfonet_6> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT 77_N2031>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	2104 gbfonet_6					
>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset_reg_n.lat_0/l2_out_n F C3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset_reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> gbfocell_6/y 0 gbfonet_6	F C3+R	566 -1672	109 1	96 6 cs_invvn C	9c NOT
0 N2031> C2162/b FC3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_out_n FC3+R 358 -1672 144 216 5 cl_invvn 07d SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1	> gbfocell_6/a 77_N2031	- R C3+R	490 -1672	206	43 1 cs_invvn = 0	9c NOT
> rcvry_reset.reg_n.lat_0/l2_out_n	0 N2021					
SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1						
FU_slow_mode.c2_1	SRL 0 revry reset a				and the second s	
FU_slow_mode.c2_1	198 slow_mode.c2_1	nus	+IOU - IN/C	, 6U	222 13 CI_INVVII.	0/d SHL
	U Slow mode.c2 1		The second second	2. 1,1	and it is the second of the second	_32_1 LCB

> reset\_critical\_slack\_limit

-1859.99 Avg: -164.32

resetting the current slack to -1859.9940

> write\_end\_point\_report -points 5

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end\_point\_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:08:18 1999

Part: IDCDSUC

Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5
Abbreviation Comparison/Description

Cause of Slack Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

TIME)

Clock Gating Setup ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

```
ARRIVAL TIME + ADJUST )
                             ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                    ClkGHld
Clock Gating Hold
ARRIVAL TIME + ADJUST )
                               ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                     CIKTPW
Clock Tree Pulse Width
TRAILING EDGE)
                        ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                Setup
Setup
ADJUST )
                        ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                Hold
Hold
ADJUST )
                            ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                  EndOfC
EndOfCycle
ADJUST)
                    CIKPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
ClockPulseWidth
TRAILING EDGE)
                            ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
                   ClkSep
ClockSeparation
ARRIVAL TIME + ADJUST )
                         ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                ALTest
Loop
CLOCK + ADJUST )
                            Slack discontinuity due to failed test
                  ATLimit
Arrival Time Limiting
                         LimitedAT/ Delay/ Failed Test/
 Num/
                            E Phase AT Slack Slew CL FO Cell
 Test PinName
NetName
2859 -1860 3626-1011 1 PO
                          - R C3+R
  1 dcd succ_last_t1
                            999....
dcd_succ_last_t1
RAT
                          R C3+R 2859 -1860 3626 1011 1 IOPAD
----> BOX714/OUT
0 dcd_succ_last_t1
                          R C3+R 2859 -1860 3626 1011 1 IOPAD IOPAD
----> BOX714/IN
0 dcd succ last t1&0
                        - R C3+R 2859 -1860 3626 1011 1 cs_invvn 01c NOT
----> C167/y
0 dcd succ_last_t1&0
                                   1079 -1860 30 139 4 cs_invvn 01c NOT
                           FC3+R
----> C167/a
1780 N675
                                    1079 -1860
                                                30 139 4 cs nnd2w 14b NAND
                           FC3+R
---->{a} C2738/y
0 N675
                                               36 111 1 cs_nnd2w 14b NAND
                                    1057 -1860
                           R C3+R
----> C2738/a
22 last_cycle
                                               36 111 1 cs_nnd2w 14e NAND
                           R C3+R
                                    1057 -1860
---->{b} C2487/y
0 last_cycle
                                               21 142 3 cs_nnd2w 14e NAND
                                   1035 -1860
                           FC3+R
----> C2487/a
23 N1587
                                               21 142 3 cs_invvv 19b NOT
                           FC3+R
                                   1035 -1860
----> C1952/v
N1587
                                               80 319 1 cs_invvv 19b NOT
                           R C3+R
                                    1024 -1860
----> C1952/a
11 num_dcd_cyl&0(1)
                                                  80 319 1 IOPAD
                                      1024 -1860
                                                                    IOPAD
                              RC3+R
----> BOX679/OUT
0 num_dcd_cyl&0(1)
                                                                   IOPAD
                                     1024 -1860
                                                 80 319 1 IOPAD
                                                                           0
                            R C3+R
----> BOX679/IN
num_dcd_cyl(1)
                                                  80 319 1 PI
                                                                       0
                                      1024 -1860
                              R C3+R
----> num_dcd_cyl(1)
num dcd cyl(1)
```

2 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2671 -1672 3658 1011 1 PO 0
RAT	999
> BOX716/OUT	999 R C3+R 2671 -1672 3658 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	TOTAL TOTAL TOTAL TOTAL
> BOX716/IN	R C3+R 2671 -1672 3658 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	
>{a} C2393/y	R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	F.00 D. 100 100 100 100
> C2393/a 2104 gbfonet_6	F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND
> gbfocell_6/y	F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6	1 00+11 000 -10/2 109 190 0 CS_INVVII 09C NOT
> gbfocell_6/a	R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
77 N2031	
>{b} C2162/y	R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND
0 N2031	F 00 B
> C2162/b 132 rcvry_reset_q	F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND
> rcvrv reset reg. n lat	_n F C3+R 358 -1672 144 216 5 cl_invvn 07d
SHL 0 rcvrv reset a	
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
U slow_mode.c2_1	
	E C2 TP 2022 1610 00 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0
3 local milli t2.reg n.lat 0/a	F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
-50-NET1056	TO THE STREET OF

	132 rcvry_reset_q		200 00000000000000000000000000000000000
	> rcvry_reset.reg_n.lat_0/l2_ou	t_n , F <sub>.</sub> (	C3+R 358 -1672 144 216 5 cl_invvn 07d
	SHL 0 rcvry_reset_q		
	> rcvry_reset.reg_n.lat_0/c2	R C3	+ 160 N/C 60 222 13 cl_invvn 07d SRL
	130 SIUW HIUGE CZ I		
and the second of the second	> slow mode clockblock/c2	· BC	3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	0 slow_mode.c2_1		
	A STATE OF THE STA		TOO 140 00 222 13 CD_CIK_32_1
er e santi	2 local milli t2 rog in lot 0/o	F.CO	R 2922 -1612 96 92 3 cl_invvn 07c SRL
A	50 NET1056	F U3+	H 2922 -1612 96 92 3 cl_invvn 07c SRL
	Setup local milli t2 reg n lat 0/c1	F.C	3- 160 60 238 14 cl_invvn 07c
	1200 slow mode c1 4	1	3° 100° 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,
	>{a} BOX789/v	F C3+R	2922 -1612 96 92 3 cs nnd3z 07c NAND
	0 NET1056		2922 -1612 96 92 3 cs_nnd3z 07c NAND
	0 NET1056 > BOX789/a	R C3+R	2862 -1612 120 32 1 cs_nnd3z 07c NAND
	60 NET1054		2002 1012 120 02 100_inido2 01014/45
	>{b} BOX785/y	R C3+R	2862 -1612 120 32 1 cs_nnd2f 03c NAND
	0 NET1054		
	> BOX785/a	FC3+R	2781 -1612 158 19 1 cs_nnd2f 03c NAND
	81 N1866		
	>{c} C2555/y	F C3+R	2781 -1612 158 19 1 cs_ao12n 03c AOI
	0 N1866		
	> C2555/b	R C3+R	2671 -1612 3658 1044 3 cs_ao12n 03c AOI
	110 iu_reset_op_c_t1&0>{d} C2393/y	D 00 - D	
	>{a} C2393/y 0 iu_reset_op_c_t1&0	R C3+R	2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
•	> C2393/a	F C3+R	500 4070 400 400 0
	2104 gbfonet_6	r US+N	566 -1672 109 196 6 cs_nnd2n 02c NAND
	> gbfocell_6/y	F C3+R	566 -1672 109 196 6 cs_invvn 09c NOT
	0 gbfonet_6	I OUTI	300 -1072 109 190 6 CS_INVVII U9C NO I
	> gbfocell_6/a	R C3+R	490 -1672 206 43 1 cs_invvn 09c NOT
	77 N2031	1. 00	100 1002 200 40 1 05_1110011 030 1401
	>{e} C2162/y	R C3+R	490 -1672 206 43 1 cs_nnd3n 02c NAND
	0 N2031	• • • • • •	100 1012 200 10 1 00_111doi1 020 14/14D
	> C2162/b	F C3+R	358 -1672 144 216 5 cs_nnd3n 02c NAND
	132 rcvry_reset_q		

	> rcvry_reset.reg_n.lat_0/l2_out_n
	4 local_milli_t1.reg_n.lat_0/a F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL 50 NET1056
	Setup local_milli_t1.reg_n.lat_0/c1
	>{a} BOX789/y F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND 0 NET1056
	> BOX789/a R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND 60 NET1054
	>{b} BOX785/y R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND 0 NET1054
	> BOX785/a F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND 81 N1866
	>{c} C2555/y F C3+R 2781 -1612 158 19 1 cs_ao12n 03c AOI 0 N1866
	> C2555/b R C3+R 2671 -1612 3658 1044 3 cs_ao12n 03c AOI 110 iu_reset_op_c_t1&0
	>{d} C2393/y R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
	> C2393/a F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND 2104 gbfonet 6
الموقود المعطوم المواقع المواق المواقع المواقع المواق	> gbfocell_6/y F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT 0 gbfonet_6
	> gbfocell_6/a R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
	>{e} C2162/y R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND 0 N2031
	> C2162/b F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND 132 rcvry_reset_q
	> rcvry_reset.reg_n.lat_0/l2_out_n
	> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1
	> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB 0 slow_mode.c2_1
	50 NET1056 Setup local_milli.reg_n.lat_0/c1
	slow_mode.c1_2 >{a} BOX789/y
	0 NET1056 > BOX789/a R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND
	60 NET1054 >{b} BOX785/y R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND
	0 NÉT1054 > BOX785/a F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND

```
81 N1866
---->{c} C2555/y
                               FC3+R
                                        2781 -1612
                                                    158 19 1 cs_ao12n 03c AOI
0 N1866
----> C2555/b
                               RC3+R
                                        2671 -1612
                                                    3658 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0
---->{d} C2393/v
                               RC3+R
                                         2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0
----> C2393/a
                               FC3+R
                                        566 -1672
                                                    109 196 6 cs_nnd2n 02c NAND
2104 gbfonet_6
----> gbfocell_6/y
                               FC3+R
                                         566 -1672
                                                    109
                                                         196 6 cs_invvn 09c NOT
0 abfonet 6
----> gbfocell_6/a
                               RC3+R
                                         490 -1672
                                                          43 1 cs_invvn 09c NOT
                                                    206
77 N2031
---->{e} C2162/v
                               R C3+R
                                         490 -1672
                                                     206
                                                          43 1 cs_nnd3n 02c NAND
0 N2031
----> C2162/b
                                        358 -1672 144 216 5 cs_nnd3n 02c NAND
                               FC3+R
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2_out_n
                                     FC3+R
                                               358 -1672 144 216 5 cl invvn 07d
SRL
        0 rcvry reset q
----> rcvry_reset.reg_n.lat_0/c2
                                   R C3+ 160 N/C
                                                        60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1
----> __slow_mode.clockblock/c2
                                    R C3+
                                             160 N/C
                                                         60 222 13 cb_clk_32 1 LCB
0 slow_mode.c2_1
 -
> repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}
initial slack is -1860 total pct of low vt boxes initially is 0.6441
box count 621, pct of low vt boxes added is 0.9662
total pct of low vt boxes used is 1.127
after repower paths slack is -1672

> write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
      for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:08:19 1999
Part: IDCDSUC
Mode: Late Mode / Nominal
                                  EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                               Max. Slack: 1.13427E+38
Sort Field: Slack
                            Max. Endpoints: 5
 Cause of Slack
                     Abbreviation Comparison/Description
 Slack Continuation
                      SlkCont
                                Slack due to a point downstream on path
 Required Arrival Time
                       RAT
                                ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Asserted Required Arrival Time AssrtRAT
                                     ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
 Clock Gating Setup
                       ClkGSet
                                 ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                      ClkGHld
                                 ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                        CIKTPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
 Setup
                   Setup
                            ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
```

```
ADJUST)
                           ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                  Hold
 Hold
 ADJUST)
                     EndOfC
                               ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 EndOfCycle
 ADJUST)
                       ClkPW
                                ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 ClockPulseWidth
 TRAILING EDGE)
                                ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ClockSeparation
                      ClkSep
 ARRIVAL TIME + ADJUST )
                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                   ALTest
 Loop
 CLOCK + ADJUST)
                                Slack discontinuity due to failed test
  Arrival Time Limiting
                      ATLimit
                                LimitedAT/
                                                               Delay/ Failed Test/
  Num/
                               E Phase AT Slack Slew CL FO Cell P Func T.Adj
   Test PinName
 NetName
                                         2671 -1672 3658 1011 1 PO
                                R C3+R
    1 iu_reset_op_c_t1
 iu_reset_op_c_t1
                                                       ·, ·· · · · 0
                                  999
 RAT
                                 R C3+R 2671 -1672 3658 1011 1 IOPAD
                                                                            IOPAD
 ----> BOX716/OUT
 0 iu_reset_op_c_t1
                                         2671 -1672 3658 1044 3 IOPAD
                                                                          IOPAD *
----> BOX716/IN
                               RC3+R
 0 iu_reset_op_c_t1&0
                                        2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
 ---->{a} C2393/y
                              R C3+R
 0 iu_reset_op_c_t1&0
                                        566 -1672 109 196 6 cs_nnd2n 02c NAND
 ----> C2393/a
                              F C3+R
                                                        -----
2104 gbfonet_6
                       F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT
 ----> gbfocell_6/y
 0 gbfonet_6
                               R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
 ----> gbfocell_6/a
 77 N2031
                                         490 -1672 206 43 1 cs_nnd3n 02c NAND
                               R C3+R
 ---->{b} C2162/y
 0 N2031
                                        358 -1672 144 216 5 cs_nnd3n 02c NAND
 ----> C2162/b
                              F C3+R
 132 rcvry_reset_q . . .
                                              358 -1672 144 216 5 cl invvn 07d
                                   F C3+R
 ----> rcvry_reset.reg_n.lat_0/l2_out_n
        0 rcvry_reset_q
 SRL
                           R C3+
                                            160 N/C
                                                       60 222 13 cl_invvn 07d SRL
 ----> rcvry_reset.reg_n.lat_0/c2
 198 slow_mode.c2_1
                                             160 N/C
                                                        60 222 13 cb_clk_32_1 LCB
                                    R C3+
 ----> slow_mode.clockblock/c2
 0 slow mode.c2_1
                                 R C3+R
                                          2668 -1669 3294 1011 1 PO
    2 dcd_succ_last_t1
 dcd_succ_last_t1
                                   999
 RAT
                                          2668 -1669 3294 1011 1 IOPAD
                                                                            IOPAD
 ----> BOX714/OUT
                                 R C3+R
 0 dcd_succ_last_t1
                                         2668 -1669 3294 1011 1 IOPAD
                                                                           IOPAD
 ----> BOX714/IN
                                R C3+R
 0 dcd_succ_last_t1&0
                                       2668 -1669 3294 1011 1 cs_invvv 01c NOT
                              R C3+R
 ----> C167/y
 0 dcd_succ_last_t1&0
 ----> C167/a
                              FC3+R
                                       1075 -1669 27 139 4 cs_invvv 01c NOT
```

1594 N675						
>{a} C2738/y	FC3+R	1075 -1669	27	139 4 cs_nnd2x	14b NAND	
0 N675				_		
> C2738/a	R C3+R	1056 -1669	33	114 1 cs_nnd2x	14b NAND	
19 last_cycle			•			
>{b} C2487/y	R C3+R	1056 -1669	33	114 1 cs_nnd2x	14e NAND	
0 last_cycle						
> C2487/a	F C3+R	1035 -1669	22	145 3 cs_nnd2x	14e NAND	
21 N1587						
> C1952/y	FC3+R	1035 -1669	22	145 3 cs_invvv	19b NOT	0
N1587						
> C1952/a	R C3+R	1024 -1669	80	319 1 cs_invvv	19b NOT	
11 num_dcd_cyl&0(1)						
> BOX679/OUT	R C3+	R 1024 -166	59	80 319 1 IOPAD	IOPAD	
0 num_dcd_cyl&0(1)	D 00 D	1001 1000				
> BOX679/IN	R C3+R	1024 -1669	80	319 1 IOPAD	IOPAD	0
num_dcd_cyl(1)	D 00.1	7 4004 400		20 040 4 51		
> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+F	R 1024 -166	9 8	30 319 1.Pl	0	
			•		÷	
and the state of t						

3 local\_milli\_t2.reg\_n.lat\_0/a FC3+R 2922 -1612 96 92 3 cl\_invvn 07c SRL 50 NET1056 Setup local\_milli\_t2.reg\_n.lat\_0/c1 F C3-160 60 238 14 cl invvn 07c 1200 slow\_mode.c1\_4 ---->{a} BOX789/y F C3+R 2922 -1612 96 92 3 cs\_nnd3z 07c NAND 0 NET1056: ----> BOX789/a 2862 -1612 120 32 1 cs\_nnd3z 07c NAND R C3+R 60 NET1054 ---->{b} BOX785/v R:C3+R = 2862 -1612 120 32 1 cs\_nnd2f 03c NAND 0 NET1054 ----> BOX785/a F C3+R 2781 -1612 81 N1866 FC3+R 2781 -1612 158 ---->{c} C2555/y 19 1 cs\_ao12n 03c AOI 0 N1866 ----> C2555/b RC3+R 2671 -1612 3658 1044 3 cs\_ao12n 03c AOI 110 iu\_reset\_op\_c\_t1&0 ---->{d} C2393/y RC3+R 2671 -1672 3658 1044 3 cs\_nnd2n 02c NAND 0 iu\_reset\_op\_c\_t1&0 ----> C2393/a FC3+R 566 -1672 109 2104 gbfonet\_6 ----> gbfocell 6/y FC3+R 566 -1672 109 196 6 cs\_invvn 09c NOT 0 gbfonet 6 ----> gbfocell\_6/a R C3+R 490 -1672 206 43 1 cs\_invvn 09c NOT 77 N2031 ---->{e} C2162/y RC3+R 490 -1672 206 43 1 cs\_nnd3n 02c NAND 0 N2031 ----> C2162/b FC3+R 358 -1672 144 216 5 cs\_nnd3n 02c NAND 132 rcvry\_reset\_q ----> rcvry\_reset.reg\_n.lat\_0/l2\_out\_n FC3+R 358 -1672 144 216 5 cl\_invvn 07d SRL 0 rcvry\_reset\_q ---> rcvry\_reset.reg\_n.lat\_0/c2 R C3+ 160 N/C 222 13 cl\_invvn 07d SRL 198 slow\_mode.c2 1 ----> slow\_mode.clockblock/c2 R C3+ 160 N/C 222 13 cb\_clk\_32\_1 LCB 0 slow\_mode.c2 1

	F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
50 NET1056	
Setup local_milli_t1.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	
>{a} BOX789/y	F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND
0 NET1056	D.O. D. 1010 1010 100 00 1
> BOX789/a	R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND
60 NET1054	D.CO. D. 0060 1610 100 20 1 on and of 020 NAND
>{b} BOX785/y	R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND
0 NET1054	F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND
> BOX785/a	F C3+H 2/81 -1012 130 13 1 C5_find21 00C 14/HD
81 N1866	F C3+R 2781 -1612 158 19 1 cs_ao12n 03c AOI
>{c} C2555/y 0 N1866	1 00+11 2701 1012 100 10 1 05_00121. 000 110.
> C2555/b	R C3+R 2671 -1612 3658 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0	1,00111 2011 1012 0000 1011 0 00_00 1011
>{d} C2393/y	R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	والمراجع والمنافر والمنافر والمنافر والمنافر والمنافر والمنافر والمنافرة والمنافرة والمنافرة والمنافرة والمنافرة
> C2393/a	F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND
2104 gbfonet_6	and the second of the second o
2104 gbfonet_6> gbfocell_6/y	F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6	
> gbfocell_6/a	R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
· 77 N2031	R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT  R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND
>{e} C2162/y	_R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND
0 N2031	5 00 D 050 4070 444 040 5 to med0m 000 NAND
> C2162/b	F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND
	المقارب والرائية والمحارب والموارة ومستستم مراوي والمراوية والمراوية والمراوية والمراوية والمراوية والمتنا
132 rcvry_reset_q	E CO. D. 250 1670 144 216 5 d invent 0.7d
> rcvry_reset.reg_n.iat_0/i2_out	R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND  F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND  n F C3+R 358 -1672 144 216 5 cl_invvn 07d
SRL 0 rcvrv reset a	CIT P COTIT 530 310/2 144 210-0 01 114411 070
SRL 0 rcvry_reset_reg_n.lat_0/i2_out> rcvry_reset_reg_n.lat_0/c2	n F C3+R 358 -1672 144 216 5 cl_invvn 07d R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
SRL 0 rcvry_reset_reg_n.lat_0/c2> rcvry_reset_reg_n.lat_0/c2 198 slow_mode_c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
SRL 0 rcvry_reset.reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
SRL 0 rcvry_reset.reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
SRL 0 rcvry_reset.reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
SRL 0 rcvry_reset.reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
SRL 0 rcvry_reset.reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND
SRL 0 rcvry_reset_reg_n.lat_0/t2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y 0 NET1054	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y 0 NET1054> BOX785/a	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1 5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y 0 NET1054> BOX785/a 81 N1866	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND  F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1     5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y 0 NET1054>{c} BOX785/a 81 N1866>{c} C2555/y	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1     5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y 0 NET1054> BOX785/a 81 N1866>{c} C2555/y 0 N1866	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND  F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND  F C3+R 2781 -1612 158 19 1 cs_ao12n 03c AOI
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND  F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND
SRL 0 rcvry_reset_reg_n.lat_0/i2_out SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2 198 slow_mode.c2_1> slow_mode.clockblock/c2 0 slow_mode.c2_1     5 local_milli.reg_n.lat_0/a 50 NET1056 Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2>{a} BOX789/y 0 NET1056> BOX789/a 60 NET1054>{b} BOX785/y 0 NET1054> BOX785/a 81 N1866>{c} C2555/y 0 N1866	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL  F C3- 160 60 238 14 cl_invvn 07c 1200  F C3+R 2922 -1612 96 92 3 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND  R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND  F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND  F C3+R 2781 -1612 158 19 1 cs_ao12n 03c AOI

```
0 iu_reset_op_c_t1&0
----> C2393/a
                                  FC3+R
                                             566 -1672
                                                          109 196 6 cs_nnd2n 02c NAND
2104 gbfonet 6
 ----> gbfocell_6/y
                                  FC3+R
                                                          109
                                             566 -1672
                                                               196 6 cs_invvn
                                                                               09c NOT
0 abfonet 6
 ----> gbfocell_6/a
                                  RC3+R
                                             490 -1672
                                                          206
                                                                43 1 cs_invvn
                                                                               09c NOT
77 N2031
---->{e} C2162/v
                                  RC3+R
                                             490 -1672
                                                                43 1 cs_nnd3n 02c NAND
                                                          206
0 N2031
----> C2162/b
                                  FC3+R
                                             358 -1672
                                                         144 216 5 cs_nnd3n 02c NAND
132 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/l2 out n
                                         FC3+R
                                                    358 -1672
                                                                144 216 5 cl_invvn 07d
SRL
         0 rcvry_reset_q
      rcvry_reset.reg_n.lat_0/c2
                                       R C3+
                                                 160
                                                       N/C
                                                             60 222 13 cl_invvn 07d SRL
198 slow_mode.c2 1
----> slow mode.clockblock/c2
                                        R C3+
                                                  160 N/C
                                                               60 222 13 cb clk 32 1 LCB
0 slow mode.c2 1
          > compare_critical_slack_limit
-1671.77 Avg: -133.92
comparing new slack -1671.7745 to saved slack -1841.3940
         > reset_critical_slack_limit
-1671.77 Avg: -133.92
resetting the current slack to -1671.7745
        > write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
                 \varphi(G_{\mathcal{A}}, \mathbb{C}) = \{\varphi_{i} = (\mathbb{C}_{i}, \mathbb{C}_{i}) \mid \mathcal{I}_{i} = 1\}
Sun Apr 18 22:08:19 1999
Part : IDCDSUC
                                      Mode: Late Mode / Nominal
                                     EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                  Max. Slack: 1.13427E+38
Sort Field: Slack
                               Max. Endpoints: 5
 Cause of Slack
                        Abbreviation Comparison/Description
 Slack Continuation
                         SIkCont
                                    Slack due to a point downstream on path
 Required Arrival Time
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                         RAT
 Asserted Required Arrival Time AssrtRAT
                                         ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
 Clock Gating Setup
                         ClkGSet
                                    ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                         ClkGHld
                                    ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                           CIKTPW
                                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
 Setup
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
ADJUST)
 Hold
                    Hold
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST)
 EndOfCycle
                       EndOfC
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
 ClockPulseWidth
                         CIkPW
                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
```

**	TRAILING EDGE ) ClockSeparation ClkSep ARRIVAL TIME + ADJUST ) Loop ALTest (I CLOCK + ADJUST ) Arrival Time Limiting ATLimit  Num/ Test PinName NetName	( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2  DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM  Slack discontinuity due to failed test  LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
	iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 2104 gbfonet_6> gbfocell_6/y 0 abfonet_6	R C3+R 2671 -1672 3658 1011 1 PO 0  999 0  R C3+R 2671 -1672 3658 1011 1 IOPAD IOPAD  R C3+R 2671 -1672 3658 1044 3 IOPAD IOPAD  R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND  F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND  F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT  R C3+R - 490 -1672 206 43 1 cs_invvn 09c NOT
	77 N2031 >{b} C2162/y 0 N2031 > C2162/b	R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND  F C3+R 358 -1672 144 216 5 cs_nnd3n 02c NAND  _n F C3+R 358 -1672 144 216 5 cl_invvn 07d  R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL  R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	2 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1594 N675>{a} C2738/y 0 N675> C2738/a 19 last_cycle>{b} C2487/y	R C3+R 2668 -1669 3294 1011 1 PO 0  999 0  R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD  R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD  R C3+R 2668 -1669 3294 1011 1 cs_invvv 01c NOT  F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT  F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND  R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND  R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND

0 last_cycle	
> C2487/a 21 N1587	F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
> C1952/y	F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
N1587	
> C1952/a 11 num_dcd_cyl&0(1)	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
> BOX679/OUT	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1) > BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1)	TOTAL OF THE PROPERTY OF THE P
> num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 PI 0
num_dcd_cyl(1)	
3 local_milli_t2.reg_n.lat_0/a 50 NET1056	F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
Setup local milli t2 reg n let 0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	
>{a} BOX/89/y 0 NET1056	F C3- 160 60 238 14 ci_invvn 0/c  F C3+R 2922 -1612 96 92 3 cs_nnd3z 0/c NAND  B C3+B 2862 -1612 120 32 1 cs_nnd3z 0/c NAND
=	R C3+R 2862 -1612 120 32 1 cs_nnd3z 07c NAND
60 NE11054	
0 NET1054	R C3+R 2862 -1612 120 32 1 cs_nnd2f 03c NAND
> BOX785/a	F C3+R 2781 -1612 158 19 1 cs_nnd2f 03c NAND
81 N1866 >{c} C2555/y	the first transfer of the control of
0 N1866	The state of the s
0 N1866 > C2555/b	R C3+R 2671 -1612 3658 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0 >{d} C2393/y	R C3+R 2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0 > C2393/a	
> C2393/a 2104 gbfonet_6	F C3+R 566 -1672 109 196 6 cs_nnd2n 02c NAND
> gbfocell_6/y	F C3+R 566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6 > gbfocell_6/a	
77 N2031	R C3+R 490 -1672 206 43 1 cs_invvn 09c NOT
>{e} C2162/y	R C3+R 490 -1672 206 43 1 cs_nnd3n 02c NAND
0 N2031 > C2162/b	F C3+R 358 -1672 144 216 5 cs nnd3n 02c NAND
132 rcvry_reset_q	
> rcvry_reset.reg_n.lat_0/l2_out	_n F C3+R 358 -1672 144 216 5 cl_invvn 07d
SRL 0 rcvry_reset_q> rcvry_reset_req_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
4 local_milli_t1.reg_n.lat_0/a 50 NET1056	F C3+R 2922 -1612 96 92 3 cl_invvn 07c SRL
Setup local_milli_t1.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	

>{a} BOX789/y	FC3+R	2922 -1612 96 92 3 cs_nnd3z 07c NAND
0 NET1056		
> BOX789/a	R C3+R	2862 -1612 120 32 1 cs_nnd3z 07c NAND
60 NET1054		0000 4040 400 00 4 middle 000 AIAND
>{b} BOX785/y	R C3+R	2862 -1612 120 32 1 cs_nnd2f 03c NAND
0 NET1054	5 00 D	0704 4040 450 40 4 as model 020 NAND
> BOX785/a	F C3+R	2781 -1612 158 19 1 cs_nnd2f 03c NAND
81 N1866	F C3+R	2781 -1612 158 19 1 cs_ao12n 03c AOI
>{c} C2555/y	F U3+H	2/81 -1012 136 19 1 CS_801211 030 AOI
0 N1866	R C3+R	2671 -1612 3658 1044 3 cs_ao12n 03c AOI
> C2555/b	n Co+n	20/1 -10/2 3000 1044 0 65_40 12/1 000 /10/1
110 iu_reset_op_c_t1&0>{d} C2393/y	R C3+R	2671 -1672 3658 1044 3 cs_nnd2n 02c NAND
0 iu_reset_op_c_t1&0	11 00711	20/1 10/2 0000 1011 0 00
> C2393/a	F C3+R	566 -1672 109 196 6 cs_nnd2n 02c NAND
2104 gbfonet_6		
> gbfocell_6/y	F C3+R	566 -1672 109 196 6 cs_invvn 09c NOT
0 gbfonet_6> gbfocell_6/a	R C3+R	490 -1672 206 43 1 cs_invvn 09c NOT
77 N2031		<del>na kanala da kan</del> ala da kanala da
>{e} C2162/y	R C3+R	490 -1672 206 43 1 cs_nnd3n 02c NAND
 0 N2031		- Control of the Cont
> C2162/b	F C3+R	358 -1672 144 216 5 cs_nnd3n 02c NAND
132 rcvrv reset a	-	こだい かいしょ 14.7 アンドル・アン・ディー・アン・ディー・アン・ディー・ディー・ディー・ディー・ディー・ディー・ディー・ディー・ディー・ディー
		C3+R 358 -1672 144 216 5 cl_invvn 07d
SRL 0 rcvry_reset_q	. B C3	+ 160 N/C 60 222 13 cl_invvn 07d SRL
and the second s		المراجع والمراجع والم
slow_mode_clockblock/c2	: <sub>B</sub> .C	3+ -160 N/C 60 222 13 cb_clk_32_1 LCB
 0 slow mode:c2 1		
 1222-122-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-		
	•	
5 local_milli.reg_n.lat_0/a	F C3+F	2922 -1612 96 92 3 cl_invvn 07c SRL
SU METHOS		
Setup local_milli.reg_n.lat_0/c1	. F C3	- 160 60 238 14 cl_invvn 07c 1200
slow_mode.c1_2		

5 local_milli.reg_n.lat_0/a	F C3+R	2922 -1612	96	92 3 cl_invvn	07c SRL
50 NET1056	* ***		•	238 14 cl_invvn	
Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2	F C3-	160	60	230 14 01_1110011	070 1200
>{a} BOX789/y	FC3+R	2922 -1612	96	92 3 cs_nnd3z	07c NAND
0 NET1056	5.00.5	0000 4040	400	00 4	OZA NIAND
> BOX789/a	R C3+R	2862 -1612	120	32 1 cs_nnd3z	U/C NAND
60 NET1054 >{b} BOX785/y	R C3+R	2862 -1612	120	32 1 cs_nnd2f	03c NAND
0 NET1054					OO NAND
> BOX785/a	F C3+R	2781 -1612	158	19 1 cs_nnd2f	03c NAND
81 N1866 >{c} C2555/y	F C3+R	2781 -1612	158	19 1 cs_ao12n	03c AOI
0 N1866					00 101
> C2555/b	R C3+R	2671 -1612 3	3658	1044 3 cs_ao12r	1 03c AOI
110 iu_reset_op_c_t1&0 >{d} C2393/y	R C3+R	2671 -1672	3658	1044 3 cs_nnd2	n 02c NAND
0 iu_reset_op_c_t1&0					00 11110
> C2393/a	F C3+R	566 -1672 1	109	196 6 cs_nnd2n	02c NAND
2104 gbfonet_6> gbfocell_6/y	F C3+R	566 -1672	109	196 6 cs_invvn	09c NOT
0 gbfonet_6					
> gbfocell_6/a	R C3+R	490 -1672	206	43 1 cs_invvn	09c NOT

```
77 N2031
       ---->{e} C2162/y
                                    R C3+R
                                              490 -1672 206
                                                            43 1 cs nnd3n 02c NAND
       0 N2031
       ----> C2162/b
                                   FC3+R
                                             358 -1672
                                                        144
                                                            216 5 cs nnd3n 02c NAND
       132 rcvry_reset_q
       ----> rcvry_reset.reg_n.lat_0/l2_out_n
                                          FC3+R
                                                   358 -1672
                                                              144 216 5 cl invvn 07d
              0 rcvry_reset_q
                                        R C3+
       ----> rcvry_reset.reg_n.lat_0/c2
                                                160
                                                     N/C
                                                           60 222 13 cl_invvn 07d SRL
      198 slow_mode.c2_1
       ----> slow_mode.clockblock/c2
                                         R C3+
                                                 160
                                                      N/C
                                                            60 222 13 cb clk 32 1 LCB
      0 slow_mode.c2 1
               > repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}
      initial slack is -1672
      total pct of low vt boxes initially is 1.127
      box count 621, pct of low vt boxes added is 20.13
      total pct of low vt boxes used is 5.475
      after repower paths slack is -1669
               > write_end_point_report -points 5
      [ET-0018]: >Begin...New EndPoint Report
            for file /tmp/end_point_report..92476.
      [ET-0019]: <End.....New Endpoint Report.
                      Sun Apr 18 22:08:20 1999
      Part : IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report
     Release Level: 03.01 and Compiled: Wed-Mar 24 22:00:23 1999
      Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38
Abbreviation Comparison/Description
       Cause of Slack
      ......
                         - SlkCont
       Slack Continuation
                                     Slack due to a point downstream on path
                            RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
       Required Arrival Time
                                          ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
       Asserted Required Arrival Time AssrtRAT
      TIME)
       Clock Gating Setup
                            ClkGSet
                                      ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
      ARRIVAL TIME + ADJUST )
       Clock Gating Hold
                            ClkGHld
                                      ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
      ARRIVAL TIME + ADJUST )
       Clock Tree Pulse Width
                              CIKTPW
                                        ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
      TRAILING EDGE)
       Setup
                        Setup
                                 ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
      ADJUST)
       Hold
                        Hold
                                ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
      ADJUST)
       EndOfCycle
                          EndOfC
                                    ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
      ADJUST )
       ClockPulseWidth
                            CIkPW
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
      TRAILING EDGE)
       ClockSeparation
                           ClkSep
                                     ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
      ARRIVAL TIME + ADJUST )
       Loop
                        ALTest
                                 ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
      CLOCK + ADJUST)
       Arrival Time Limiting
                            ATLimit
                                     Slack discontinuity due to failed test
```

Num/ Test PinName NetName	LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
	R C3+R 2668 -1669 3294 1011 1 PO 0
RAT> BOX714/OUT 0 dcd_succ_last_t1	999 R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
> BOX714/IN 0 dcd_succ_last_t1&0	R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
> C167/y 0 dcd_succ_last_t1&0	R C3+R 2668 -1669 3294 1011 1 cs_invvv 01c NOT
> C167/a 1594 N675	F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT
>{a} C2738/y 0 N675	F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND
> C2738/a 19 last_cycle	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND  R C3+R 1056 -1669 33 114 1 cs_nnd2x 14e NAND
>{b} C2487/y 0 last_cycle	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14e NAND F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
> C2487/a 21 N1587 > C1952/y	F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
N1587 > C1952/a	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1) > BOX679/OUT	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD
> BOX679/OUT 0 num_dcd_cyl&0(1) > BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
> BOX679/OUT 0 num_dcd_cyl&0(1)	
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1) 2 iu_reset_op_c_t1	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0 R C3+R 1024 -1669 80 319 1 PI 0
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1) 2 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0 R C3+R 1024 -1669 80 319 1 PI 0  R C3+R 2420 -1421 3327 1011 1 PO 0 999 0
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1) 2 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0 R C3+R 1024 -1669 80 319 1 PI 0  R C3+R 2420 -1421 3327 1011 1 PO 0  999 R C3+R 2420 -1421 3327 1011 1 IOPAD IOPAD
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1) 2 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0> (a) C2393/y 0 iu_reset_op_c_t1&0> C2393/a	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0 R C3+R 1024 -1669 80 319 1 PI 0  R C3+R 2420 -1421 3327 1011 1 PO 0 R C3+R 2420 -1421 3327 1011 1 IOPAD IOPAD R C3+R 2420 -1421 3327 1044 3 IOPAD IOPAD
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)  2 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1875 gbfonet_6> gbfocell_6/y	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0  R C3+R 1024 -1669 80 319 1 PI 0  R C3+R 2420 -1421 3327 1011 1 PO 0  R C3+R 2420 -1421 3327 1011 1 IOPAD IOPAD  R C3+R 2420 -1421 3327 1044 3 IOPAD IOPAD  R C3+R 2420 -1421 3327 1044 3 CS_nnd2v 02c NAND
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)  2 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1875 gbfonet_6> gbfocell_6/y 0 gbfonet_6> gbfocell_6/a	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0  R C3+R 1024 -1669 80 319 1 PI 0  R C3+R 2420 -1421 3327 1011 1 PO 0  R C3+R 2420 -1421 3327 1011 1 IOPAD IOPAD  R C3+R 2420 -1421 3327 1044 3 IOPAD IOPAD  R C3+R 2420 -1421 3327 1044 3 CS_nnd2v 02c NAND  R C3+R 2420 -1421 3327 1044 3 cs_nnd2v 02c NAND  F C3+R 545 -1421 102 196 6 cs_nnd2v 02c NAND  F C3+R 545 -1421 102 196 6 cs_invvv 09c NOT  R C3+R 480 -1421 196 44 1 cs_invvv 09c NOT
> BOX679/OUT 0 num_dcd_cyl&0(1)> BOX679/IN num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)  2 iu_reset_op_c_t1 iu_reset_op_c_t1 RAT> BOX716/OUT 0 iu_reset_op_c_t1> BOX716/IN 0 iu_reset_op_c_t1&0>{a} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1875 gbfonet_6> gbfocell_6/y 0 gbfonet_6	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0 R C3+R 1024 -1669 80 319 1 PI 0  R C3+R 2420 -1421 3327 1011 1 PO 0 R C3+R 2420 -1421 3327 1011 1 IOPAD IOPAD R C3+R 2420 -1421 3327 1044 3 IOPAD IOPAD R C3+R 2420 -1421 3327 1044 3 Cs_nnd2v 02c NAND F C3+R 545 -1421 102 196 6 cs_nnd2v 02c NAND F C3+R 545 -1421 102 196 6 cs_invvv 09c NOT

	122 rcvry_reset_q	
	> rcvry_reset.reg_n.lat_0/l2_out_n	
	SRL 0 rcvry_reset_q	
	> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL	
	198 slow_mode.c2_1	
	> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB	
i	0 slow_mode.c2_1	
	3 local_milli_t2.reg_n.lat_0/a F C3+R 2671 -1361 96 92 3 cl_invvn 07c SRL 50 NET1056	
	Setup local_milli_t2.reg_n.lat_0/c1 F C3- 160 60 238 14 cl_invvn 07c 1200 slow_mode.c1_4	
	>{a} BOX789/y F C3+R 2671 -1361 96 92 3 cs_nnd3z 07c NAND 0 NET1056	
	> BOX789/a R C3+R 2611 -1361 120 32 1 cs_nnd3z 07c NAND 60 NET1054	
	>{b} BOX785/y R C3+R 2611 -1361 120 32 1 cs_nnd2f 03c NAND 0 NET1054	
· · · · · · · · · · · · · · · · · · ·	> BOX785/a F C3+R 2530 -1361 158 19 1 cs_nnd2f 03c NAND	
	81 N1866 >{c} C2555/y F C3+R 2530 -1361 158 19 1 cs_ao12n 03c AOI	
	>{c} C2555/y F C3+R 2530 -1361 158 19 1 cs_ao12n 03c AOI 0 N1866	
an ada you ya a	> C2555/b R C3+R 2420 -1361 3327 1044 3 cs ao12n 03c AOI	
- ·	110 iu reset op c t1&0	, * <u>-</u>
in a second of the second of t	>{d} C2393/y R C3+R 2420 -1421 3327 1044 3 cs_nnd2v 02c NAND	
· ·	U iu_reset_op_c_t1&0	
	> C2393/a F.C3+R 545 -1421 102 196 6 cs_nnd2v 02c NAND 1875 gbfonet_6	, 1777 1 1 2 3 2 1
	> gbfocell_6/y F C3+R 545 -1421 102 196 6 cs_invvv 09c NOT	Land Control
are a second of the second	U QUIONEL 6	
** *** *** *** *** *** *** *** *** ***	> gbfocell_6/a R C3+R 480 -1421 196 44 1 cs_invvv 09c NOT 65 N2031	
	>{e} C2162/y R C3+R 480 -1421 196 44 1 cs_nnd3v 02c NAND 0 N2031	
	> C2162/b F C3+R 358 -1421 144 217 5 cs_nnd3v 02c NAND	
	122 rcvry_reset_q	
	> rcvry_reset.reg_n.lat_0/l2_out_n F C3+R 358 -1421 144 217 5 cl_invvn 07d SRL 0 rcvry_reset_q	•
	> rcvry_reset.reg_n.lat_0/c2 R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1	
	> slow_mode.clockblock/c2 R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB	
	0 slow_mode.c2_1	
	4 local_milli_t1.reg_n.lat_0/a F C3+R 2671 -1361 96 92 3 cl_invvn 07c SRL 50 NET1056	
	Setup local_milli_t1.reg_n.lat_0/c1 F C3- 160 60 238 14 cl_invvn 07c	
	1200 slow_mode.c1_4 >{a} BOX789/y F C3+R 2671 -1361 96 92 3 cs_nnd3z 07c NAND	
	0 NET1056	
	> BOX789/a R C3+R 2611 -1361 120 32 1 cs_nnd3z 07c NAND 60 NET1054	
	>{b} BOX785/y R C3+R 2611 -1361 120 32 1 cs_nnd2f 03c NAND	
	0 NET1054	

> BOX785/a	F C3+R	2530 -1361	158	19 1 cs_nnd2f 03c NAND
81 N1866	F C3+R	2530 -1361	158	19 1 cs_ao12n 03c AOI
>{c} C2555/y 0 N1866	I COTII	2550 -1501	150	13 1 03_001211 0007101
> C2555/b	R C3+R	2420 -1361	3327	1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0		0.400	0007	4044 0
>{d} C2393/y	R C3+R	2420 -1421	3327	1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0 > C2393/a	F C3+R	545 -1421	102	196 6 cs_nnd2v 02c NAND
1875 gbfonet_6				_
> gbfocell_6/y	F C3+R	545 -1421	102	196 6 cs_invvv 09c NOT
0 gbfonet_6	R C3+R	480 -1421	106	44 1 cs_invvv 09c NOT
> gbfocell_6/a 65 N2031	n Co+n	400 -1421	130	44 1 C3_#IVVV
>{e} C2162/y	R C3+R	480 -1421	196	44 1 cs_nnd3v 02c NAND
0 N2031	5.00 B	050 4404	444	047 F an maddy 000 NAND
> C2162/b 122 rcvry_reset_q	F C3+R	358 -1421	144	217 5 cs_nnd3v
> rcvry_reset.reg_n.lat_0/l2_ou	tn F	C3+R 358	-1421	144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q				
> rcvry_reset.reg_n.lat_0/c2	R C	3+ 160 N	/C 6	0 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1> slow_mode.clockblock/c2	- R (	C3+ 160 I	N/C	60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1				

	0 slow_mode.c2_1						
	5 local_milli.reg_n.lat_0/a			· .			
	5 local_milli.reg_n.lat_0/a	F C3+R	2671 -136	1 96	92 3 cl_invvn	07c SRL	•
	50 NET1056						
	Setup local_milli.reg_n.lat_0/c1	FC3	- 160	60 2	238 14 cl_invvn	07c 1200	
· · · · · · · · · · · · · · · · · · ·	slow_mode.c1_2						
* • : ·	>{a} BOX789/y	F C3+R	2671 -1361	96	92 3 cs_nnd3z	U/C NAND	The strate of the second
-	0 NET1056		0044 4004		00.4	OZ- NIAND	
<u>.</u>	> BOX789/a	R C3+R	2611 -1361	. 120	32 1 cs_nnd3z	U/C NAND	
	60 NET1054		0044 4004	400	00 4	OO NAND	
	>{b} BOX785/y	R C3+R	2611 -1361	120	32 1 cs_nnd2f	03C NAND	
	0 NET1054	F 00 - D	0500 4004	150	10 1 as mad0f	OOO NIAND	
	> BOX785/a	F C3+R	25 <u>3</u> 30 -1361	158	19 1 cs_nnd2f	03C IVAIND	•
	81 N1866	E 00. B	0000 1061	150	10 1 00 00100	020 401	
	>{c} C2555/y	F C3+R	2530 -1361	156	19 1 cs_ao12n	USC AOI	
	0 N1866	D CO. D	0400 1061	2227 1	044 3 cs_ao12r	020 AOI	
	> C2555/b	R C3+R	2420 -1301	3321 1	044 3 CS_a0121	1 03C AOI	
	110 iu_reset_op_c_t1&0	R C3+R	2420 1421	2227	1044 3 cs_nnd2	V O20 NAND	
	>{d} C2393/y	n Co+n	2420 -1421	3321	1044 3 CS_111102	V UZC IVAND	
	0 iu_reset_op_c_t1&0	F C3+R	545 -1421	102 10	96 6 cs_nnd2v	OSC NIAND	
	> C2393/a	r Co+n	343 -1421	102 18	o o cs_iiiuzv	UZC IVAND	•
	1875 gbfonet_6	F C3+R	EAE 1401	102 1	96 6 cs_invvv	OOO NOT	
	> gbfocell_6/y	r Co+n	343 -1421	102 1	90 0 C3_11VVV	030 110 1	
	0 gbfonet_6	R C3+R	480 -1421	106	44 1 cs_invvv	noc NOT	
	> gbfocell_6/a 65 N2031	n Co+n	400 -1421	130 .	++ 1 C3_IIIVVV	0901101	
		R C3+R	490 <sub>-</sub> 1421	106	44 1 cs_nnd3v	O2c NAND	
	>{e} C2162/y	II COTII	400: 1421	130	++ 1 C3_1111GOV	OZOTANIO	
	0 N2031 > C2162/b	F C3+R	358 -1421	144 2	17 5 cs_nnd3v	O2c NAND	
		i Cotii	000 -1421	177 6	., 5 05_\\\\\	02011/110	
	122 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_ou	ıtın E	C3_B 358	-1421	144 217 5 cl_i	inwn 07d	
	> icvry_reset.reg_mat_0/12_00	ii_ii   1 '	00711 000	1761	141 217 301_	1117411 0/0	

```
SRL
         0 rcvry_reset_q
 ----> rcvry_reset.reg_n.lat_0/c2
                                      R C3+
                                                160
                                                      N/C
                                                             60 222 13 cl_invvn 07d SRL
 198 slow_mode.c2_1
 ----> slow_mode.clockblock/c2
                                       R C3+
                                                  160
                                                       N/C
                                                              60 222 13 cb_clk_32_1 LCB
 0 slow mode.c2 1
          > compare_critical slack limit
 -1669.49 Avg: -124.51
 comparing new slack -1669.4933 to saved slack -1655.0568
         > traceset {repower_paths HOWMANY}
 [traceset]: trace string = repower_paths HOWMANY
 [tracing]: set trace variable repower_paths to 20
          > reset_critical_slack_limit
 -1669.49 Avg: -124.51
 resetting the current slack to -1669.4933
          > quick tswap(SCORE(ALL),ACTUAL,ONE_LEVEL)
 >>]: [quick]:( tswap(SCORE(ALL),ACTUAL,ONE_LEVEL) );
 -1669.49 Avg: -124.51
 setting SCORE option to ALL.
setting ACTUAL option.
setting ONE_LEVEL option.
maximum area for proto box IDCDSUC is 4664
[quick]: Number of boxes to process is 906.
[quick]: Number of boxes processed is 0.
-1669.49 Avg: -124.48
-1669.49 Avg: -124.48
-1009.49 Avg: -124.48 [BD-500304]: 35 pins swapped on 22 gates and 0 gates cloned.
                                      [tswap]: Execution time was 5.7 seconds.
          > to_parm {WEIGHTED_BENEFIT(1),ATTEMPTS(1),ITERATIONS(1),R...
 [tc_parm]: [set_benefit_per_unit_cost]: unit cost is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: benefit_units is 0.000172
[tc_parm]: [set_benefit_per_unit_cost]: benefit is 1.000000
[tc_parm]: [set_benefit_per_unit_cost]: weight is 4.000000
[tc_parm]: [set_benefit_per_unit_cost]: calculated margin is 6.090000
          > critical repower(SCORE(ALL),REPOWER_GROUP(TAPERED),TAPER...
critical( repower(SCORE(ALL), REPOWER_GROUP(TAPERED), TAPERED_PIN_SWAP) );
-1669.49 Avg: -124.48
maximum area for proto box IDCDSUC is 4664
repower: setting SCORE option to ALL.
repower: setting TAPERED_PIN_SWAP option.
Number of paths is 5
[BD-500026]: repower was applied 3 times.
Number of Tapered Cells = 14
[repower]: Execution time was 0.8 seconds.
[BD-502000]: Called transforms 30 times and applied 3 of them.
          > critical repower(SCORE(ALL),NO_VIOLATIONS)
critical( repower(SCORE(ALL),NO_VIOLATIONS) );
-1669.49 Avg: -125.12
maximum area for proto box IDCDSUC is 4671
```

```
repower: setting SCORE option to ALL.
repower: setting NO_VIOLATIONS option.
Number of paths is 5
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 27 times and applied 0 of them.
          > critical repower(SCORE(ALL),NO_VIOLATIONS,REPOWER_GROUP(...
critical( repower(SCORE(ALL), NO_VIOLATIONS, REPOWER_GROUP(BETA)) );
-1669.49 Avg: -125.12
maximum area for proto box IDCDSUC is 4671
repower: setting SCORE option to ALL.
repower: setting NO_VIOLATIONS option.
Number of paths is 5
Number of paths is 5
[BD-500026]: repower was applied 1 times.
[repower]: Execution time was 1.0 seconds.
[BD-502000]: Called transforms 27 times and applied 1 of them.
           > tc_parm MARGIN(0),ATTEMPTS(1),ITERATIONS(1),ABSOLUTE_OFF...
           > noncritical repower(SCORE(ALL),LOWEST_NOT_EQUAL,NO_VIOLA...
repower: setting SCORE option to ALL.
                                         ...
repower: setting LOWEST_NOT_EQUAL mode.
repower: setting NO_VIOLATIONS option.
-1669.49 Avg: -125.32
maximum area for proto box IDCDSUC is 4675
-1669.49 Avg: -125.32
[noncritical]: noncritical applied to boxes with slack > 0.00
[noncritical]: Number of boxes to process is 906.
[noncritical]: Number of boxes processed is 0.
-1669.49 Avg: -125.31
IBD-5000261; repower was applied 1 times.
[repower]: Execution time was 7.7 seconds.
           > tc_parm_MARGIN(10000000)
           > compare critical slack_limit
-1669.49 Avg: -125.31
comparing new slack -1669.4933 to saved slack -1652.7983
           > reset critical slack_limit
-1669.49 Avg: -125.31
resetting the current slack to -1669.4933
           > write end point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
        for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
 Sun Apr 18 22:08:37 1999
 Part: IDCDSUC
                                        EDA EinsTimer EndPoint Report
 Mode: Late Mode / Nominal
 Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                     Max. Slack: 1.13427E+38
 Min. Slack: -1.13427E+38
                                  Max. Endpoints: 5
 Sort Field: Slack
                          Abbreviation Comparison/Description
  Cause of Slack
                                      Slack due to a point downstream on path
  Slack Continuation
                           SlkCont
                                      ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
  Required Arrival Time
                           RAT
                                           ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
  Asserted Required Arrival Time AssrtRAT
```

TIME)

```
Clock Gating Setup
                                                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                                                 ClkGSet
  ARRIVAL TIME + ADJUST )
    Clock Gating Hold
                                                ClkGHld
                                                                    ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
  ARRIVAL TIME + ADJUST )
    Clock Tree Pulse Width
                                                   CIKTPW
                                                                         ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
  TRAILING EDGE)
    Setup
                                        Setup
                                                          ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
  ADJUST )
    Hold
                                      Hold
                                                        ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
  ADJUST )
    EndOfCycle
                                            EndOfC
                                                                 ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
  ADJUST)
    ClockPulseWidth
                                                ClkPW
                                                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
  TRAILING EDGE )
    ClockSeparation
                                               ClkSep
                                                                  ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
  ARRIVAL TIME + ADJUST )
    Loop
                                       ALTest
                                                           ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
  CLOCK + ADJUST )

    Arrival Time Limiting

                                               ATLimit -
                                                                  Slack discontinuity due to failed test
      Num/
                                                                                                                 Delay/ Fäiled Test/
                                                                  LimitedAT/
                                                                                      AT Slack Slew CL FO Cell
      Test PinName
                                                                 E Phase
                                                                                                                                                 P Func T.Adj
  NetName
                                                                                                     and the second of the second o
   1 dcd_succ_last_t1
                                                                   RC3+R
                                                                                      2668 -1669 3294 1011 1 PO
 dcd_succ_last_t1
  RAT
                                                             999
                                                     R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
 ----> BOX714/OUT
  0 dcd_succ_last_t1
  ----> BOX714/IN
                                                             R C3+R
                                                                                    2668 -1669 3294 1011 1 IOPAD
                                                                                                                                                         IOPAD
  0 dcd_succ_last_t1&0
  ----> C167/v
                                                             RC3+R
                                                                                2668 -1669
                                                                                                        3294 1011 1 cs_invvv 01c NOT
  0 dcd_succ_last_t1&0
  ----> .C167/a
                                                              FC3+R
                                                                                1075 -1669
                                                                                                          27 139 4 cs_invvv 01c NOT
  1594 N675
  ---->{a} C2738/v
                                                                FC3+R
                                                                                  1075 -1669
                                                                                                            27 139 4 cs_nnd2x 14b NAND
 0 N675
  ----> C2738/a
                                                              R C3+R
                                                                                  1056 -1669
                                                                                                           33 114 1 cs_nnd2x 14b NAND
  19 last_cycle
  ---->{b} C2487/y
                                                                RC3+R
                                                                                  1056 -1669
                                                                                                            33 114 1 cs nnd2x 14e NAND
 0 last_cycle
  ----> C2487/a
                                                              FC3+R
                                                                                 1035 -1669
                                                                                                           22 145 3 cs_nnd2x 14e NAND
  21 N1587
  ----> C1952/v
                                                              FC3+R
                                                                                                           22 145 3 cs_invvv 19b NOT
                                                                                 1035 -1669
                                                                                                                                                                       0
  N1587
  ----> C1952/a
                                                              R C3+R
                                                                                 1024 -1669
                                                                                                           80 319 1 cs_invvv 19b NOT
  11 num_dcd_cyl&0(1)
  ----> BOX679/OUT
                                                                    RC3+R
                                                                                       1024 -1669
                                                                                                                 80 319 1 IOPAD
                                                                                                                                                         IOPAD
 0 num_dcd_cyl&0(1)
  ----> BOX679/IN
                                                                 R C3+R
                                                                                    1024 -1669
                                                                                                              80 319 1 IOPAD
                                                                                                                                                     IOPAD
                                                                                                                                                                       0
 num_dcd_cyl(1)
  ----> num_dcd_cyl(1)
                                                                   R C3+R
                                                                                      1024 -1669
                                                                                                                80 319 1 PI
  num_dcd_cyl(1)
```

2 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO 0
iu_reset_op_c_t1	000
RAT	999 0
	R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
	H C3+H 2399 -1400 3310 1044 310FAD 10FAD
0 iu_reset_op_c_t1&0	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
>{a} C2393/y 0 iu_reset_op_c_t1&0	N C3+11 2393 1400 3010 1044 0 03_111024 02010/100
> C2393/a	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6	1 00111 000 1100 100 100 0 00a.
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 abfonet 6	_
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
EA NOO21	
>{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
	• *
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvrv reset o	
	out_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL -R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
> rcvry_reset.reg_n.lat_0/c2	H C3+ 160 N/C 60 222 13 CI_INVII U/U SHL
198 slow_mode.c2_1	P.C2: 160 N/C 60 222 13 ch clk 32 1 LCB
> Slow_mode.clockblock/c2	-n C3+ 100 14/C 00 222 13 CD_CIK_02_1 EOD
U Slow_IIIode.cz_1	
e subsection of the second control of the se	والمتطبيقين والتورفي والمنطب الطبيعين فالخاجم جحاجه والعبوا المنتج الحالج الماليان المناسب الواريد وأرأن والمنا
- 3 ded suce last t1	F C3+R 2354 -1355 1874 1011 1 PO 0  999 0  F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
ded succ last t1	
RAT	999
> BOX714/OUT	F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
U dcd succ last ti	
> BOX714/IN	F C3+R 2354 -1355 1874 1011 1 IOPAD TOPAD
0 dcd_succ_last_t1&0	F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT
> C167/y	F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT
0 000_0000_1001_1100	
> C10//a	R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT
1208 N675	D 00 D 4440 4055 60 400 4 oo nod0y 14b NAND
,	R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND
0 N675	F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND
> C2738/b	P C3+N 1097 -1333 04 170 3 65_11102X 14014/140
49 N1692	F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND
>{b} C2725rwr/y	
0 N1602	1 00111 1007 1000 of 110 o oca_g
0 N1692	
> C2725rwr/a	R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND
> C2725rwr/a 46 N1479	R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND
> C2725rwr/a 46 N1479 >{c} C2721rwr/y	
> C2725rwr/a 46 N1479 >{c} C2721rwr/y 0 N1479	R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND
> C2725rwr/a 46 N1479 >{c} C2721rwr/y	R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd3i 11b NAND

F C3+R

R C3+R

---->{d} C2338/y

----> C2338/a 24 N1119

0 N892

983 -1355 36 113 2 cs\_nnd2x 14c NAND

959 -1355 71 159 3 cs\_nnd2x 14c NAND

	> C2905/y 1119	R C3+R	959 -1355	71	159 3 cs_in	vvv 12b l	TOP	0	
	> C2905/a	F C3+R	915 -1355	59	76 1 cs_inv	vv 12b N	OT 4	45	•
	2010 >{e} C2906/y	F C3+R	915 -1355	59	76 1 cs_nc	or2g 12e	NOR		
	N2010 > C2906/b	R C3+R	868 -1355	80	124 1 cs_nc	or2a 12e	NOR		
47	7 dcd_blk_dsucc&0 > BOX644/OUT	R C3+F			30 124 1 IC				
0	dcd_blk_dsucc&0						IOPAD		
do	> BOX644/IN cd_blk_dsucc	R C3+R	868 -1355	80	124 1 IOP	AD IC	PAD	0	
	> dcd_blk_dsucc cd_blk_dsucc	R C3+R	868 -1355	80	) 124 1 PI		0		
		~~~~~~~							
50	4 local_milli_t2.reg_n.lat_0/a ) NET1056	F C3+F	R 2650 -134	10	96 92 3 cl	l_invvn 0	7c SRL		
	etup local_milli_t2.reg_n.lat_0/c1 200_slow_mode.c1_4	F C	3- 160	60	) 238 14 cl_	_invvn 07	C -		
		F C3+R	2650 -1340	96	92 3 cs_i	nnd3z 07	c NAND		
	> BOX789/a	R C3+R	2590 -1340	120	) 32 1 cs_i	nnd3z 07	c NAND		- · · · -
	) NET1054 >{b} BOX785/y	R C3+R	2590 -1340	120	0 32 1 cs_	_nnd2f 03	c NAND		
	NE11054 > BOX785/a		2510 -1340	158	19 1 cs_r	nnd2f 03d	NAND	•	
181	N1866 >{c} C2555/y				The contract of the contract o	are an area of the second			
·. 0	N1866		2399 -1340		· .			-	
	iu_reset_op_c_t1&u	1,11			5 - F - F - F - F - F - F - F - F - F -	4. 7			The second secon
0	iu_reset_op_c_t1&0		•		· ·				_
18	363 gbfonet_6	F C3+R	536 -1400	100	196 6 cs_nr	nd2v 02c	NAND	e î	
0	-> gbfocell_6/y gbfonet_6	F C3+R	536 -1400	100	196 6 cs_in	vvv 09c i	TON		
	-> gbfocell_6/a N2031	R C3+R	472 -1400	184	44 1 cs_in	vvv 09c 1	TON		
	>{e} C2162/y N2031	R C3+R	472 -1400	184	44 1 cs_nr	nd3v 02c	NAND		
	-> C2162/a	F C3+R	358 -1400	144	217 5 cs_nr	nd3v 02c	NAND		
	4 rcvry_reset_q -> rcvry_reset.reg_n.lat_0/l2_out_	n FC	3+R 358 -	1400	144 217	5 cl_invvn	07d		
	RL 0 rcvry_reset_q -> rcvry_reset.reg_n.lat_0/c2	R C3+	- 160 N/C	6	0 222 13 cl	l invvn 0	7d SRL		
	98 slow_mode.c2_1 -> slow_mode.clockblock/c2	R C3			60 222 13				
	slow_mode.c2_1		•				_1 LOB		
							_		
	5 local_milli_t1.reg_n.lat_0/a NET1056	F C3+F		0 9	96 92 3 cl <sub>.</sub>	_invvn 07	c SRL		
Se	etup local_milli_t1.reg_n.lat_0/c1	FC3	- 160	60	238 14 cl_	invvn 07d			,

```
1200 slow_mode.c1_4
                                                            92 3 cs_nnd3z 07c NAND
                                 FC3+R
                                          2650 -1340
                                                       96
 ---->{a} BOX789/y
 0 NET1056
                                                      120
                                                            32 1 cs_nnd3z 07c NAND
                                          2590 -1340
                                R C3+R
 ----> BOX789/a
 60 NET1054
                                                            120
                                 R C3+R
                                          2590 -1340
 ---->{b} BOX785/y
 0 NET1054
                                                            FC3+R
                                         2510 -1340
                                                      158
 ----> BOX785/a
 81 N1866
                                                           158
                                FC3+R
                                         2510 -1340
 ---->{c} C2555/y
 0 N1866
                                         2399 -1340 3318 1044 3 cs_ao12n 03c AOI
                               RC3+R
 ----> C2555/b
 110 iu_reset_op_c_t1&0
                                         2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
                                RC3+R
 ---->{d} C2393/y
 0 iu_reset_op_c_t1&0
                                                     100 196 6 cs_nnd2v 02c NAND
                                         536 -1400
                                FC3+R
 ----> C2393/a
 1863 qbfonet_6
                                                     100 196 6 cs_invvv 09c NOT
                                         536 -1400
                                FC3+R
 ----> gbfocell_6/y
 0 qbfonet_6
                                          472 -1400
                                                           44 1 cs_invvv....09c NOT
                                                     184
 ----> -gbfocell_6/a
                                R C3+R
 64 N2031
                                          472 -1400 184
                                                           44 1 cs_nnd3v 02c NAND
                                R C3+R
 ---->{e} C2162/y
 0 N2031
 ----> C2162/a
                                                     144 217 5 cs_nnd3v 02c NAND
                        F-C3+R 358 -1400
 114 rcvry_reset_q
 ----> rcvry_reset.reg_n.lat_0/l2_out_n F-C3+R
                                                358 -1400
                                                          144 217 5 cl invvn 07d
 SRL 0 rcvry_reset_q ----> rcvry_reset.reg_n.lat_0/c2 ----> R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL 198 slow_mode.c2_1
 ----> slow_mode.clockblock/c2
                                              160 N/C 60 222 13 cb_clk_32_1 LCB
                                     R C3+
                                             عبها والمناف المتاريخ والمنافي والمناف والمناف والمنافي والمناف والمناف والمناف والمناف والمناف والمناف والمناف
0 slow_mode.c2_1
```

> repower\_paths {FUZZY(0.02), LOWVT, NUM\_CLUSTERS(16)}

initial slack is -1669

total pct of low vt boxes initially is 5.475

box count 621, pct of low vt boxes added is 19.65....

total pct of low vt boxes used is 5.475

after repower paths slack is -1669

> write\_end\_point\_report -points 5

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end\_point\_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:08:37 1999

Part: IDCDSUC

Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 5

Cause of Slack Abbreviation

Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path

Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)

Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

```
TIME)
  Clock Gating Setup
                        ClkGSet
                                  ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 ARRIVAL TIME + ADJUST )
  Clock Gating Hold
                       ClkGHld
                                 ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 ARRIVAL TIME + ADJUST )
  Clock Tree Pulse Width
                         CIKTPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE )
  Setup
                   Setup
                            ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 ADJUST)
  Hold
                   Hold
                           ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
  EndOfCycle
                      EndOfC
                                ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
  ClockPulseWidth
                       ClkPW
                                 ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
  ClockSeparation
                      ClkSep
                                ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST )
  Loop
                   ALTest
                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
 CLOCK + ADJUST )
  Arrival Time Limiting
                      ATLimit
                                Slack discontinuity due to failed test
   Num/
                                LimitedAT/
                                                               Delay/ Failed Test/
   Test PinName
                               E Phase AT Slack Slew CL FO Cell P Func T.Adj
 NetName
 1 dcd_succ_last_t1
                           R C3+R
                                         2668 -1669 3294 1011 1 PO
dcd_succ_last_t1
                         999
RAT
----> BOX714/OUT
                      R C3+R
                                          2668 -1669 3294 1011 1 IOPAD
                                                                         IOPAD
0 dcd_succ_last t1
----> BOX714/IN
                              R C3+R
                                        2668 : -1669 3294 1011 1 IOPAD
                                                                         IOPAD
 0 dcd_succ_last_t1&0
 ----> C167/v
                             R C3+R
                                      2668 -1669 3294 1011 1 cs_invvv 01c NOT
 0 dcd_succ_last_t1&0
 ----> C167/a
                             FC3+R
                                      1075 -1669
                                                   27 139 4 cs_invvv 01c NOT
1594 N675
---->{a} C2738/y
                              F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND
0 N675
----> C2738/a
                              R C3+R
                                       1056 -1669
                                                    33 114 1 cs_nnd2x 14b NAND
19 last_cycle
---->{b} C2487/y
                              RC3+R
                                       1056 -1669
                                                    33 114 1 cs_nnd2x 14e NAND
0 last_cycle
----> C2487/a
                              FC3+R
                                       1035 -1669
                                                   22 145 3 cs_nnd2x 14e NAND
21 N1587
----> C1952/v
                             FC3+R
                                       1035 -1669
                                                       145 3 cs_invvv 19b NOT
N1587
----> C1952/a
                              RC3+R
                                       1024 -1669
                                                   80 319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT
                                RC3+R
                                          1024 -1669
                                                      80 319 1 IOPAD
                                                                         IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN
                               RC3+R
                                        1024 -1669
                                                     80 319 1 IOPAD
                                                                       IOPAD
                                                                                0
num_dcd_cyl(1)
----> num_dcd_cyl(1)
                                R C3+R
                                         1024 -1669
                                                     80 319 1 PI
                                                                            0
num_dcd_cyl(1)
```

2 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO 0
iu_reset_op_c_t1	
RAT	999 · 0
RAT > BOX716/OUT	R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	·
> BOX716/IN	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	
>{a} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0	$\cdot$
> C2393/a	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6	
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031	
>{b} C2162/v	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031 ···	en de la companya de
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	
> rcvry reset.reg n.lat_0/l2_c	out_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	
> rcvrv reset.reg n.lat 0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	
• • • • • • • • • • • • • • • • • • •	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB  F C3+R 2354 -1355 1874 1011 1 PO 0
• • • • • • • • • • • • • • • • • • •	"E-00.D" 00E4 40EE 4074 4044 4 DC
• • • • • • • • • • • • • • • • • • •	"E-00.D" 00E4 40EE 4074 4044 4 DC
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD FC3+R 2354 -1355 1874 1011 1 CS_invvv 01c NOT RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y 0 N675	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 CS_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y 0 N675> C2738/b	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y 0 N675> C2738/b 49 N1692	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675> {a} C2738/y 0 N675> C2738/b 49 N1692>{b} C2725rwr/y	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 CS_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675> {a} C2738/y 0 N675> C2738/b 49 N1692>{b} C2725rwr/y 0 N1692	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675> {a} C2738/y 0 N675> C2738/b 49 N1692> {b} C2725rwr/y 0 N1692> C2725rwr/a	999 0 FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  FC3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  RC3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND  FC3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y 0 N675> C2738/b 49 N1692>{b} C2725rwr/y 0 N1692> C2725rwr/a 46 N1479	999 0  F C3+R 2354 -1355 1874 1011 1 PO 0  F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND  F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND  R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y 0 N675> C2738/b 49 N1692>{b} C2725rwr/y 0 N1692> C2725rwr/a 46 N1479>{c} C2721rwr/y	999 0  F C3+R 2354 -1355 1874 1011 1 PO 0  F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD  F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT  R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT  R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND  F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND  F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND  R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675>{a} C2738/y 0 N675> C2738/b 49 N1692> {b} C2725rwr/y 0 N1692> C2725rwr/a 46 N1479>{c} C2721rwr/y 0 N1479	999 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675> {a} C2738/y 0 N675> C2738/b 49 N1692> {b} C2725rwr/y 0 N1692> C2725rwr/a 46 N1479> C2721rwr/y 0 N1479> C2721rwr/b 68 N892	999 0 F C3+R 2354 -1355 1874 1011 1 PO 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd3i 11b NAND F C3+R 983 -1355 36 113 2 cs_nnd3i 11b NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675> {a} C2738/y 0 N675> C2738/b 49 N1692> {b} C2725rwr/y 0 N1692> C2725rwr/a 46 N1479> C2721rwr/y 0 N1479> C2721rwr/b 68 N892> {d} C2338/y	999 0 F C3+R 2354 -1355 1874 1011 1 PO 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd3i 11b NAND F C3+R 983 -1355 36 113 2 cs_nnd3i 11b NAND
3 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT 0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0> C167/y 0 dcd_succ_last_t1&0> C167/a 1208 N675> {a} C2738/y 0 N675> C2738/b 49 N1692> {b} C2725rwr/y 0 N1692> C2725rwr/a 46 N1479> C2721rwr/y 0 N1479> C2721rwr/b 68 N892	999 0 F C3+R 2354 -1355 1874 1011 1 PO 0 F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 IOPAD IOPAD F C3+R 2354 -1355 1874 1011 1 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_invvv 01c NOT R C3+R 1146 -1355 69 139 4 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2x 14b NAND F C3+R 1097 -1355 64 178 3 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd2g 14e NAND R C3+R 1051 -1355 116 170 2 cs_nnd3i 11b NAND F C3+R 983 -1355 36 113 2 cs_nnd3i 11b NAND

.

04 N4440	
24 N1119 > C2905/y	R C3+R 959 -1355 71 159 3 cs_invvv 12b NOT 0
N1119	11 00111 000 71 100 005_111444 1201401 0
> C2905/a	F C3+R 915 -1355 59 76 1 cs_invvv 12b NOT 45
N2010	•
>{e} C2906/y	F C3+R 915 -1355 59 76 1 cs_nor2g 12e NOR
0 N2010	D.CO.D. 000 1055 00 104 1 or north 100 NOD
> C2906/b 47 dcd_blk_dsucc&0	R C3+R 868 -1355 80 124 1 cs_nor2g 12e NOR
> BOX644/OUT	R C3+R 868 -1355 80 124 1 IOPAD IOPAD
0 dcd_blk_dsucc&0	
> BOX644/IN	R C3+R 868 -1355 80 124 1 IOPAD IOPAD 0
dcd_blk_dsucc	B 00 B 000 40FF 00 404 4 F
	R C3+R 868 -1355 80 124 1 PI 0
dcd_blk_dsucc	
	·
4 local_milli_t2.reg_n.lat_0/a	F C3+R2650 -134096923 cl_invvn07c SRL
50 NET1056	
Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	E CO.D. 0050 4040 00 00 0
0 NET1056	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
> BOX789/a	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
60 NET1054	**************************************
>{b} BOX785/y	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c.NAND
0 NET1054	
> BOX785/a	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
81 N1866 >{c} C2555/y	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
0 N1866	13 COTTI 2010 -1040 100 10 105_d01211 000 AOI
> C2555/b	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0	
>{d} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
> C2393/a 1863 gbfonet_6	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031	D.O. D. 470 4400 404 444 15 15 15 15 15 15 15 15 15 15 15 15 15
>{e} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031 > C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	. 55.11 555 1400 144 £17 5 65_HINGSV 026 NAIND
> rcvry_reset.reg_n.lat_0/l2_out	_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32 1 LCB
> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
Elocal milli td rear in lat 0/-	E C2   D   2650   1240   06   02 2 d   invers   070 CD

Setup local_milli_t1.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C	3- 160	60	238 14 cl_invvn	07c
>{a} BOX789/y	F C3+R	2650 -1340	96	92 3 cs_nnd3z	07c NAND
0 NET1056		2000 1010		02 0 00	<b>3.3.</b>
> BOX789/a	R C3+R	2590 -1340	120	32 1 cs_nnd3z	07c NAND
60 NET1054					
>{b} BOX785/y	R C3+R	2590 -1340	120	32 1 cs_nnd2f	03c NAND
0 NÈT1054					
> BOX785/a	F C3+R	2510 -1340	158	19 1 cs_nnd2f	03c NAND
81 N1866				•	
>{c} C2555/y	F C3+R	2510 -1340	158	19 1 cs_ao12n	03c AOI
0 N1866					
> C2555/b	R C3+R	2399 -1340	3318	1044 3 cs_ao12n	03c AOI
110 iu_reset_op_c_t1&0			0040	4044.0	. OO- NAND
>{d} C2393/y	H C3+H	2399 -1400	3318	1044 3 cs_nnd2\	/ U2C NAND
0 iu_reset_op_c_t1&0	- 00 D	F00 4400	400	100 0	OO - NIAND
> C2393/a	F C3+R	536 -1400	100	196 6 cs_nnd2v	U2C NAND
1863 gbfonet_6	E 00 - D	F0C 4400	100	100 C oo imaa. (	no NOT
3	FC3+R	536 -1400	100	196 6 cs_invvv (	J9C NOT
0 gbfonet_6	D C2 . D	470 1400	104	44 1 cs_invvv (	no NOT
> gbfocell_6/a	n Co+n	472 -1400	104	44 I CS_IIIVVV	DEC NO 1
64 N2031 >{e} C2162/y	B C3 B	472 -1400	19/	44 1 cs_nnd3v	02c NAND
0 N2031	n com	472 -1400	704	++ 1 C3_III/GOV	02011/1110
> C2162/a	F C3+B	358 -1400	144 2	217 5 cs nnd3v	02c NAND
114 rcvry_reset_q					
> rcvry_reset.reg_n.lat_0/l2_out	n . F(	C3+R 358 -	-1400	144 217 5 cl ii	nvvn 07d
SRL 0 rcvrv reset a					•
> rcvry_reset.reg_n.lat_0/c2	R C3	+ 160 N/	C 60	222 13 cl_invvr	n 07d SRL
198 slow mode.c2_1		and the second second		* ** **	
> slow_mode.clockblock/c2	RC	3+ 160 N	1/C (	60. 222 13 cb_clk	_32_1 LCB`
- 0 ·slow mode c2 1					

> compare\_critical\_slack\_limit

-1669.49 Avg: -125.31

comparing new slack -1669.4933 to saved slack -1652.7983

> traceset {repower\_paths HOWMANY}

[traceset]: trace string = repower\_paths HOWMANY

[tracing]: set trace variable repower\_paths to 20

> write\_end\_point\_report -points 3 -paths 1

[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end\_point\_report..92476.

[ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:08:37 1999

Part: IDCDSUC

Mode : Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 3

Cause of Slack Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path

Required Arrival Time RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)

```
Asserted Required Arrival Time AssrtRAT
                                     ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
 Clock Gating Setup
                       ClkGSet
                                 ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                      ClkGHld
                                 ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                        CIKTPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
 Setup
                   Setup
                            ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST )
 Hold
                  Hold
                           ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST)
 EndOfCycle
                     EndOfC
                                ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST )
 ClockPulseWidth
                       CIkPW
                                 ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE )
 ClockSeparation
                      ClkSep
                                ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
ARRIVAL TIME + ADJUST )
 Loop
                  ALTest
                            ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
CLOCK + ADJUST )
 Arrival Time Limiting
                      ATLimit
                                Slack discontinuity due to failed test
  Num/
                                LimitedAT/
                                                                Delay/ Failed Test/
 Test PinName
                               E Phase AT Slack Slew CL FO Cell P Func T.Adi
NetName
 __1 dcd_succ_last_t1
                                RC3+R 2668 -1669 3294 1011 1 PO
dcd_succ_last_t1
RAT
                                 999
----> BOX714/OUT
                                 RC3+R
                                           2668 -1669 3294 1011 1 IOPAD
0 dcd_succ_last_t1
                               R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
----> BOX714/IN
0 dcd_succ_last_t1&0
                                       2668 -1669 3294 1011 1 cs_invvv 01c NOT
----> C167/y
                              RC3+R
0 dcd_succ_last_t1&0
----> C167/a
                                       1075 -1669
                              FC3+R
                                                    27
                                                        139 4 cs_invvv 01c NOT
1594 N675
---->{a} C2738/v
                               FC3+R
                                        1075 -1669
                                                         139 4 cs_nnd2x 14b NAND
0 N675
----> C2738/a
                              RC3+R
                                        1056 -1669
                                                        114 1 cs_nnd2x 14b NAND
19 last_cycle
---->{b} C2487/y
                               R C3+R
                                        1056 -1669
                                                     33 114 1 cs_nnd2x 14e NAND
0 last_cycle
----> C2487/a
                              FC3+R
                                       1035 -1669
                                                     22 145 3 cs_nnd2x 14e NAND
21 N1587
----> C1952/y
                              FC3+R
                                       1035 -1669
                                                    22
                                                        145 3 cs_invvv 19b NOT
                                                                                   0
N1587
----> C1952/a
                                        1024 -1669
                              R C3+R
                                                     80 319 1 cs_invvv
                                                                       19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT
                                 R C3+R
                                           1024 -1669
                                                        80
                                                           319 1 IOPAD
                                                                           IOPAD
0 num_dcd cyl&0(1)
----> BOX679/IN
                               RC3+R
                                         1024 -1669
                                                      80 319 1 IOPAD
                                                                          IOPAD
                                                                                   0
num_dcd_cyl(1)
----> num_dcd_cyl(1)
                                RC3+R
                                          1024 -1669
                                                       80
                                                          319 1 PI
                                                                               0
```

` <b></b>	
2 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO 0
iu_reset_op_c_t1	
RAT	999 0
> BOX716/OUT	R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	
> BOX716/IN	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	D. CO. D
>{a} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
> C2393/a 1863 gbfonet_6	P C34H 550 -1400 100 190 0 C3_1md24 02014 1105
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
04 10004	
>{b} C2162/y	R-C3+R 472 -1400 184 -44 1 cs_nnd3v 02c NAND
0 N2031	
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	07d
> rcvry_reset.reg_n.lat_0/l2_out	_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	

1874 1011 1 PO 2354 -1355 3 dcd\_succ\_last\_t1 F.C3+R dcd\_succ\_last\_t1 999 RAT 2354 -1355 1874 1011 1 IOPAD **IOPAD** FC3+R ----> BOX714/OUT 0 dcd\_succ\_last\_t1 **IOPAD** 2354 -1355 1874 1011 1 IOPAD FC3+R ----> BOX714/IN 0 dcd\_succ\_last\_t1&0 2354 -1355 1874 1011 1 cs\_invvv 01c NOT FC3+R ----> C167/y 0 dcd\_succ\_last\_t1&0 69 139 4 cs\_invvv 01c NOT RC3+R 1146 -1355 ----> C167/a 1208 N675 139 4 cs\_nnd2x 14b NAND R C3+R 1146 -1355 ---->{a} C2738/y 0 N675 1097 -1355 178 3 cs\_nnd2x 14b NAND ----> C2738/b FC3+R 64 49 N1692 1097 -1355 64 178 3 cs\_nnd2g 14e NAND FC3+R ---->{b} C2725rwr/y 0 N1692 116 170 2 cs\_nnd2g 14e NAND RC3+R 1051 -1355 ----> C2725rwr/a 46 N1479 116 170 2 cs\_nnd3i 11b NAND RC3+R 1051 -1355 ---->{c} C2721rwr/y 0 N1479 36 113 2 cs\_nnd3i 11b NAND 983 -1355 ---> C2721rwr/b FC3+R 68 N892 36 113 2 cs\_nnd2x 14c NAND ---->{d} C2338/y FC3+R 983 -1355 0 N892

```
----> C2338/a
                                  RC3+R
                                             959 -1355
                                                          71 159 3 cs_nnd2x 14c NAND
 24 N1119
 ----> C2905/v
                                  RC3+R
                                            959 -1355
                                                          71
                                                              159 3 cs invvv 12b NOT
                                                                                           0
 N1119
 ----> C2905/a
                                  FC3+R
                                            915 -1355
                                                          59
                                                              76 1 cs invvv 12b NOT
                                                                                          45
 N2010
 ---->{e} C2906/y
                                  FC3+R
                                             915 -1355
                                                          59
                                                               76 1 cs_nor2g 12e NOR
 0 N2010
 ----> C2906/b
                                  RC3+R
                                             868 -1355
                                                          80 124 1 cs_nor2g 12e NOR
 47 dcd_blk_dsucc&0
 ----> BOX644/OUT
                                     RC3+R
                                                868 -1355
                                                             80 124 1 IOPAD
                                                                                  IOPAD
 0 dcd_blk_dsucc&0
 ----> BOX644/IN
                                   RC3+R
                                              868 -1355
                                                           80 124 1 IOPAD
                                                                                 IOPAD
                                                                                           0
 dcd blk dsucc
 ----> dcd_blk_dsucc
                                    R C3+R
                                               868 -1355
                                                            80 124 1 PI
 dcd blk dsucc
       > critical clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIO...
 critical(clone(SCORE(ALL),ACTUAL,RE_POWER,FASTEST,NO_VIOLATIONS));
 -1669.49 Avg: -125.31
maximum area for proto box IDCDSUC is 4675
setting SCORE option to ALL.
setting ACTUAL option.
 setting RE_POWER option.
setting RE_POWER option.
setting FASTEST mode.
setting NO_VIOLATIONS option.
-1669.49 Avg: -125.31
 ArrayNum: 6 ArrayMax: 906
ArrayNum: 6 ArrayMax: 906
[BD-500100]: 0 parallel copies of gates were made.
[clone]: Execution time was 0.1 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > reset_critical_slack_limit
 -1669.49 Avg: -125.31
resetting the current slack to -1669,4933
        the current slack to -1669.4933

> critical tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATI...
 critical( tswap(SCORE(ALL),ESTIMATED,TWO_LEVEL,NO_VIOLATIONS) );
 -1669.49 Avg: -125.31
maximum area for proto box IDCDSUC is 4675
setting SCORE option to ALL.
setting ESTIMATED option.
setting TWO LEVEL option.
setting NO_VIOLATIONS option.
 -1669.49 Avg: -125.31
ArrayNum: 6 ArrayMax: 906
[BD-500304]: 0 pins swapped on 0 gates and 0 gates cloned.
[tswap]: Execution time was 0.0 seconds.
[BD-502000]: Called transforms 6 times and applied 0 of them.
        > tc_parm REGALL
        > repower_paths {FUZZY(0.02), SIMULTANEOUS_REPOWER}
initial slack is -1669
after repower paths slack is -1669
        > repower_paths FUZZY(0.02)
```

initial slack is -1669

after repower paths slack is -1669

```
> critical {repower(SCORE(ALL),INC ,NO_VIOLATIONS), re...
critical( repower(SCORE(ALL ),INC ,NO_VIOLATIONS),
repower(SCORE(ALL),INC,NO_VIOLATIONS,REPOWER_GROUP(BETA)));
-1669.49 Avg: -125.34
maximum area for proto box IDCDSUC is 4676
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
repower: setting SCORE option to ALL.
repower: setting INC mode.
repower: setting NO_VIOLATIONS option.
-1669.49 Avg: -125.34
ArrayNum: 6 ArrayMax: 906
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-500026]: repower was applied 0 times.
[repower]: Execution time was 0.3 seconds.
[BD-502000]: Called transforms 12 times and applied 0 of them.
  -----> compare_critical_slack_limit
-1669.49 Avg: -125.34
comparing new slack -1669.4933 to saved slack -1652.7983
          > reset critical_slack_limit
-1669.49 Avg: -125.34
resetting the current slack to -1669.4933
         > write_end_point_report -points 5
[ET-0018]: >Begin...New EndPoint Report
    for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:09:29 1999
Part: IDCDSUC
                                      EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                  Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                                Max. Endpoints: 5
Sort Field: Slack
                        Abbreviation Comparison/Description
 Cause of Slack
                                    Slack due to a point downstream on path
                         SlkCont
 Slack Continuation
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Required Arrival Time
                          RAT
                                         ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                          ClkGSet
 Clock Gating Setup
ARRIVAL TIME + ADJUST )
                                    ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK -
 Clock Gating Hold
                         CIkGHId
ARRIVAL TIME + ADJUST )
                                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                           CIKTPW
 Clock Tree Pulse Width
TRAILING EDGE)
                               ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                     Setup
 Setup
ADJUST)
                              ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                     Hold
 Hold
ADJUST )
                                   ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
  EndOfCycle
                        EndOfC
 ADJUST)
                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
  ClockPulseWidth
                         CIkPW
TRAILING EDGE)
```

ARRIVAL TIME + ADJUST) Loop ALTe CLOCK + ADJUST) Arrival Time Limiting Num/	est (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM  ATLimit Slack discontinuity due to failed test  LimitedAT/ Delay/ Failed Test/
Test PinName NetName	E Phase AT Slack Slew CL FO Cell P Func T.Adj
1 dcd_succ_last_t1 dcd_succ_last_t1	R C3+R 2668 -1669 3294 1011 1 PO 0
RAT > BOX714/OUT 0 dcd_succ_last_t1	999 0 R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
> BOX714/IN 0_dcd_succ_last_t1&0	
> C167/y 0 dcd_succ_last_t1&0 > C167/a	R C3+R 2668 -1669 3294 1011 1 cs_invvv 01c NOT F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT
1594 N675 >{a} C2738/y 0 N675	F C3+R 1075 -1669 27 139_4 cs_nnd2x 14b NAND
> C2738/a 19 last_cycle	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND
>{b} C2487/y 0 last_cycle > C2487/a	R C3+R 1056 -1669 33 114_1 cs_nnd2x 14e,NAND F C3+R 1035 -1669 22 145_3 cs_nnd2x 14e,NAND
21 N1607	F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
> C1952/a 11 num dcd cvl&0(1)	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
> BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1) > num_dcd_cyl(1) num_dcd_cyl(1) 	R C3+R 1024 -1669 80 319 1 Pl 0
 2 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO 0
RAT > BOX716/OUT 0 iu_reset_op_c_t1	999 R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
> BOX716/IN 0 iu_reset_op_c_t1&0 >{a} C2393/y	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0 > C2393/a	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6 > gbfocell_6/y 0 gbfonet_6	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT

1	Line N. Ole	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
	> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
	64 N2031 >{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
	0 N2031	11 00111 112 1100 101 111 112 2 2 2 2 2
i	> C2162/a	F C3+R .358 -1400 144 217 5 cs_nnd3v 02c NAND
	114 rcvry_reset_q	
i	> rcvry_reset.reg_n.lat_0/l2_out	ut_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
i	SRL 0 rcvry_reset_q	
i	> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	198 slow_mode.c2_1	D.CO. 150 N/C 50 222 13 ch clk 32 1 LCB
i	> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
i		
1		: : : : : :
1		F C3+R 2352 -1353 1874 1011 1 PO 0
1	dcd_succ_last_t1	999 0
i	RAT POY714/OUT	999 F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
1		F C3+n 2332 -1333 1074 1011 1101715 10775
1	0 dcd_succ_last_t1> BOX714/IN	F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
i	0 dcd_succ_last_t1&0	1 00111 2002 1000 1001 1000
i	> C167/y	F C3+R 2352 -1353 1874 1011 1 cs_invvv 01c NOT
	0 dcd succ last t1&0	
1	> C167/a	R C3+R 1144 -1353 69 139 4 cs_invvv 01c NOT
the section of	1.20g NR75	D.CO. D. 11444 1252 60 120 4:00 nnd2v 14h NAND
1	>{a} C2738/y	R C3+R 1144 -1353 69 139 4 cs_nnd2x 14b NAND
· · · · · · · · · · · · · · · · · · ·	0 N6/5	F C3+R 1095 -1353 64 178 3 cs_nnd2x 14b NAND
	> C2738/b 49 N1692	F C3+H 1095 -1353 04 170 3 05 inidex 175 inidex
	49 N1692 >{b} C2725rwr/y	F C3+R 1095 -1353 64 178 3 cs_nnd2g 14e NAND
	0 N1692	
1	> C2725rwr/a	R C3+R 1049 -1353 116 170 2 cs_nnd2g 14e NAND
1	46 N1479	
1 .	>{c} C2721rwr/y	R C3+R 1049 -1353 116 170 2 cs_nnd3i 11b NAND
1 ,	0 N1479	5 00 5 004 4050 04 112 2 oc pp//3i 11h NAND 1 17 7 7 1 1 1 1
	> C2721rwr/b	F C3+R 981 -1353 34 113 2 cs_nnd3i 11b NAND
i	67 N892 >{d} C2338/y	F C3+R 981 -1353 34 113 2 cs_nnd2x 14c NAND
i	>{u} C2338/y 0 N892	1 00+11 001 1000 01 1.0 2 00
i	> C2338/a	R C3+R 958 -1353 62 159 3 cs_nnd2x 14c NAND
1	23 N1119	
1	> C2905/y	R C3+R 958 -1353 62 159 3 cs_invvv 13b NOT 0
i	N1119	
i	> C2905/a	F C3+R 918 -1353 63 92 1 cs_invvv 13b NOT 41
i	N2010	F C3+R 918 -1353 63 92 1 cs_nor2g 12e NOR
i	>{e} C2906/y	F C3+R 918 -1353 63 92 1 cs_nor2g 12e NOR
i	0 N2010 > C2906/b	R C3+R 868 -1353 80 124 1 cs_nor2g 12e NOR
	50 dcd blk_dsucc&0	N C3+N 000 -1000 00 12+ 1 00_10129 120 1101.
	> BOX644/OUT	R C3+R 868 -1353 80 124 1 IOPAD IOPAD
	0 dcd_blk_dsucc&0	1100111 000 1000 00 1=1
	> BOX644/IN	R C3+R 868 -1353 80 124 1 IOPAD IOPAD 0
	dcd_blk_dsucc	
	> dcd_blk_dsucc	R C3+R 868 -1353 80 124 1 PI 0
1	dcd_blk_dsucc	
4		

	***************************************	
	- <del>-</del>	
	4 local_milli_t2.reg_n.lat_0/a	F C3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
	50 NET1056	
	Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
	1200 slow_mode.c1_4	
	>{a} BOX789/y	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
	0 NET1056	
	> BOX789/a	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
	60 NET1054	B 00 B 0-00 (010 100 00 )
	>{b} BOX785/y	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
	0 NET1054	E 00 D 0540 4040 450 40 4 · · · · · · · · · · · · · · · · ·
	> BOX785/a	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
	81 N1866	E.CO. D. 0510 1040 150 10 1 co co10c 00c AOI
	>{c} C2555/y	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
	0 N1866 > C2555/b	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
	110 iu_reset_op_c_t1&0	N 03+N 2399 -1340 3316 1044 3 CS_a01211 03C AOI
	>{d} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
	0 iu_reset_op_c_t1&0	TOOPTI 2000 - 1400 0010 1044 0 63_HIIQEY 026 IMMIND
	> C2393/a	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
	1863 abfonet 6	
19,14	> abfocell 6/v	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
	0 gbfonet_6	
		R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
	C4 NOOO4	المنافع
11	>{e} C2162/y	-R-C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
	0 N2031	
· ·		F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
	114 rcvry_reset_q	
		_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	SRL 0 rcvry_reset_q	D 00 1 1400 1400 00 000 40 d 1400 107d 000
*		R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	198 slow_mode.c2_1	160 N/C - 60-222.13-cb_clk_32_1LCB
== \$1775	0 slow_mode.c2_1	100 1 N/O ; OUNT 222 13 CO_CIK_32_11 LOD
	0 Slow_IIIode.cz_1	
		·
	5 local milli t1.reg n.lat 0/a	F C3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
	50 NET1056	. 22 2000 10.10 00 02 001_111111 070 0112
	Setup local_milli_t1.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
	1200 slow_mode.c1_4	
	>{a} BOX789/y	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
	0 NET1056	· — · ·
	> BOX789/a	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
	60 NET1054	
	>{b} BOX785/y	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
	0 NET1054	
	> BOX785/a	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
	81 N1866	
	>{c} C2555/y	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
	0 N1866	D.OO.D. 0000 4040 0040 4044 0 40 00 401
	> C2555/b	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
	110 iu_reset_op_c_t1&0	D.C2.D. 2200 1400 2219 1044 2 as modely 00s NAND
	>{d} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND

```
0 iu reset_op_c_t1&0
                                FC3+R
                                           536 -1400
                                                       100 196 6 cs_nnd2v 02c NAND
----> C2393/a
1863 gbfonet_6
                                                        100 196 6 cs_invvv
                                                                            09c NOT
----> gbfocell_6/y
                                FC3+R
                                           536 -1400
0 abfonet 6
                                                              44 1 cs invvv 09c NOT
----> gbfocell_6/a
                                 R C3+R
                                            472 -1400
                                                        184
64 N2031
                                 RC3+R
                                            472 -1400
                                                        184
                                                              44 1 cs_nnd3v 02c NAND
---->{e} C2162/y
0 N2031
                                FC3+R
                                           358 -1400
                                                       144 217 5 cs nnd3v 02c NAND
----> C2162/a
114 rcvry_reset_q
                                       FC3+R
                                                  358 -1400
                                                              144 217 5 cl_invvn 07d
----> rcvry reset.reg_n.lat_0/l2_out_n
SRL
     0 rcvrv reset q
                                                     N/C
                                                            60 222 13 cl_invvn 07d SRL
----> rcvry_reset.reg_n.lat_0/c2
                                     R C3+
                                               160
198 slow mode.c2 1
                                    R C3+
                                                      N/C
                                                             60 222 13 cb_clk_32_1 LCB
                                                160
----> slow mode.clockblock/c2
0 slow mode.c2_1
         > repower_paths {FUZZY(0.02), LOWVT, NUM_CLUSTERS(16)}
initial slack is -1669
total pct of low vt boxes initially is 5.475
box count 621, pct of low vt boxes added is 19.65
total pct of low vt boxes used is 5.636
after repower paths slack is -1669

> write_end_point_report -points 5

[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report:.92476.
for file /tmp/end_point_report:.92476.

[ET-0019]: <End.....New Endpoint Report.
                                  Sun Apr 18 22:09:30 1999
Part: IDCDSUC
Mode : Late Mode / Nominal
                                   EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                 Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                    Max. Endpoints: 5
Sort Field: Slack
                       Abbreviation Comparison/Description
 Cause of Slack
                        SlkCont
                                   Slack due to a point downstream on path
 Slack Continuation
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                        RAT
 Required Arrival Time
 Asserted Required Arrival Time AssrtRAT
                                        ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
                                    ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 Clock Gating Setup
                         ClkGSet
ARRIVAL TIME + ADJUST )
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                        CIkGHId
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                          CIKTPW
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 Clock Tree Pulse Width
TRAILING EDGE)
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
 Setup
ADJUST )
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 Hold
                    Hold
ADJUST)
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                       EndOfC
 EndOfCycle
ADJUST)
 ClockPulseWidth
                         CIkPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
```

A I C	TRAILING EDGE ) ClockSeparation ARRIVAL TIME + ADJUST Loop AI CLOCK + ADJUST ) Arrival Time Limiting  Num/ Test PinName NetName	ClkSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2  ST) LTest (DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM  ATLimit Slack discontinuity due to failed test  LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
	1 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT	R C3+R 2668 -1669 3294 1011 1 PO 0 999 0 R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
***************************************	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0	R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
	> C167/y 0 dcd_succ_last_t1&0 > C167/a	R C3+R 2668 -1669 3294 1011 1 cs_invvv 01c NOT F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT
e in the second of the second	0 N675	F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND
	> C2738/a 19 last_cycle >{b} C2487/y 0 last_cycle	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND  R C3+R 1056 -1669 33 114 1 cs_nnd2x 14e NAND
	> C2487/a 21 N1587 > C1952/y	F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
	N1587 > C1952/a 11 num_dcd_cyl&0(1)	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
	> BOX679/OUT 0 num_dcd_cyl&0(1) > BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD  R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
	num_dcd_cyl(1)> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 PI 0
	2 iu_reset_op_c_t1	
	RAT> BOX716/OUT 0 iu_reset_op_c_t1	999 0 R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
	> BOX716/IN 0 iu_reset_op_c_t1&0 >{a} C2393/y	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD  R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
	0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
	> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT

0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031	D 00 D 470 4400 404 44 4 22 mmd0v 000 NAND
>{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031 > C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q > rcvry_reset.reg_n.lat_0/l2_ou	ıt_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q > rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	
3 dcd_succ_last_t1 dcd_succ_last_t1	F C3+R 2352 -1353 1874 1011 1 PO 0
RAT	999 0
	F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1 > BOX714/IN	F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
0 dcd_succ_last_t1&0	P 05+N 2552 -1555 1074 1011 1101 NB 101 NB
	F C3+R 2352 -1353 1874 1011 1 cs_invvv 01c NOT
0 dcd_succ_last_t1&0	
=	R C3+R 1144 -1353 69 139 4 cs_invvv 01c NOT
1208 N675 >{a} C2738/y	R C3+R 1144 -1353 69 139 4 cs_nnd2x 14b NAND
0 N675	
> C2738/b	F C3+R 1095 -1353 64 -178 3 cs_nnd2x 14b NAND
49 N1692	F C3+R 1095 -1353 64 178 3 cs_nnd2g 14e NAND
>{b} C2725rwr/y 0 N1692	F C3+H 1095 -1353 64 178 3 CS_IIIIUZY 146 INAIND
> C2725rwr/a	R C3+R 1049 -1353 116 170 2 cs_nnd2g 14e NAND
46 N1479	
>{c} C2721rwr/y	R C3+R 1049 -1353 116 170 2 cs_nnd3i 11b NAND
0 N1479 > C2721rwr/b	F C3+R 981 -1353 34 113 2 cs_nnd3i 11b NAND
67 N892	1 00111 001 1000 04 110 £ 00_1mdoi 110 10 10
>{d} C2338/y	F C3+R 981 -1353 34 113 2 cs_nnd2x 14c NAND
0 N892	D.CO. D. 050 4050 60 450 0 as modely 445 NAND
> C2338/a 23 N1119	R C3+R 958 -1353 62 159 3 cs_nnd2x 14c NAND
> C2905/y	R C3+R 958 -1353 62 159 3 cs_invvv 13b NOT 0
N1119	
> C2905/a	F C3+R 918 -1353 63 92 1 cs_invvv 13b NOT 41
N2010	F C3+R 918 -1353 63 92 1 cs_nor2g 12e NOR
>{e} C2906/y 0 N2010	1 COTIL 310 -1000 00 32 1 W_HOLZY 120 HOLL
> C2906/b	R C3+R 868 -1353 80 124 1 cs_nor2g 12e NOR
50 dcd_blk_dsucc&0	D 00 D 000 40F0 00 404 4 10D4D 10D4D
> BOX644/OUT	R C3+R 868 -1353 80 124 1 IOPAD IOPAD
0 dcd_blk_dsucc&0 > BOX644/IN	R C3+R 868 -1353 80 124 1 IOPAD IOPAD 0
dcd_blk_dsucc	7, 55171 550 1500 55 121 1157715 151715 5
> dcd_blk_dsucc	R C3+R 868 -1353 80 124 1 PI 0

4 local_milli_t2.reg_n.lat_0/a	F C3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
50 NET1056	
Setup local_milli_t2.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4	
>{a} BOX789/y	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
0 NET1056	
> BOX789/a	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
60 NET1054	
>{b} BOX785/y	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
0 NET1054	
> BOX785/a	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
81 N1866	
>{c} C2555/y	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
0 N1866	
	R.C3+R. 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0	5.00 B
>{d} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0	F. CO. D
1969 obtains 6	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6	E.C. D. F. F. 1400 100 106 6 on invest 000 NOT
0 gbfonet_6	F.C3+R536 -1400 100 196 6 cs_invvv 09c NOT
o gbioriet_o	B C3+B - 472 - 1400 - 194 - 44 1 ce invay - 00c NOT
- 64 N2031	R-C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
>{e} C2162/v	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031	11 00 111 472 1400 104 44 1 03_11100V 02011AND
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	
> rcvrv reset.reg n.lat 0/l2 out	_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	and the state of the
	F.O. B
5 local_milli_t1.reg_n.lat_0/a	F C3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
50 NET1056	F.CO. 400 CO. 000 44 al incom. 07a
Setup local_milli_t1.reg_n.lat_0/c1	F C3- 160 60 238 14 cl_invvn 07c
1200 slow_mode.c1_4 >{a} BOX789/y	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
0 NET1056	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
> BOX789/a	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
60 NET1054	11 COTIT 2090 -1040 120 32 1 CS_IIIIG32 U/C IVAIND
>{b} BOX785/y	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
0 NET1054	11 00+11 2000 10+0 120 02 1 C3_111021 00C 14A10D
> BOX785/a	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
81 N1866	. 35 2510 1610 160 10 1 65_HHQ21 000 IVAIVD
>{c} C2555/y	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
0 N1866	10 100 LO 10 10 100 LO 100
> C2555/b	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0	

```
2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
                               RC3+R
---->{d} C2393/y
0 iu reset op c t1&0
                                                          196 6 cs_nnd2v 02c NAND
                               FC3+R
                                         536 -1400
                                                     100
----> C2393/a
1863 abfonet_6
                                                           196 6 cs_invvv
                                                                          09c NOT
                               FC3+R
                                        536 -1400
                                                      100
----> gbfocell_6/y
0 gbfonet_6
                                          472 -1400
                                                      184
                                                            44 1 cs invvv 09c NOT
----> gbfocell_6/a
                               R C3+R
64 N2031
                                                            44 1 cs nnd3v 02c NAND
                               RC3+R
                                          472 -1400
                                                      184
---->{e} C2162/y
0 N2031
                                                     144 217 5 cs_nnd3v 02c NAND
                                         358 -1400
                               FC3+R
----> C2162/a
114 rcvry_reset_q
                                                358 -1400
                                                           144 217 5 cl_invvn 07d
                                      FC3+R
----> rcvry_reset.reg_n.lat_0/l2_out_n
SRL
        0 rcvry_reset_q
                                    R C3+
                                                   N/C
                                                         60 222 13 cl invvn 07d SRL
                                             160
----> rcvry_reset.reg_n.lat_0/c2
198 slow mode.c2_1
                                                           60 222 13 cb clk 32_1 LCB
---> slow_mode.clockblock/c2
                                     R C3+
                                              160
                                                    N/C
0 slow mode.c2_1
         > compare_critical_slack_limit
-1669.49 Avg: -125.33
comparing new slack -1669.4933 to saved slack -1652.7983
        > traceset {repower_paths HOWMANY}
[traceset]: trace string = repower_paths HOWMANY
[tracing]: set trace variable repower_paths to 20
      > write end_point_report -points 3 -paths 1
[ET-0018]: >Begin...New EndPoint Report
for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:09:30 1999
Part: IDCDSUC
                                   EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
Sort Field: Slack
                              Max. Endpoints: 3
 Cause of Slack
                      Abbreviation Comparison/Description
                   _____
                                  Slack due to a point downstream on path
                       SIkCont
 Slack Continuation
                                  ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                        RAT
 Required Arrival Time
                                       ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
                                  ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                        ClkGSet
 Clock Gating Setup
ARRIVAL TIME + ADJUST )
                                  ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                       CIkGHId
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                                     ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 Clock Tree Pulse Width
                         CIKTPW
TRAILING EDGE )
                             ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 Setup
                   Setup
ADJUST)
                            ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                   Hold
 Hold
ADJUST)
                                 ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                      EndOfC
 EndOfCycle
ADJUST )
```

	kPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE ) ClockSeparation Cli ARRIVAL TIME + ADJUST )	(Sep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
Loop ALTest CLOCK + ADJUST )	( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
	Limit Slack discontinuity due to failed test
Num/ Test PinName NetName	LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
1 dcd_succ_last_t1 dcd_succ_last_t1 RAT	R C3+R 2668 -1669 3294 1011 1 PO 0
> BOX714/OUT 0.dcd_succ_last_t1	R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
> BOX714/IN 0 dcd_succ_last_t1&0	R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
> C167/y 0 dcd_succ_last_t1&0	
> C167/a 1594 N675	F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT
>{a} C2738/y 0-N675 > C2738/a	F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND
> C2/38/a 19 last_cycle >{b} C2487/y	
0 last_cycle > C2487/a	F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
21 N1587 > C1952/y	F C3+R 1035 -1669 - 22 145 3 cs_invvv 19b NOT 0
N1587 > C1952/a	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1)> BOX679/OUT	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1) > BOX679/IN num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 PI 0
2 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO 0
RAT> BOX716/OUT 0 iu_reset_op_c_t1	999 R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
> BOX716/IN 0 iu_reset_op_c_t1&0	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
>{a} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
> C2393/a 1863 gbfonet_6	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND

	1. N. O.L.	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
	> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
	0 gbfonet_6> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
	64 N2031	
	>{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
	0 N2031	The second secon
	> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
	114 rcvry_reset_q	t_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
	CDI A rount recet a	
	> rcvrv reset.reg n.lat 0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	100 alow made c2 1	
	> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	0 slow_mode.c2_1	
	3 ded succ last t1	F C3+R 2352 -1353 1874 1011 1 PO 0
	4 4 14 44	
	-RAT	999
	> BOX714/OUT	F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1	F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
	0 ded citée lest t180	
	> C167/v	F C3+R 2352 -1353 1874 1011 1 cs_invvv 01c NOT
	> C167/a	R C3+R 1144 -1353 69 139 4 cs_invvv 01c NOT
	1208 N675	-D C2 D 1144 -1353 60 139 4 cs nnd2x 14h NAND
	>{a} U2/38/y	R C3+R 1144 -1353 69 139 4 cs_nnd2x 14b NAND
• ".	> C2738/b	F C3+R 1095 -1353 64 178 3 cs_nnd2x 14b NAND
	49 N1692	F C3+R 1095 -1353 64 178 3 cs_nnd2x 14b NAND
		F C3+R 1095 -1353 64 178 3 CS 10020 146 NAND
	0 N1692	R C3+R 1049 -1353 116 170 2 cs_nnd2g 14e NAND
	46 N1470	
	>{c} C2721rwr/v	R C3+R 1049 -1353 116 170 2 cs_nnd3i 11b NAND
-	0 N1479	
	> C2721rwr/b	F C3+R 981 -1353 34 113 2 cs_nnd3i 11b NAND
	67 N892	F C3+R 981 -1353 34 113 2 cs_nnd2x 14c NAND
	>{d} C2338/y 0 N892	1 00111 001 1000 01 110 <u>2 302</u>
	> C2338/a	R C3+R 958 -1353 62 159 3 cs_nnd2x 14c NAND
	23 N1119	
	> C2905/y	R C3+R 958 -1353 62 159 3 cs_invvv 13b NOT 0
	N1119	F C3+R 918 -1353 63 92 1 cs_invvv 13b NOT 41
	> C2905/a N2010	1 00 11 010 1000 00 02 1 00_mm 1 00 110 1
	>{e} C2906/y	F C3+R 918 -1353 63 92 1 cs_nor2g 12e NOR
	0 N2010	
	> C2906/b	R C3+R 868 -1353 80 124 1 cs_nor2g 12e NOR
	50 dcd_blk_dsucc&0	R C3+R 868 -1353 80 124 1 IOPAD IOPAD
	> BOX644/OUT 0 dcd_blk_dsucc&0	N 60+N 000 -1000 00 12+ 1101 NP 101 NP
	> BOX644/IN	R C3+R 868 -1353 80 124 1 IOPAD IOPAD 0
	dcd_blk_dsucc	
1	- <b>-</b>	

```
----> dcd_blk_dsucc
                                    R C3+R
                                               868 -1353
                                                             80 124 1 PI
                                                                                       0
dcd_blk_dsucc
       > chkbuff
[BD-500000]: chkbuff CMVC version 1.11 compiled on Apr 13 1999 at 18:21:07
[BD-501000]: Removed 0 buffers and merged 0 AND gates.
[chkbuff]: Execution time was 0.0 seconds.
       > dualcnt REG
[dualcnt]: 0 REG boxes are followed by inverters
       > dualcnt IOPAD
[dualcnt]: 32 or 7 IOPAD boxes are followed by inverters
       > dual_rail_to single rail
[dual_rail_to_single_rail]: CMVC version 1.8 compiled on Apr 13 1999 at 18:01:34.
[dual_rail_to_single_rail]: created 0 single rail boxes
       > nextbox chklegal
>>]: nextbox(_chklegal_);_____
[BD-41212]: (E) Gate 'slow_mode.clockblock' is bound to cell 'cb_clk_32_1' which is not a proper parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_1' is bound to cell 'cb_clk_32_1' which is not a proper
[BD-41212]: (E) Gate 'slow_mode.clockblock_2' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_3' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41212]: (E) Gate 'slow_mode.clockblock_4' is bound to cell 'cb_clk_32_1' which is not a proper
[BD-41212]: (E) Gate 'slow_mode.clockblock_5' is bound to cell 'cb_clk_32_1' which is not a proper
parent.
[BD-41200]: No illegal DOT gates found.
[BD-41200]: No illegal pin drops found.
                                                                             > nextnet chklegal
>>]: nextnet( chklegal );
[BD-41206]: No illegal pin drops found.
[BD-41204]: No illegally dotted nets found.
       > checksrc
[BD-40132]: Network IDCDSUC has no potential problems.
      > nextbox dbuff()
>>]: nextbox( dbuff() );
[BD-500000]: dbuff CMVC version 1.6 compiled on Apr 13 1999 at 18:22:00
      > reset timing
      > checkfan
Electrical Violations in Network 'IDCDSUC'
                                              Capacitance
                                                                   Slew
                                                                                   Sink
Fanout
Pin/Port
                       -> Net
                                                Limit / AdjLim / Actual Limit / AdjLim / Actual
Limit / AdjLim / Actual
eu_iu_enter slow md
                            -> eu_iu_enter_slow_md
                                                              141.00 / 141.00 / 16.73 290.00
/ 290.00 / 352.00 * 12 / 12 / 1 1 on ing stores
op_inq_stores
                         -> op ing stores
                                                      141.00 / 141.00 / 159.72 * 290.00 /
```

290.00 / 112.00

12/ 12/ 3 1

```
141.00 / 141.00 / 32.56 290.00 /
eu_iu_mmode
                     -> eu_iu_mmode
290.00 / 326.00 * 12 / 12 / 2 1
                                                 141.00 / 141.00 / 141.99 * 290.00
du iu hold_aa_req
                       -> du_iu_hold_aa_req
                 12/ 12/ 2 1
/ 290.00 / 424.00 *
                                                  141.00 / 141.00 / 30.80 290.00 /
                       -> eu_iu_fpu_end_op
eu_iu_fpu_end_op
                12/ 12/ 1 1
290.00 / 339.00 *
                                                141.00 / 141.00 / 19.15 290.00 /
                       -> eu_iu_misc_hold
eu_iu_misc_hold
                12/ 12/ 1 1
290.00 / 332.00 *
                                                 141.00 / 141.00 / 144.35 * 290.00 /
                       -> op_mcend_raw
op_mcend_raw
290.00 / 91.00
               12/ 12/ 3 1
                                        141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                  -> clkg
clka
       12/ 12/ 3 1
60.00
                      -> du_iu_quiesced
                                               141.00 / 141.00 / 20.50 290.00 /
du_iu_quiesced
290.00 / 338.00 *
              12/ 12/ 1 1
                                           141.00 / 141.00 / 170.11 * 290.00 / 290.00
                    -> iq_empty
ia empty
/ 116.00
         12 / 12 / 4 1
                     -> gptr_scan_in
                                             141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
gptr_scan_in
    12/ 12/ 1 1
0.00
            gptr_a_clk
      12/ 12/ 1 1
0.00
                                           141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                    -> gptr_b_clk
gptr_b_clk
            12/ 1 1
0.00
      12/
                            141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                  -> clka2
clkq2
/ 290.00 / 390.00 * 12 / 12 / 1 1 ....
du_iu_store_status(2) -> du_iu_store_status(2) 141.00 / 141.00 / 16.89 290.00 /
290.00 / 500.00 * 12 / 12 / 1 1
                                               141.00 / 141.00 / 47.57 290.00 /
                     -> eu_iu_srlz_op_actn(0)
eu iu srlz op actn(0)
290.00 / 374.00 * 12 / 12 / 2 1
eu_iu_srlz_op_actn(1) -> eu_iu_srlz_op_actn(1) 141.00 / 141.00 / 47.57 290.00 / 290.00 / 341.00 * 12 / 12 / 2 1
290.00 / 341.00 * 12 / 12 / 2 1
                                                                         وروسيني سدد د
                                               141.00 / 141.00 / 318.91 * 290.00 /
                    -> num_dcd_cyl(1)
num dcd cyl(1)
290.00 / 80.00
             12 / 12 / 1 1
                                                       141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(0)
                         -> eu_iu_srlz_op_encode(0)
290.00 / 290.00 / 401.00 *
                        12/ 12/ 1 1
                        -> eu_iu_srlz_op_encode(1)
                                                      141.00 / 141.00 / 16.89
eu iu srlz op encode(1)
290.00 / 290.00 / 400.00 *
                        12/ 12/ 1 1
                                                      141.00 / 141.00 / 16.89
                         -> eu_iu_srlz_op_encode(2)
eu iu srlz op encode(2)
                        12/ 12/ 1 1
290.00 / 290.00 / 420.00 *
                                                       141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(3)
                         -> eu_iu_srlz_op_encode(3)
290.00 / 290.00 / 302.00 *
                        12/ 12/ 1 1
                                                       141.00 / 141.00 / 16.89
eu iu srlz_op_encode(4)
                         -> eu_iu_srlz_op_encode(4)
290.00 / 290.00 / 406.00 *
                        12/ 12/ 1 1
                                                       141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(5)
                          -> eu_iu_srlz_op_encode(5)
290.00 / 290.00 / 373.00 *
                        12/ 12/ 1 1
                                                       141.00 / 141.00 / 16.89
                          -> eu_iu_srlz_op_encode(6)
eu iu srlz op encode(6)
290.00 / 290.00 / 354.00 *
                        12/ 12/ 1 1
                                                       141.00 / 141.00 / 16.89
eu iu srlz_op_encode(7)
                         -> eu_iu_srlz_op_encode(7)
290.00 / 290.00 / 398.00 *
                        12/ 12/ 1 1
                         -> eu_iu_srlz_op_encode(8)
                                                       141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(8)
                        12/ 12/ 1 1
290.00 / 290.00 / 367.00 *
                        -> eu_iu_srlz_op_encode(9)
                                                       141.00 / 141.00 / 16.89
eu iu srlz op encode(9)
                        12/ 12/ 1 1
290.00 / 290.00 / 323.00 *
                         -> eu_iu_srlz_op_encode(11)
                                                      141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(11)
```

```
290.00 / 290.00 / 500.00 * 12 / 12 / 1 1
           c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1 78.50 / 78.50 / 220.92 *
           200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP BTR KEEP BHC NO PARALLEL
           NO SERIAL
           c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
                                                               78.50 / 78.50 / 222.27 *
           200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
           NO SERIAL
           clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
                                                                78.50 / 78.50 / 212.39 *
           200.00 / 200.00 / 184.59 12 / 2 / 13 * 13 KEEP_BTR KEEP BHC NO PARALLEL
           c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
                                                                78.50 / 78.50 / 237.92 *
           200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
           NO SERIAL
           c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
                                                                78.50 / 78.50 / 239.36 *
           200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO SERIAL
           clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2
                                                                78.50 / 78.50 / 228.73 *
          200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
                                                                78.50 / 78.50 / 237.92 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP BHC NO PARALLEL
     NO_SERIAL
          c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3
                                                             78.50 / 78.50 / 239.37 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
      NO_SERIAL ....
clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
          200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
 200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO_SERIAL
                  Capacitance Slew
                                                                    Sink
          Fanout
          Limit / AdiLim / Actual
          c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                                78.50 / 78.50 / 239.36 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP BHC NO PARALLEL
          NO SERIAL
          clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4 78.50 / 78.50 / 228.73 *
          NO SERIAL
          c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
                                                                78.50 / 78.50 / 237.91 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO_SERIAL
          c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5
                                                                78.50 / 78.50 / 239.37 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP BHC NO PARALLEL
          NO_SERIAL
          clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5
                                                              78.50 / 78.50 / 228.73 *
          200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO SERIAL
          c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1
                                                               78.50 / 78.50 / 237.92 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO SERIAL
          c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2
                                                               78.50 / 78.50 / 239.37 *
```

```
12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
                                                             78.50 / 78.50 / 228.73 *
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                       12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 198.79
NO SERIAL
                                                        70.00 / 70.00 / 1011.00 * 301.00
                           -> dcd_succ_last_t1&0
y@C167:cs_invvv01c
                         12 / 1 1 KEEP_BTR
/ 301.00 / 3294.02 *
                    12/
                                                    68.00 / 68.00 / 77.40 * 290.00 /
                            -> N1531
y@C1994:cs_invvn01c
                            2 2
290.00 / 286.02
                 12/ 12/
                                                    68.00 / 68.00 / 1011.00 * 301.00 /
                            -> N18&0
v@C2013:cs_invvn01c
301.00 / 3608.92 *
                 12/
                        12 / 1 1
                                                     68.00 / 68.00 / 1011.00 * 301.00 /
                            -> N146&0
v@C2082:cs_invvn01c
                        12 / 1 1
301.00 / 3604.78 * 12 /
                                                    261.00 / 261.00 / 271.46 * 290.00 /
                            -> N1681
y@C2194:cs_invvn07c
290.00 / 261.53
                 12/ 12/
                            7 7
                                                         71.00 / 71.00 / 1044.40 *
y@C2393:cs_nnd2v02c
                            -> iu_reset_op_c_t1&0
290.00 / 290.00 / 3371.12 *
                          12/ 12/
                                     3 3
                                                    68.00 / 68.00 / 125.56 * 290.00 /
y@C2425:cs_invvn01c
                            -> N1815
                                                   ------
290.00 / 451.90 * 12 /---12 /
                           1 1 --
                                                     85.00 / 85.00 / 97.67 * 290.00 /
                            -> N1435
v@C2496:cs_nnd4n03c
290.00 / 353.82 *
                       12/ 5 5
                 12/
                                                    133.00 / 133.00 / 150.69 * 290.00 /
                            -> N1645
y@C2646:cs_invvn04c
                       12/ 6 6
290.00 / 275.60
                 12 /
                                                        500.00 / 500.00 / 540.60 *
v@C2726;cs nnd2n11c
                            -> dsucc_or_agi&0
290.00 / 290.00 / 258.01 12 / 12 / 2 2
y@C2744:cs_invvn13c
                           -> N2086&0
                                                     996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 271.62 12 / 12 / 7 7
                                                    326.00 / 326.00 / 234.15 290:00 /
y@C2800:cs_invvn08c
                            -> N1290
               12/ 12/ 14*14:
290.00 / 193.42
                                                     167.00 / 167.00 / 183.47 * 290.00 / ...
                            -> N1097
y@C2728rwr:cs_invvn05c
290.00 / 266.58
                 12/--12/ 4 4
                                                     110.00 / 110.00 / 132.34 * 290.00 /
y@C2918:cs_nor2n04c
                           -> N2016
290.00 / 428.15 *
                 12/
                       12/
                            1 1
                                                                              290.00 / - -
                                                     797.00 / 797.00 / 402.55
y@gbfocell_0:cs_invvn12c
                            -> abfonet_0
290.00 / 149.98
                 12 / 12 / 20 * 20
                                                          l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
290.00 / 290.00 / 242.45
                         12/ 12/ 8 8
```

## [BD-500900]: (W) There were 64 electrical violations. > measure

1.544730

The model <IDCDSUC> has: 122 **Primary Inputs** 73 **Primary Outputs** 0 **Primary BIDIs** 1129 Signals 906 Gate Count Connections 1744 Master REG Bits 83 83 Slave REG Bits 4676 Internal Area 0 External Area 0.519495 Gates/Connects 1744 **Fanout Count** 

Average Fanout

Avg Tech Box Size = 5.161148 Tech Box Size Stddev = 0.011242 Power 0.000000 \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\* Real signals 754 Real boxes 531 Real connections 1369 Real LSTs 2123 Real ICells/box 8.806026 Real LSTs/box 3.998117 Real nets/box 1.419962 Cell Total Each Cell Type Cnt Boxname Power Level Function Int Ext Power Int Ext Power -----6 cs ao22n03c 03c AOI 6 0 0.000 36 0 0.000 ...2 cs\_ao12n03c-----03c- --> --AOI 4----0 0.000 --8--0.000 1 cs\_ao12n10c 10c AOI > 12 0 0.000 12 0.000 cs\_ao22n04c 04c AOI 6 > 0 0.000 6 0.000 cs\_ao22n10c 1 10c > AOI 18 0.000 0 18 0.000 1 cs\_ao12n07c 07c ·>: -AOI 6 0 0.000 6 0.000 .> 180 BRKPT BRKPT 0 0 0.000 --- 0 0 0.000 195 IOPAD .... > IOPAD 0 0-0.000 0 0.000 141 NAND 3 cs\_nnd2n02c 02c 0.000 423 0.000 19 cs\_nnd2n04c 04c NAND 3 0 0.000 57 0.000 \_\_1 cs\_nnd2v05c 05c NAND 4 0.000 4 0 0.000 ---1 cs\_nnd2n12c 12c > . **NAND** 12 0 - 0.000 12 0 0.000 cs\_nnd3n02c 18 02c > NAND 4 - 0 0.000 0.000 72 0 1 cs\_nnd3v02c 02c NAND 4 0 0.000 4 0.000 3 cs\_nnd2v13c - 13c > NAND 15 0 0.000 45 0.000 3 cs\_nnd2n03c 03c : > NAND. 3 0 0.000 9 0 0.000 5 cs\_nnd4n03c 03c NAND . 5 25 0.000 > . 0 0.000 2 cs\_nnd3n03c 03c NAND 4 > 0 0.000 8 0 0.000 **....2** .... cs\_nnd2n11c 11c > NAND 11 0.000 22 .... 0 0.000 2 cs\_nnd2x14c 14c NAND 24 0 0.000 48 0 0.000 1 cs\_nnd2v02c 02c > **NAND** 3 0 0.000 3 0 0.000 1 cs nnd3n07c 07c **NAND** > 6 0 0.000 6 0 0.000 4 cs\_nnd2x14e 14e > **NAND** 20 0.000 80 0.000 2 cs\_nnd2n07c 07c > **NAND** 4 0 0.000 8 0.000 1 cs nnd2x14b 14b NAND 28 > 0.000 28 0.000 1 cs\_nnd3i11b 11b NAND 30. 0 0.000 -30 0.000 1 cs\_nnd4v10c 10c > **NAND** 20 0 0.000 20 0 0.000 1 cs\_nnd2q14e 14e **NAND** > 23 0 0.000 23 0 0.000 1 cs\_nnd4v10b 10b NAND 20 > 0 0.000 20 0.000 1 cs\_nnd2n08c 08c NAND > 7 0 0.000 7 0.000 1 cs\_nnd2v14c 14c > NAND 19 0 0.000 19 0.000 2 cs\_nnd3n05c 05c > NAND 6 0 0.000 12 0.000 1 cs\_nnd2n05c 05c > NAND 4 0 0.000 4 0 0.000 1 cs nnd2v11c 11c > **NAND** 11 0 0.000 0 11 0.000 1 cs\_nnd2g11b 11b > **NAND** 19 0 0.000 19 0 0.000 1 cs\_nnd3z10c 10c > NAND 18 0 0.000 18 0 0.000 1 cs\_nnd2f03c 03c NAND 4 0 0.000 4 0.000 1 cs\_nnd3z07c 07c **NAND** 10 0 0.000

10

0

0.000

_	mmd4v060		06c	_	NAND	8	0	0.000	16	0	0.000	
2	cs_nnd4v06c		02c	>	NOR	3	0	0.000	21	o	0.000	
7	cs_nor2n02c			>		3	0	0.000	12	ő	0.000	
4	cs_nor2n04c		04c	>	NOR			0.000	4		0.000	
1	cs_nor3n03c		03c	>	NOR	4	0					
1	cs_nor2g12e		12e	>	NOR	27	0	0.000	27	0	0.000	
1	cs_nor3v10e		10e	>	NOR	16	0	0.000	16	0	0.000	
1	cs_nor2v11c		11c	>	NOR	11	0	0.000	11	0	0.000	
1	cs_invvv01c		01c	>	NOT	2		0.000	2		0.000	
22	cs_invvn12c		12c	>	NOT	6	0	0.000	132	0	0.000	
6	cs_invvn10c		10c	>	NOT	4	0	0.000	24		0.000	
5	cs_invvn09c		09c	>	NOT	4	0	0.000	20		0.000	
48	cs_invvn07c		07c	>	NOT	2	0	0.000	96	0	0.000	
49	cs_invvn01c		01c	>	NOT	2	0	0.000	98	0	0.000	
6	cs_invvn15c		15c	>	NOT	10	0	0.000	60	0	0.000	
3	cs_invvn11c		11c	>	NOT	6	0	0.000	18	0	0.000	
4	cs_invvn13c		13c	>	NOT	8	0	0.000	32	0	0.000	
1	cs_invvv19b		19b	>	NOT	28	Ō	0.000	28	0	0.000	
6	cs_invvn06c		06c	>	NOT	2	Õ	0.000	12	0	0.000	
	cs_invvn08c		-08c	>	NOT	4	0	0.000	12	Ö	0.000	
3 -	<b>-</b>		02c	>	NOT	2	Ö	0.000	6		0.000	
3	cs_invvn02c		14c	>	NOT	8	0	0.000	16		0.000	
2	cs_invvv14c		04c		NOT	2	0	0.000	24	ŏ	0.000	
12	cs_invvn04c			>	NOT	2	0	0.000	16		0.000	
8	cs_invvn05c		05c	>		8		0.000	8		0.000	
1.	cs_invvn14c	·	14c	->	NOT				8		0.000	- 
. 1	cs_invvv13b	_	13b	>	NOT	. 8	0	0.000			0.000	•
.1	cs_invvv13c	2 411 3	13c	>	NOT	8	0	0.000	8 .		0.000	
1	cs_invvv10c		10c	_>-	NOT	4	0	0.000				
1_	cs_invvn16c		16c	<u>≥</u> <u>.</u>	NOT	14	0	0.000			0.000	
_1	cs_invvv09c		09c	>	NOT	4	0	0.000	4			1.12
1.	cs_invvn01e		01e		NOT	2	0	0.000	2		0.000	
1	cs_oa21n10c		10c	>	OAI	14	0	0.000	14	0	0.000	• • •
1	cs_oa22n10c		10c	>	OAI	18	0	0.000	18	0	0.000	
1	cs_oa21n10e		10e	>	OAI	14	0	0.000	14	0	0.000	
22	cl_invvn07d		07d `	>	REG	25	0	0.000	550	0		
12	cl_invvn07c		07c	. چ.	REG	25	0	0.000	300	0	0.000	
18	cl_nnd2n07c	_ ````···	07c	>	REG	26		0.000			0.000	) · ·
1	cl_invvn05c		05c	>	REG	25	0_	0.000	25	0	0.000	
8	cl_ao22n07c		07c	>	REG	33	0	0.000	264			
14	cl_invvn06d		06d	>	REG	25	0	0.000	350	0		
1	cl_invvn05d		05d	>	REG	25	0	0.000	25	0	0.000	
2	cl_nnd3n07c		07c	>	REG	29	0	0.000	58	0	0.000	
1	cl_nor2n06c		06c	>	REG	26	0	0.000	26	0	0.000	
1	cl_ao21n07c		07c	>	REG	30	0	0.000	30	0	0.000	
2	cl_invvn06c		06c	>	REG	25	0 '	0.000	.50	0	0.000	,
1	cl_oa21n07c		07c	>	REG	30	0	0.000	30	0	0.000	
i	cb_mode_block		Α	> 5	SEQUEN		70		0.000	70	0 (	0.000
6	cb_clk_32_1				QUENTIA		30	0 0.0		180		000
1	cs_xbn2n01b		01b		XNOF			0.000				
1	cs_xbo2n01d		01d		XOR	. 8	0		8	0	0.000	
	OS_ADOEITO IG		514	_	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	-	•		•	-		

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

# of Levels Output

```
0 1 *
1 59 50* plus *********
2 1 *
3 4 ****
4 1 *
10 3 ***
11 1 *
12 3 ***
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
# of
Levels Register
       7
 2
       21
  3
       1
  5
       6
  6
 9
~ 10 6
 12
        2
        6.
 14
 15
 16
       14
```

The Histogram Of Fanin vs. Box

The Histogram Of Fanout vs. Net

```
# of
Fanout Nets
0
   2
      1
   931
      2
   96
3
   37
4
   16
5
   8
6
   13
7
8
   3
   3
13
14
   16
```

## [End of measure]

```
[measure]: Execution time was 0.8 seconds.
      > slackhist
[slackhist]: CMVC version 1.6 compiled on Mar 31 1999 at 11:27:25.
[slackhist]: worst = -1669.49, best = 1019.49, stddev=716.94 maxfanout 20
[slackhist]: avg = -125.33, delta = 0.50, intervals = 50
Distribution of Slacks for All Nets
Islackhistl: Worst -1669.49, Best
                                 1019.49
[slackhist]: Avg -125.33, Std Dev 716.94
                     High: Number Percent Cum Percent
[slackhist]:
            Low to
[slackhist]: -1669.50 to -1669.00:
                                7 0.62
                                            0.62
[slackhist]:
             Above -1644.50: 817 72.36
                                            72.98
[slackhist]:
               Other nets: 305 27.02
                                         100.00
[slackhist]:
      > prtdelay
[BD-500000]: prtdelay CMVC version 1.4 compiled on Apr 13 1999 at 18:31:38
IBD-5019001: Worst arrival time in the network is 2668.493164.
       > write end point report -points 10
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End.....New Endpoint Report.
Sun Apr 18 22:09:35 1999
Part: IDCDSUC
Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
                                  Max. Slack: 1.13427E+38
Min. Slack: -1.13427E+38
                               Max. Endpoints: 10
Sort Field: Slack
                        Abbreviation Comparison/Description
 Cause of Slack
                         SlkCont
                                    Slack due to a point downstream on path
 Slack Continuation
                                    ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                          RAT
 Required Arrival Time
                                         ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                     ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                         ClkGSet
 Clock Gating Setup
ARRIVAL TIME + ADJUST )
                                    ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
                         CIkGHId
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                           CIKTPW
                                       ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 Clock Tree Pulse Width
TRAILING EDGE )
                               ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
 Setup
                     Setup
ADJUST)
                              ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
                    Hold
 Hold
ADJUST )
                                   ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
                       EndOfC
 EndOfCycle
ADJUST)
                                    ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                         CIkPW
 ClockPulseWidth
TRAILING EDGE)
                                    ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ClockSeparation
                         ClkSep
```

ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM ALTest CLOCK + ADJUST ) Arrival Time Limiting **ATLimit** Slack discontinuity due to failed test Num/ LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj Test PinName NetName 1 dcd succ last t1 R C3+R 2668 -1669 3294 1011 1 PO 0 dcd\_succ\_last\_t1 RAT 999 ----> BOX714/OUT R C3+R 2668 -1669 3294 1011 1 IOPAD **IOPAD** 0 dcd\_succ\_last\_t1 ----> BOX714/IN R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD 0 dcd\_succ last t1&0 ----> C167/y --- --- R C3+R -- 2668 --1669 3294 1011 1 cs\_invvv 01c-NOT 0 dcd\_succ\_last\_t1&0 ----> C167/a F C3+R 1075 -1669 27 139 4 cs\_invvv 01c NOT 1594 N675 F C3+R -- 1075 -1669 27 139 4 cs\_nnd2x 14b NAND ---->{a} C2738/y 0 N675 R C3+R 1056 -1669 33 114 1 cs\_nnd2x 14b NAND 19 last\_cycle ---->{b} C2487/y R C3+R 1056 -1669 33 114 1 cs\_nnd2x 14e NAND 0 last cycle -----> C2487/a F C3+R 1035 -1669 22 145 3 cs\_nnd2x 14e NAND ----> C2487/a ---> C1952/y F C3+R 1035 -1669 22 145 3 cs\_invvv 19b NOT 0 N1587 ----> C1952/a R C3+R 1024 -1669 80 319 1 cs\_invvv 19b NOT 11 num\_dcd\_cyl&0(1) ----> BOX679/OUT R C3+R 1024 -1669 80 319 1 IOPAD **IOPAD** 0 num\_dcd\_cyl&0(1) ----> BOX679/IN R C3+R 1024 -1669 80 319 1 IOPAD IOPAD num\_dcd\_cyl(1) ----> num\_dcd\_cyl(1) R C3+R 1024 -1669 80 319 1 PI 0 num\_dcd\_cyl(1) 2 iu\_reset\_op\_c\_t1 R C3+R 2399 -1400 3318 1011 1 PO iu\_reset\_op\_c\_t1 RAT 999 ----> BOX716/OUT RC3+R 2399 -1400 3318 1011 1 IOPAD **IOPAD** 0 iu\_reset\_op c t1 ----> BOX716/IN R C3+R 2399 -1400 3318 1044 3 IOPAD **IOPAD** 0 iu\_reset\_op\_c\_t1&0 ---->{a} C2393/y R C3+R 2399 -1400 3318 1044 3 cs\_nnd2v 02c NAND 0 iu\_reset\_op\_c\_t1&0 ----> C2393/a FC3+R 536 -1400 100 196 6 cs nnd2v 02c NAND 1863 gbfonet\_6 ----> gbfocell\_6/y FC3+R 536 -1400 100 196 6 cs invvv 09c NOT 0 gbfonet\_6 ----> abfocell 6/a R C3+R 472 -1400 184 44 1 cs\_invvv 09c NOT

	64 N2031	= 0= = 100 100 101 11 10 00 NAND
	>{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
	0 N2031 > C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
	> C2162/a 114 rcvry_reset_q	F C3+N 330 -1400 144 217 3 65_1111007 325.11112
	> rcvry_reset.reg_n.lat_0/l2_ou	ut_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
	SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2	
	198 slow_mode.c2_1	N C3+ 100 14/0 00 222 10 01_1111111 07 0 01.12
	> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	0 slow_mode.c2_1	
	3 dcd_succ_last_t1 dcd_succ_last_t1	F C3+R 2352 -1353 1874 1011 1 PO 0
	RAT	999 0
	> BOX714/OUT	F C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
	0 dcd succ last t1	
·*	> BOX714/IN	F-C3+R 2352 -1353 1874 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1&0	A NOT
		F C3+R 2352 -1353 1874 1011 1 cs_invvv 01c NOT
	0 dcd_succ_last_t1&0	R C3+R 1144 -1353 69 139 4 cs_invvv 01c NOT
	> C167/a 1208 N675	H C3+H 1144 -1353 69 139 4 C5_IIIVVV OTCINOT
- T#↑ 5		
- 10 <del>- 10 - 1</del>	> C2738/b	F C3+R 1095 -1353 64 178 3 cs_nnd2x 14b NAND
	40 N1602	National Control of the Control of t
	>{b} C2725rwr/y	F C3+R 1095 -1353 64 178 3 cs_nnd2g 14e NAND
	U N1092	200 D 4040 4050 440 470 0 20 mmd0m 440 NAND
	> C2725rwr/a 46 N1479	R C3+R 1049 -1353 116 1/0 2 cs_nnd2g 14e NAND
	46 N1479	R C3+R 1049 -1353 116 170 2 cs_nnd2g 14e NAND  R C3+R 1049 -1353 116 170 2 cs_nnd3i 11b NAND
٠.	>{c} C2/21rwr/y 0 N1479	H C3+H 1049 -1333 110 170 2 63_111001 110 14/142
l	0 1114/9	
· · · · · · · · · · · · · · · · · · ·		F C3+R 981 -1353 34 113 2 cs_nnd3i 11b NAND
l	>{d} C2338/y	F C3+R 981 -1353 34 113 2 cs_nnd2x 14c NAND
1	0 N892	
1	> C2338/a	R C3+R 958 -1353 62 159 3 cs_nnd2x 14c NAND
1	23 N1119	1070 00 450 0 in 406 NOT 0
1	> C2905/y	R C3+R 958 -1353 62 159 3 cs_invvv 13b NOT 0
1	N1119	F C3+R 918 -1353 63 92 1 cs_invvv 13b NOT 41
l	> C2905/a N2010	F C3+M 918 -1333 03 92 1 C5_IIIVVV 100 NOT
1	N2010 >{e} C2906/y	F C3+R 918 -1353 63 92 1 cs_nor2g 12e NOR
1	0 N2010	1 00111 010 1000 00 02 1 00
1	> C2906/b	R C3+R 868 -1353 80 124 1 cs_nor2g 12e NOR
1	50 dcd_blk_dsucc&0	
ĺ	> BOX644/OUT	R C3+R 868 -1353 80 124 1 IOPAD IOPAD
1	0 dcd_blk_dsucc&0	
1	> BOX644/IN	R C3+R 868 -1353 80 124 1 IOPAD IOPAD 0
1	dcd_blk_dsucc	
1	> dcd_blk_dsucc	R C3+R 868 -1353 80 124 1 Pl 0
1	dcd_blk_dsucc	
4		**************************************

	4 local_milli_t2.reg_n.lat_0/a 50 NET1056	F C3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
	Setup local_milli_t2.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
	>{a} BOX789/y 0 NET1056	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
	> BOX789/a 60 NET1054	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
	>{b} BOX785/y 0 NET1054	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
	> BOX785/a 81 N1866	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
	>{c} C2555/y 0 N1866	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
	> C2555/b 110 iu_reset_op_c_t1&0	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
-0.1500 (0.1000 0.1000 0.1000 0.100		R C3+R 2399 1400 3318 1044 3 cs_nnd2v 02c NAND
	> C2393/a 1863 gbfonet_6	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
	> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv = 09c NOT
ادر کا میں کی میں فعاد دار ہے۔ ادار معادل معادل کی ایک کا دار ادار کا دار ایک کا دار کا	> gbfocell_6/a 64 N2031	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
-	U NZU31	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
	114 rcvrv reset a	F.C3+R3581400144 _ 217 _5 cs_nnd3v _ 02c NAND
***************************************	> rcvry_reset.reg n.lat 0/l2 out	_n F.C3+R 358 -1400 144 217 5 cl_invvn 07d
TO CATE PER CONTRACTOR AND	196 Slow_mode.cz_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
	> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	50 NET1056	F C3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
	Setup local_milli_t1.reg_n.lat_0/c1 1200 slow_mode.c1_4	F C3- 160 60 238 14 cl_invvn 07c
·	>{a} BOX789/y 0 NET1056	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
	> BOX789/a 60 NET1054	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
	>{b} BOX785/y 0 NET1054	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
	> BOX785/a 81 N1866	F C3+R 2510 -1340 158 19 1 cs_nnd2f 03c NAND
	>{c} C2555/y 0 N1866	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
	> C2555/b 110 iu_reset_op_c_t1&0	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
	>{d} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND

> C2393/a	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6	
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031	D 00 D 470 4400 404 44 4 12 mm 401 000 NAND
>{e} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
> C2162/a	F C3+H 330 -1400 144 217 3 C5_11103V 02C 14A10D
114 rcvry_reset_q> rcvry_reset.reg_n.lat_0/l2_out	n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	_11 1 00111 000 1400 111 277 0 0
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	
	F G3+R 2650 -1340 96 92 3 cl_invvn 07c SRL
50 NET1056	F C3- 160 60 238 14 cl_invvn 07c 1200
Setup local_milli.reg_n.lat_0/c1 slow_mode.c1_2	F C3- 100 00 230 14 CI_IIIVII 07C 1200
\$10W_1110de.C1_2	F C3+R 2650 -1340 96 92 3 cs_nnd3z 07c NAND
0 NET1056	
> BOX789/a	R C3+R 2590 -1340 120 32 1 cs_nnd3z 07c NAND
>{b} BOX785/y	R C3+R 2590 -1340 120 32 1 cs_nnd2f 03c NAND
O NETIOEA	Land to the control of the control o
	F-C3+R25101340158 19-1-cs_nnd2f - 03c NAND
81 N1866	F CO. D . 0510 . 1240 . 150 . 10.1 apr pp12n - 020-001
··· 0· N1866 ··	F C3+R 2510 -1340 158 19 1 cs_ao12n 03c AOI
> C2555/b	R C3+R 2399 -1340 3318 1044 3 cs_ao12n 03c AOI
110 iu_reset_op_c_t1&0	1100111 2000 1010 0010 1011 000_001211 0007101
>{d} C2393/v	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
>{d} C2393/y 0 iu_reset_op_c_t1&0 > C2393/a	
> C2393/a	F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6	
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6	D. CO. D. 470, 4400, 404, 44 4 co improv. 00c NOT
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
>{e} C2162/y 0 N2031	N 03+N 472 -1400 104 44 1 03_111100V 020 14/14D
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	7 00 11 000 110 111 217 0 00 <u>-</u>
> rcvry_reset.reg_n.lat_0/l2_out	t_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1	

	3 NET1056						
	Setup local_milli_t2.reg_n.lat_0/c1	FC	23- 160	60	238 14 cl_invvr	07c	
	1200 slow_mode.c1_4				200 0	. 0,0	
	>{a} BOX789/y	R C3+R	2582 -1225	145	92 3 cs_nnd3	z 07c NAND	
	0 NET1056		•				
	> BOX789/b	FC3+R	2486 -1225	132	36 1 cs_nnd3z	2 07c NAND	
	96 N639	E 00 B	0.400 400=				
	>{b} C2466/y 0 N639	F C3+R	2486 -1225	132	36 1 cs_nnd2n	02c NAND	
	> C2466/b	R C3+R	2300 -1225	2210	1044 3 cs_nnd2	n OOo NAND	
	86 iu_reset_op_c_t1&0	11 00+11	2099 -1220	3316	1044 3 CS_111102	II UZCINAND	
	>{c} C2393/y	R C3+R	2399 -1400	3318	1044 3 cs_nnd2	PV 02c NAND	
	0 iu_reset_op_c_t1&0					020 17 11 10	
	> C2393/a	FC3+R	536 -1400	100 1	96 6 cs_nnd2v	02c NAND	
	1863 gbfonet_6						
	> gbfocell_6/y	FC3+R	536 -1400	100 1	196 6 cs_invvv	09c NOT	
	0 gbfonet_6	D CO. D	470 4400	404	44 4 5	OO- NOT	
	> gbfocell_6/a		4/2- <del></del> 1400	184	441 CS_INVV	OAC NOT	The state of the control of the same of th
		B C3+B	472 -1400	184	44 1 cs_nnd3v	OSC NAND	
	N N2031						
may year of any	> C2162/a	F C3+R	358 - <b>-</b> 1400	144 2	217 5 cs nnd3v	- 02c NAND	-
	114 rcvry_reset_q				•		
	> rcvry_reset.reg_n.lat_0/l2_out	_nF(	C3+R 358 -	1400	-144 217 5 cl_	invvn 07d	
	SRL 0 rcvry_reset_q> rcvry_reset.reg_n.lat_0/c2			or Amerikan			
Carly and Life Wilson.	198 slow mode of 1	, 12 : H C3	3+ 160 N/G	60	° 222 13 cl_inv\	n 07d SRL	The state of the s
The state of the s	198 slow_mode.c2_1> slow_mode.clockblock/c2_	B C	.3± 160 N	_ <u>-</u> I/C∷=: 6	sn 222 13 ch c	k 22 1 I CB	
	0 slow_mode.c2_1	A STATE OF THE PERSON OF THE P		,,,,,,,,,	, , , , , , , , , , , , , , , , , , ,	N_02_1;; EOD,;;;;	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -
	0 slow_mode.c2_1			· ·			The second second second second
	. The state of the					and the second second	
•	8 local_milli_t1.reg_n.lat_0/a	R C3+	-R 2582 -12	25 14	l5 92 3 d inva	/n 07c SRL	Santa Harris Color
	3 NET1056				02 00_1110		
	Setup local milli t1 roa n let 0/e1		160		the work of the control of		* *
2000 00 0 00 00 0	Setup local_milli_t1.reg_n.lat_0/c1 1200_slow_mode_c1_4	FC	3- 160		the work of the control of		
	1200 slow_mode.c1_4			<u></u> 60	238 14 cl_invvn	<b>07c</b>	* .
	Setup local_milli_t1.reg_n.lat_0/c1 1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056			<u></u> 60	238 14 cl_invvn	<b>07c</b>	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b	R C3+R	2582 -1225	60 145	238 14 cl_invvn 92 3 cs_nnd3	07c z 07c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639	R C3+R F C3+R	2582 -1225 2486 -1225	60 145 132	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z	07c z 07c NAND 07c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y	R C3+R	2582 -1225 2486 -1225	60 145 132	238 14 cl_invvn 92 3 cs_nnd3	07c z 07c NAND 07c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y 0 N639	R C3+R F C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225	60 145 132 132	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z 36 1 cs_nnd2n	07c z 07c NAND 07c NAND 02c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y 0 N639 > C2466/b	R C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225	60 145 132 132	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z	07c z 07c NAND 07c NAND 02c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y 0 N639 > C2466/b 86 iu_reset_op_c_t1&0	R C3+R F C3+R F C3+R R C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225	60 145 132 132 3318	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z 36 1 cs_nnd2n 1044 3 cs_nnd2	07c z 07c NAND 07c NAND 02c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y 0 N639 > C2466/b 86 iu_reset_op_c_t1&0 >{c} C2393/y	R C3+R F C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225	60 145 132 132 3318	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z 36 1 cs_nnd2n	07c z 07c NAND 07c NAND 02c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y 0 N639 > C2466/b 86 iu_reset_op_c_t1&0 >{c} C2393/y 0 iu_reset_op_c_t1&0 > C2393/a	R C3+R F C3+R F C3+R R C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400	145 132 132 3318	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z 36 1 cs_nnd2n 1044 3 cs_nnd2	07c z 07c NAND 07c NAND 02c NAND n 02c NAND	* .
	1200 slow_mode.c1_4 >{a} BOX789/y 0 NET1056 > BOX789/b 96 N639 >{b} C2466/y 0 N639 > C2466/b 86 iu_reset_op_c_t1&0 >{c} C2393/y 0 iu_reset_op_c_t1&0 > C2393/a 1863 gbfonet_6	R C3+R F C3+R F C3+R R C3+R R C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400	145 132 132 3318 3318	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2 1044 3 cs_nnd2 96 6 cs_nnd2v	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y	R C3+R F C3+R F C3+R R C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400	145 132 132 3318 3318	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd3z 36 1 cs_nnd2n 1044 3 cs_nnd2	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y 0 gbfonet_6	R C3+R F C3+R R C3+R R C3+R F C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400	145 132 132 3318 3318 100 19	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2 1044 3 cs_nnd2 96 6 cs_nnd2v 96 6 cs_invvv	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND 02c NAND	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y 0 gbfonet_6> gbfocell_6/a	R C3+R F C3+R F C3+R R C3+R R C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400	145 132 132 3318 3318 100 19	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2 1044 3 cs_nnd2 96 6 cs_nnd2v	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND 02c NAND	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y 0 gbfonet_6> gbfocell_6/a 64 N2031	R C3+R F C3+R R C3+R R C3+R R C3+R F C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400 536 -1400 472 -1400	60 145 132 132 3318 3318 100 19 100 1	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2n 1044 3 cs_nnd2n 96 6 cs_nnd2v 96 6 cs_invvv 44 1 cs_invvv	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND 02c NAND 02c NAND	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y 0 gbfonet_6> gbfocell_6/a	R C3+R F C3+R R C3+R R C3+R F C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400 536 -1400 472 -1400	60 145 132 132 3318 3318 100 19 100 1	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2 1044 3 cs_nnd2 96 6 cs_nnd2v 96 6 cs_invvv	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND 02c NAND 02c NAND	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y 0 gbfonet_6> gbfocell_6/a 64 N2031>{d} C2162/y	R C3+R F C3+R R C3+R R C3+R R C3+R F C3+R F C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400 472 -1400 472 -1400	60 145 132 132 3318 3318 100 19 100 1 184 184	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2n 1044 3 cs_nnd2n 96 6 cs_nnd2v 96 6 cs_invvv 44 1 cs_nnd3v	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND 02c NAND 09c NOT 09c NOT	* .
	1200 slow_mode.c1_4>{a} BOX789/y 0 NET1056> BOX789/b 96 N639>{b} C2466/y 0 N639> C2466/b 86 iu_reset_op_c_t1&0>{c} C2393/y 0 iu_reset_op_c_t1&0> C2393/a 1863 gbfonet_6> gbfocell_6/y 0 gbfonet_6> gbfocell_6/y 0 Total C2162/y 0 N2031	R C3+R F C3+R R C3+R R C3+R R C3+R F C3+R F C3+R R C3+R	2582 -1225 2486 -1225 2486 -1225 2399 -1225 2399 -1400 536 -1400 472 -1400 472 -1400	60 145 132 132 3318 3318 100 19 100 1 184 184	238 14 cl_invvn 92 3 cs_nnd3 36 1 cs_nnd2n 36 1 cs_nnd2n 1044 3 cs_nnd2n 1044 3 cs_nnd2n 96 6 cs_nnd2v 96 6 cs_invvv 44 1 cs_invvv	07c z 07c NAND 07c NAND 02c NAND n 02c NAND v 02c NAND 02c NAND 09c NOT 09c NOT	* .

> rcvry_reset.reg_n.lat_0/l2_out_ SRL 0 rcvry_reset_q	_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
> rcvry_reset_reg_n.lat_0/c2 198 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
U Slow_mode.cz_1	·
3 NET1056	R C3+R 2582 -1225 145 92 3 cl_invvn 07c SRL
Setup local_milli.reg_n.lat_0/c1 slow mode.c1 2	F C3- 160 60 238 14 cl_invvn 07c 1200
>{a} BOX789/y	R C3+R 2582 -1225 145 92 3 cs_nnd3z 07c NAND
0 NET1056 > BOX789/b	F C3+R 2486 -1225 132 36 1 cs_nnd3z 07c NAND
96 N639 >{b} C2466/y	F C3+R 2486 -1225 132 36 1 cs_nnd2n 02c NAND
0 N639	- R C3+R 239912253318 1044 3 cs_nnd2n 02c NAND
86 iu_reset_op_c_t1&0	
>{c} C2393/y 0 iu_reset_op_c_t1&0	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
> C2393/a 1863 gbfonet_6	F C3+R 536 -1400 -100 - 196 6 cs_nnd2v 02c NAND
gbfocell_6/y	F C3+R - 536 -1400 -100 -196 6 cs_invvv 09c NOT
0 gbtonet_6	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031 >{d} C2162/y	R C3+R - 472 -1400 - 184 - 44 1 cs_nnd3v 02c NAND
	F-C3+R = 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvrv reset a	
SRL 0 rcvrv reset a	
198 slow mode.c2 1	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
> slow_mode.clockblock/c2 0 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	D. CO. D
10 idcdsuc_err N146	R C3+R 2126 -1127 3605 1011 1 PO 0
RAT > BOX750/OUT	999 R C3+R 2126 -1127 3605 1011 1 IOPAD IOPAD
0 N146 > BOX750/IN	R C3+R 2126 -1127 3605 1011 1 IOPAD IOPAD
0 N146&0 > C2082/y	R C3+R 2126 -1127 3605 1011 1 cs_invvn 01c NOT
0 N146&0 > C2082/a	F C3+R 295 -1127 48 32 2 cs_invvn 01c NOT
1831 dcdsuc_err_q	
> dcdsuc_err.reg_n.lat_0/l2_out SRL 0 dcdsuc_err_q	t_n F C3+R 295 -1127 48 32 2 cl_nnd2n 07c
> dcdsuc_err.reg_n.lat_0/c2 135 slow_mode.c2_1	R C3+ 160 N/C 60 222 13 cl_nnd2n 07c SRL

#### > measure

The model <idci< th=""><th>DSUC&gt; t</th><th>nas:</th></idci<>	DSUC> t	nas:
Primary Inputs	=	122
<b>Primary Outputs</b>	=	73
Primary BIDIs	=	0
Signals =	=	1129
Gate Count	=	906
Connections	=	1744
Master REG Bits	=	83
Slave REG Bits	=	83
Internal Area	=	4676
External Area	=	0
_Gates/Connects		0.519495
Fanout Count	=	1744
Average Fanout	=	1.544730
Avg Tech Box Si		5.161148
Tech Box Size S	tddev =.	0.011242
Power :	= :	0.000000

\*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\* 754 Real signals Real boxes \_531 Real connections = 1369 Real LSTs 2123 Real ICells/box 8.806026 Real LSTs/box 3.998117 Real nets/box 1.419962

Cell Total Each Cell

Type C	Cnt Boxname	Power	r Leve	I Fund	tion	Int	Ext	Power	Int	Ext	Powe
											. •
6	cs_ao22n03c	03c	>	AOI	6	0	0.000	36	0	0.000	
2.	cs_ao12n03c	03c	> .	AOI	4	0	0.000	8	0 (	0.000	•
1	cs_ao12n10c	10c	>	AOI	12	0	0.000	12	0	0.000	
1	cs_ao22n04c	04c	>	AOI	6	0	0.000	6	0 (	0.000	
1	cs_ao22n10c	10c	>	AOI	18	0	0.000	18	0	0.000	
1	cs_ao12n07c	07c	>	AOI	6	0	0.000	6	0 (	0.000	
180	BRKPT	>	BF	RKPT	0 .	0(	.000.0	. 0		.000	
195	IOPAD	>		PAD	0	0 0	.000	0 0		000	
141	cs_nnd2n02c	02c	>	NANI	D (	3 (	0.00	0 423		0.00	00
19	cs_nnd2n04c	04c	>	NANE	) 3	0			0		-
1	cs_nnd2v05c	05c	>	NAND	4	0	0.000		0	0.000	•
1	cs_nnd2n12c	12c	>	NAND	12	0			0		)
18	cs_nnd3n02c	02c	>	NANE	) 4	0	0.000		Ō		
1	cs_nnd3v02c	02c	>	NAND		0	0.000		0	0.000	
3	cs_nnd2v13c	13c	>	NAND	15	0			Ō	0.000	ì
3	cs_nnd2n03c	03c	>	NAND		0	0.000		o	0.000	,
5	cs_nnd4n03c	03c	>	NAND		Õ	0.000		0	0.000	
2	cs_nnd3n03c	03c	>	NAND	_	Ö	0.000		0	0.000	
2	cs_nnd2n11c	11c	>	NAND		0		-	0	0.000	`
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               cs nnd3n07c
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               cs nnd2x14e
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               cs invvn09c
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                cs_invvn01c
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               cs invvn15c
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               cs invvn11c
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               cs_invvn13c
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               cs invvv19b
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               cs invvn02c
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               cs invvv14c
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                                              >
                                                    NOT
                cs_invvn04c
           12
                                                                                   0.000
                                                                           16
                                                                                0
                                        05c
                                                    NOT
                                                           2
                                                               0
                                                                   0.000
                                              >
           8
               cs_invvn05c
                                                                   0.000
                                                                           8
                                                                                0
                                                                                   0.000
                                                    NOT
                                                           8
                                                               0
               cs invvn14c
                                        14c
                                              >
           1
                                                                                   0.000
                                                                   0.000
                                                                           8
                                                                                0
                                                   NOT
                                                           8
                                                                0
                                        13b
                                              >
               cs_invvv13b
           1
                                                                                   0.000
                                                           8
                                                               0
                                                                   0.000
                                                                           8
                                                                                0
                                        13c
                                                    NOT
                                              >
           1
               cs_invvv13c
                                                    NOT
                                                           4
                                                               0
                                                                   0.000
                                                                           4
                                                                                0
                                                                                   0.000
                                        10c
                                              >
           1
               cs_invvv10c
                                                           14
                                                                0
                                                                   0.000
                                                                           14
                                                                                 0
                                                                                    0.000
                                              >
                                                    NOT
                                        16c
               cs_invvn16c
           1
                                                               0
                                                                   0.000
                                                                           4
                                                                                0
                                                                                   0.000
                                                    NOT
                                                           4
                                        09c
                                              >
           1
                cs invvv09c
                                                           2
                                                                0
                                                                   0.000
                                                                           2
                                                                                0
                                                                                   0.000
                                                    NOT
                                        01e
                                              >
                cs invvn01e
           1
                                                                                    0.000
                                                                   0.000
                                                                           14
                                                                                 0
                                                    OAI
                                                           14
                                                                0
                                         10c
                                              >
                cs_oa21n10c
           1
                                                                    0.000
                                                                            18
                                                                                 0
                                                                                    0.000
                                                           18
                                                                0
                                                     OAL
                cs oa22n10c
                                         10c
                                               >
           1
                                                                                 0
                                                                                     0.000
                                                                 0
                                                                    0.000
                                                                            14
                                                           14
                cs_oa21n10e
                                         10e
                                               >
                                                     OAI
           1
                                                                                     0.000
                                                                           550
                                                                                  0
                                                           25
                                                                 0
                                                                    0.000
           22
                cl_invvn07d
                                        07d
                                              >
                                                    REG
                                                                           300
                                                                                     0.000
                                                                0
                                                                    0.000
                                                                                  0
                cl invvn07c
                                        07c
                                              >
                                                    REG
                                                           25
           12
                                                                    0.000
                                                                            468
                                                                                      0.000
                                         07c
                                               >
                                                     REG
                                                            26
                                                                 0
                                                                                  0
                cl_nnd2n07c
           18
```

. \_\_\_

```
1
   cl_invvn05c
                       05c >
                                 REG
                                      25
                                           0.000
                                                    25
                                                         0.000
8
   cl_ao22n07c
                                           0 0.000 264
                        07c >
                                 REG
                                      33
                                                          0.000
14
    cl_invvn06d
                        06d
                                 REG
                                       25
                                           0.000
                                                    350
                                                          0.000
1
   cl invvn05d
                       05d
                                 REG
                                       25
                                           0.000
                                                    25
                                                         0.000
2
   cl_nnd3n07c
                        07c
                            >
                                 REG
                                       29
                                           0.000
                                                    58
                                                         0.000
   cl_nor2n06c
                       06c
                                 REG
                                       26
                                           0.000
                                                    26
                            >
                                                         0
                                                            0.000
1
   cl_ao21n07c
                        07c >
                                 REG
                                      30
                                           0.000
                                                    30
                                                         0.000
2
   cl_invvn06c
                       06c >
                                 REG
                                      25
                                           0.000
                                                    50
                                                        0.000
1
   cl_oa21n07c
                        07c
                                 REG
                                       30
                                           0 0.000 30
                                                         0.000
1
   cb_mode_block
                                                             0 0.000
                                                0.000
                            > SEQUENTIAL
                                           70
                                                         70
6
   cb_clk_32_1
                           > SEQUENTIAL 80
                                              0 0.000 480
                                                            0.000
   cs_xbn2n01b
1
                        01b
                                 XNOR
                                         8
                                            0.000
                                                      8
                                                          0.000
1
   cs_xbo2n01d
                                  XOR
                                                         0.000
                        01d
                                        8
                                            0
                                              0.000
```

The Histogram Of Paths From Primary Inputs Or Registers To Outputs

```
# of
Levels Output

----

0    1    *
1    59    50* plus ********
2    1    *
3    4    ****
4    1    *
10    3    ***

11    1    1
12    3    ***
```

The Histogram Of Paths From Primary Inputs Or Registers To Registers

```
Levels Register
 2 ...
     21
 3
      1
 4
      5
 5
      6
 6
 9
      1
10
      6
12
      2
13
      1
14
      6
15
      7
16
      4
17
      14
```

The Histogram Of Fanin vs. Box

```
3
       35
       18
  4
The Histogram Of Fanout vs. Net
   # of
Fanout Nets
  0
       2
            1
      931
           2
       96
  3
       37
  4
       16
  5
       8
  6
       13
  7
       3
  8
       3
 13
        3
 14
       16
 20
        1
[End of measure]
[measure]: Execution time was 0.8 seconds.
 > randsim q
>>]: randsim( q );
 > randsim q
>>]: randsim( q ); _____
> good_names
 Good names for IDCDSUC
                                             Count
                                                     User
                                                             Like
                                                                     New
                                          17.45%
                                                    1.59%
                          1129
                                 80.96%
 For all nets
                                        0.00%
                                                 0.00%
 For register output nets
                        166 100.00%
                               99.44%
                                        0.56%
                                                 0.00%
 For break point input nets
                         180
                                         0.51%
                                                  0.00%
                                99.49%
 For model input/output nets
                          195
                                             Count
                                                       User
                                                               Like
                                                                       New
                                                  41.83%
 For all boxes
                           906
                                 58.17%
                                          0.00%
                           83
                                100.00%
                                          0.00%
                                                   0.00%
 For register boxes
   > summary_report
 The model <IDCDSUC> has:
                          122
  Primary Inputs
  Primary Outputs
                           73
  Primary BIDIs
                           0
                        1129
  Signals
  Gate Count
                          906
  Connections
                          1744
  Master REG Bits
                            83
  Slave REG Bits
                           83
                         4676
  Internal Area
  External Area
                           0
```

Gates/Connects 0.519495 **Fanout Count** 1744 Average Fanout 1.544730 Avg Tech Box Size = 5.161148 Tech Box Size Stddev = 0.011242 Power = 0.000000

### \*\*\*R-E-A-L\*\*\*S-T-A-T-I-S-T-I-C-S\*\*\*

Real signals = Real boxes 531 Real connections = 1369 Real LSTs 2123 Real ICells/box 8.806026 Real LSTs/box 3.998117 Real nets/box 1.419962

Total Cell Each Cell

يتسايد والمسائد

Type C	Ont Boxname	Power	r Leve	el Function	on I	Int	Ext Po	ower	Int	Ext Power
6	cs_ao22n03c	03c	>	AOI	6 (	0 0	0.000	36	0 (	0.000
2	cs_ao12n03c	03c	>	AOI				8 (		0.000
1	cs_ao12n10c		>				0.000			0.000
1	cs_ao22n04c		.>.	AOI			0.000	6 (	-	0.000
, <b>1</b> , .			->		.18					0.000-
1	cs_ao12n07c	070	>	AOI .				6 (		0.000
180	BRKPT	>			0 0	) 0				0.000
195	BRKPT IOPAD	_>.	. 10	PAD C	Ö Ö		000			000.
141	cs_nnd2nu2c						0.000	423	. (	0 0.000
19	cs_nnd2n04c		>	NAND		0		57	0	0.000
1	cs_nnd2v05c		>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd2n12c	12c	>	NAND		0.	٠,	12	0	0.000
	cs_nnd3n02c	02c	> .	NAND	4	0	0.000	72	0	0.000
1	cs_nnd3v02c	02c	>	NAND	4-	0	0.000	4	0	
3	cs_nnd2v13c	13c	>	NAND	15	0	0.000	45	0	
3	cs_nnd2n03c		->:	NAND	3	0	0.000	9		-0.000
5	cs_nnd4n03c	03c	> .	NAND	5	0	0.000	25	0 -	0.000
2	cs_nnd3n03c	03c	> .	NAND	4	0	0.000	8	0	0.000
2	cs_nnd2n11c	11c	>	NAND	11	0	0.000	22	0	
2	cs_nnd2x14c	14c	>	NAND	24	0	0.000	48	0	
1	cs_nnd2v02c	02c	>	NAND	3	0	0.000	3	0	0.000
1	cs_nnd3n07c	07c	>	NAND	6	0	0.000	6	0	0.000
4	cs_nnd2x14e	14e	>	NAND	20	0	0.000	80	0	
2	cs_nnd2n07c	07c	>	NAND	4	0	0.000	- 8		<b>0.000</b>
1	cs_nnd2x14b	14b	>	NAND	28	0	0.000	28	0	
1	cs_nnd3i11b	11b	>	NAND	30	0	0.000	30	0	0.000
1	cs_nnd4v10c	10c	>	NAND	20	0	0.000	20	0	
1	cs_nnd2g14e	14e	>	NAND	23	0		23	0	
1	cs_nnd4v10b	10b	>	NAND	20	0	0.000	20	0	
1	cs_nnd2n08c	08c	>	NAND	7	0	0.000	7	0	0.000
1	cs_nnd2v14c	14c	>	NAND	19	0	0.000	19	0	
2	cs_nnd3n05c	05c	>	NAND	6	0	0.000	12	0	0.000
1	cs_nnd2n05c	05c	>	NAND	4	0	0.000	4	0	0.000
1	cs_nnd2v11c	11c	>	NAND	11	0	0.000	11	0	
1	cs_nnd2g11b	11b	>	NAND	19	0	0.000	19	0	
1	cs_nnd3z10c	10c	>	NAND	18	0	0.000	18	0	0.000

1	cs_nnd2f03c	03c	>	NAND	4	0	0.000	4	0	0.000	
1	cs_nnd3z07c	07c	>	NAND	10	0	0.000	10	0	0.000	
2	cs_nnd4v06c	06c	>	NAND	8	0	0.000	16	0	0.000	
7	cs_nor2n02c	02c	>	NOR	3	0	0.000	21	0	0.000	
4	cs_nor2n04c	04c	>	NOR	3	0	0.000	12	0	0.000	
1	cs_nor3n03c	03c	>	NOR	4	0	0.000	4	0	0.000	
i	cs_nor2g12e	12e	>	NOR	27	0	0.000	27	0	0.000	
i	cs_nor3v10e	10e	>	NOR	16	Õ	0.000	16	0	0.000	
1	cs_nor2v11c	11c	>	NOR	11	Ō	0.000	11	0	0.000	
1	cs_invvv01c	01c	>	NOT	2		0.000			0.000	
22	cs_invvn12c	12c	>	NOT	6	0	0.000	132	0	0.000	
	cs_invvn10c	10c	>	NOT	4	Õ	0.000	24		0.000	
6		09c	>	NOT	4	Ö	0.000	20		0.000	
5	cs_invvn09c	07c	>	NOT	2	0	0.000	96	ŏ	0.000	
48	cs_invvn07c	0/C		NOT	2	0	0.000	98	0	0.000	
49	cs_invvn01c		>	NOT	10	0	0.000	60	0	0.000	
6	cs_invvn15c	15c	>	NOT	6	0	0.000	18		0.000	
3	cs_invvn11c	11c	>				0.000	32		0.000	
4	cs_invvn13c	13c	>	NOT	8	0		32 28		0.000	
- 1 -	cs_invvv19b	19b	>	NOT	28	0	0.000		9.		
6	cs_invvn06c	06c	>	NOT	2	0	0.000	12		0.000	
3	cs_invvn08c	08c	>	NOT	4	0	0.000	12		0.000	
3	cs_invvn02c	02c	>	NOT	2	0	0.000	6		0.000	
2	cs_invvv14c	14c	> .	NOT .	8	0	0.000	16		0.000	
12	cs_invvn04c	04c	>	NOT	2	0	0.000	24	0	0.000	•
8	cs_invvn05c	05c	> '	NOT	2	. 0	0.000	16		0.000	
1	cs_invvn14c	14c	>	NOT	8	0	0.000	8		0.000	
1 -	cs_invvv13b	- 13b	· >	NOT	8	0	0.000	8		0.000	
1	cs_invvv13c	13c	<b>&gt;</b> . ,	NOT	8	0	0.000	8		0.000	••
1	cs_invvv10c	-10c-		NOT	4		0.000	4		0.000	-
11.	.cs_invvn16c	16c "	> ~	NOT	14	0	0.000	14	0		
1	cs_invvv09c		·->	NOT	4	0	0.000	.4		0.000	
1:	cs_invvn01e	01e	> .	NOT	2	0	0.000	2		0.000	
1	cs_oa21n10c	10c	>	OAI	14	0	0.000	14	0	0.000	
1	cs_oa22n10c	10c	>	OAI	18	. 0	0.000	18	0	0.000	
1 .	cs_oa21n10e	10e	>	OAI	14	0	0.000	14	0	0.000	
22	cl_invvn07d	07d	> `	- REG	25	. 0	0.000	550	0	0.000	- ;.
12	cl_invvn07c	07c	>	REG	25	0	0.000	300	0		-
18	cl_nnd2n07c	07c	>	REG	26	0	0.000	468	0	0.000	
1	cl_invvn05c	05c	>	REG	25	0	0.000	25	0	0.000	
8	cl_ao22n07c	07c	>	REG	33	0	0.000	264	0	0.000	
14	cl_invvn06d	06d	>	REG	25	0	0.000	350	0	0.000	
1	cl_invvn05d	05d	>	REG	25	0	0.000	25	0	0.000	
2	cl_nnd3n07c	07c	>	REG	29	0	0.000	58	0	0.000	
1	cl_nor2n06c	06c	>	REG	26	0	0.000	26	0	0.000	
1	cl_ao21n07c	07c	>	REG	30	0	0.000	30	0	0.000	
2	cl_invvn06c	06c	>	REG	25	0	0.000	50	0	0.000	
1	cl_oa21n07c	07c	>	REG	30	0	0.000	30	0	0.000	
1	cb_mode_block	Α		SEQUEN		70		0.000	70		0.000
6	cb_clk_32_1			QUENTIA		30	0.0		80	0 0.0	
1	cs_xbn2n01b	01b	> OL	XNOF			0.000		0		
1	cs_xbn2n01b cs_xbo2n01d	01d	>	XOR	8	o		8	o	0.000	
ı	CS_XDUZHUTU	Jiu	_	AUIT	J	J	0.000	J	J	0.000	

[End of measure]

[measure]: Execution time was 0.6 seconds.

> write\_end\_point\_report -points 2 [ET-0018]: >Begin...New EndPoint Report for file /tmp/end\_point\_report..92476. [ET-0019]: <End.....New Endpoint Report.

Sun Apr 18 22:09:38 1999

Part: IDCDSUC

Mode: Late Mode / Nominal **EDA EinsTimer EndPoint Report** 

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack Max. Endpoints: 2

Cause of Slack Abbreviation Comparison/Description

Slack Continuation SlkCont Slack due to a point downstream on path

Required Arrival Time RAT ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Asserted Required Arrival Time AssrtRAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL

TIME)

Clock Gating Setup ClkGSet ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK

ARRIVAL TIME + ADJUST )

Clock Gating Hold ClkGHld ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK

ARRIVAL TIME + ADJUST )

Clock Tree Pulse Width **CIKTPW** ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE

Setup (DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + Setup

ADJUST )

Hold Hold ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +

ADJUST )

EndOfCycle EndOfC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +

- ADJUST )

ClockPulseWidth CIKPW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK

TRAILING EDGE

ClockSeparation ClkSep ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2

ARRIVAL TIME + ADJUST )

Loop ALTest ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM

CLOCK + ADJUST )

**Arrival Time Limiting ATLimit** Slack discontinuity due to failed test

Num/ LimitedAT/ Delay/ Failed Test/ Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj

NetName

1 dcd\_succ last t1 R C3+R 2668 -1669 3294 1011 1 PO dcd\_succ\_last\_t1

RAT 999

----> BOX714/OUT R C3+R 3294 1011 1 IOPAD 2668 -1669 **IOPAD** 0 dcd\_succ\_last t1

----> BOX714/IN R C3+R 2668 -1669 3294 1011 1 IOPAD **IOPAD** 

0 dcd succ last t1&0

----> C167/y R C3+R 2668 -1669 3294 1011 1 cs\_invvv 01c NOT

0 dcd\_succ\_last\_t1&0

----> C167/a FC3+R 1075 -1669 27 139 4 cs\_invvv 01c NOT

1594 N675

---->{a} C2738/y FC3+R 1075 -1669 27 139 4 cs nnd2x 14b NAND

0 14073	D CO D 4050 4000 00 444 4 55 mmd0v 44b NAND
> C2738/a	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND
19 last_cycle	D 00 D 4050 4000 00 444 4 co modey 140 NAND
>{b} C2487/y	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14e NAND
0 last_cycle	
> C2487/a	F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
21 N1587	AND NOT
> C1952/y	F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
N1587	401 NOT
> C1952/a	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
11 num_dcd_cyl&0(1)	
> ' BOX679/OUT	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD
0 num_dcd_cyl&0(1)	
> BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
num_dcd_cyl(1)	
> num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 PI 0
num_dcd_cyl(1)	
	Commence of the Commence of th
2 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO 0
iu_reset_op_c_t1	
RAT	999 0
> BOX716/OUT	R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
0 iu_reset_op_c_t1	
> BOX716/IN	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
0 iu_reset_op_c_t1&0	
>{a} C2393/y	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
0 iu_reset_op_c_t1&0	
> C2393/a	FC3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
1863 gbfonet_6	
> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT
0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031	
>{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031	
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	1 00111 000 1100 1111 211 0 112
> rcvry_reset_reg_n.lat_0/l2_ou	nt n F C3+R 358 -1400 144 217 5 cl_invvn 07d
SRL 0 rcvry_reset_q	<u> </u>
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	11 001 100 100 00 111 10 00 111
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB
	11001 100 100 00 222 10 00_3/\_022_1 200
0 slow_mode.c2_1	***************************************

<sup>&</sup>gt; msg::get\_highest\_level

0 N675

<sup>&</sup>gt; echo {Highest MsgLevel is error}

Highest MsgLevel is error

<sup>&</sup>gt; total\_area

<sup>&</sup>gt; echo {Total Area is 4676}

Total Area is 4676

<sup>&</sup>gt; critical\_slack

<sup>&</sup>gt; echo {Critical Slack is -1669.49328613}

Critical Slack is -1669.49328613

```
> slackhist DELTA(50),INTERVALS(10)
[slackhist]: CMVC version 1.6 compiled on Mar 31 1999 at 11:27:25.
[slackhist]: Slack delta 50.000000
[slackhist]: Max Intervals 10
[slackhist]: worst = -1669.49, best = 1019.49, stddev=716.94 maxfanout 20
[slackhist]: avg = -125.33, delta = 50.00, intervals = 10
[slackhist]:
Distribution of Slacks for All Nets
[slackhist]: Worst -1669.49. Best
                                1019.49
[slackhist]: Avg -125.33, Std Dev 716.94
[slackhist]:
            Low to
                    High: Number Percent Cum Percent
[slackhist]: -1700.00 to -1650.00:
                               7 0.62
                                           0.62
[slackhist]: -1650.00 to -1600.00:
                               10 0.89
                                            1.51
[slackhist]: -1600.00 to -1550.00:
                               26 2.30
                                           3.81
[slackhist]: -1550.00 to -1500.00:
                               17 1.51
                                           5.31
[slackhist]: -1500.00 to -1450.00:
                               15 1.33
                                           6.64
[slackhist]: -1450.00 to -1400.00:
                               28 2.48
                                           9.12
[slackhist]: -1400.00 to -1350.00:
                               13 1.15
                                           10.27
[slackhist]: -1350.00 to -1300.00:
                               10 0.89
                                           11.16
                                         .11.87
[slackhist]: -1300.00 to -1250.00:
                               8 0.71
[slackhist]: -1250.00 to -1200.00: 10 0.89 12.75
[slackhist]: Above -1200.00: 680 60.23 72.98
[slackhist]: Other nets: 305 27.02 100.00
  > write_end_point_report -points 2 -audit
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End....New Endpoint Report.
Sun Apr 18 22:09:38 1999
Part: IDCDSUC
Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38 Max. Slack: -1.13427E+38
Sort Field: Slack
                               Max. Endpoints: 2
 Cause of Slack
                       Abbreviation Comparison/Description
 Slack Continuation
                        SlkCont
                                   Slack due to a point downstream on path
 Required Arrival Time
                         RAT
                                   ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
 Asserted Required Arrival Time AssrtRAT
                                        ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
TIME)
 Clock Gating Setup
                         ClkGSet -
                                    ( DATA ARRIVAL TIME + CLOCK GATING SETUP. < CLOCK
ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                        ClkGHld
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
ARRIVAL TIME + ADJUST )
 Clock Tree Pulse Width
                          CIKTPW
                                      ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
TRAILING EDGE)
 Setup
                    Setup
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
ADJUST)
 Hold
                   Hold
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
ADJUST)
 EndOfCycle
                       EndOfC
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
ADJUST)
 ClockPulseWidth
                        CIkPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
```

	TRAILING EDGE ) ClockSeparation ClkS ARRIVAL TIME + ADJUST ) Loop ALTest CLOCK + ADJUST ) Arrival Time Limiting ATLi Num/ Test PinName NetName	( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
	1 dcd_succ_last_t1 dcd_succ_last_t1 RAT> BOX714/OUT	R C3+R 2668 -1669 3294 1011 1 PO 0 999 0 R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
	0 dcd_succ_last_t1> BOX714/IN 0 dcd_succ_last_t1&0	R C3+R 2668 -1669 3294 1011 1 IOPAD IOPAD
	> C167/y 0 dcd_succ_last_t1&0 > C167/a	R C3+R 2668 -1669 3294 1011 1 cs_invvv 01c NOT F C3+R 1075 -1669 27 139 4 cs_invvv 01c NOT
e	1594 N675 >{a} C2738/y 0 N675	F C3+R 1075 -1669 27 139 4 cs_nnd2x 14b NAND
: - : : - : : : : : : : : : : : : :	> C2738/a 19 last_cycle >{b} C2487/y	R C3+R 1056 -1669 33 114 1 cs_nnd2x 14b NAND  R C3+R 1056 -1669 33 114 1 cs_nnd2x 14e NAND
	0 last_cycle> C2487/a 21 N1587	F C3+R 1035 -1669 22 145 3 cs_nnd2x 14e NAND
	> C1952/y N1587	F C3+R 1035 -1669 22 145 3 cs_invvv 19b NOT 0
	> C1952/a 11 num_dcd_cyl&0(1) > BOX679/OUT	R C3+R 1024 -1669 80 319 1 cs_invvv 19b NOT
	0 num_dcd_cyl&0(1) > BOX679/IN num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 IOPAD IOPAD 0
	> num_dcd_cyl(1) num_dcd_cyl(1)	R C3+R 1024 -1669 80 319 1 PI 0
	2 iu_reset_op_c_t1 iu_reset_op_c_t1	R C3+R 2399 -1400 3318 1011 1 PO - 0 - 0 -
	RAT> BOX716/OUT 0 iu_reset_op_c_t1	999 0 R C3+R 2399 -1400 3318 1011 1 IOPAD IOPAD
	> BOX716/IN 0 iu_reset_op_c_t1&0	R C3+R 2399 -1400 3318 1044 3 IOPAD IOPAD
	>{a} C2393/y 0 iu_reset_op_c_t1&0 > C2393/a	R C3+R 2399 -1400 3318 1044 3 cs_nnd2v 02c NAND F C3+R 536 -1400 100 196 6 cs_nnd2v 02c NAND
	1863 gbfonet_6> gbfocell_6/y	F C3+R 536 -1400 100 196 6 cs_invvv 09c NOT

0 gbfonet_6	
> gbfocell_6/a	R C3+R 472 -1400 184 44 1 cs_invvv 09c NOT
64 N2031 >{b} C2162/y	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
0 N2031	R C3+R 472 -1400 184 44 1 cs_nnd3v 02c NAND
> C2162/a	F C3+R 358 -1400 144 217 5 cs_nnd3v 02c NAND
114 rcvry_reset_q	
> rcvry_reset.reg_n.lat_0/l2_ou SRL 0 rcvry_reset_q	t_n F C3+R 358 -1400 144 217 5 cl_invvn 07d
> rcvry_reset.reg_n.lat_0/c2	R C3+ 160 N/C 60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1	
> slow_mode.clockblock/c2	R C3+ 160 N/C 60 222 13 cb_clk_32_1 LCB <sup>-</sup>
0 slow_mode.c2_1	
******* Audit Secti	ion ************************************
Sun Apr 18 22:09:38 1999	
C41.7, p. 10 22.00.00 1000	Commence of the control of the commence of the
Part: IDCDSUC	
Compiled: Wed Mar 24 22:00:23 19	EDA EinsTimer Design Information
Release Level: 03.01	*** Wire model Information ***
n de la composition de la composition La composition de la	
Block WireModel1	ype CellCount ModelName
IDCDSUC Enclosed	d 4676 2kCells
Dia NACHARA	and the common of the control of the
Pin ModelName	
Pin ModelName	
Pin ModelName  Sun Apr 18 22:09:38 1999	
• •	
Sun Apr 18 22:09:38 1999  Part: IDCDSUC  Analysis: Late and Early / Nominal	EDA EinsTimer Design Information
Sun Apr 18 22:09:38 1999  Part: IDCDSUC  Analysis: Late and Early / Nominal  Compiled: Wed Mar 24 22:00:23 19	EDA EinsTimer Design Information
Sun Apr 18 22:09:38 1999  Part: IDCDSUC  Analysis: Late and Early / Nominal	EDA EinsTimer Design Information
Sun Apr 18 22:09:38 1999  Part: IDCDSUC  Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01	EDA EinsTimer Design Information
Sun Apr 18 22:09:38 1999  Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based	EDA EinsTimer Design Information
Sun Apr 18 22:09:38 1999  Part: IDCDSUC  Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01	EDA EinsTimer Design Information 199  *** General Information ***
Sun Apr 18 22:09:38 1999  Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default	EDA EinsTimer Design Information  *** General Information ***
Sun Apr 18 22:09:38 1999  Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12	EDA EinsTimer Design Information  *** General Information ***  LoadUnitToFarads= 1.00e-15
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00	EDA EinsTimer Design Information  199  *** General Information ***  LoadUnitToFarads= 1.00e-15  ResistanceUnitToOhms= 1.00e+03
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00 ClockGatingPulseWidth= 0.00ns	EDA EinsTimer Design Information  *** General Information ***  LoadUnitToFarads= 1.00e-15
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00 ClockGatingPulseWidth= 0.00ns	EDA EinsTimer Design Information  199  **** General Information ***  LoadUnitToFarads= 1.00e-15  D. ResistanceUnitToOhms= 1.00e+03  ClockGatingSetup= 0.00ns ClockGatingHold= 0.00ns
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00 ClockGatingPulseWidth= 0.00ns	EDA EinsTimer Design Information  199  **** General Information ***  LoadUnitToFarads= 1.00e-15  D. ResistanceUnitToOhms= 1.00e+03  ClockGatingSetup= 0.00ns ClockGatingHold= 0.00ns
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00 ClockGatingPulseWidth= 0.00ns Sun Apr 18 22:09:38 1999 Part: IDCDSUC	EDA EinsTimer Design Information  199  **** General Information ***  LoadUnitToFarads= 1.00e-15  D. ResistanceUnitToOhms= 1.00e+03  ClockGatingSetup= 0.00ns ClockGatingHold= 0.00ns
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00 ClockGatingPulseWidth= 0.00ns  Sun Apr 18 22:09:38 1999  Part: IDCDSUC Analysis: Late and Early / Nominal	EDA EinsTimer Design Information  *** General Information ***  LoadUnitToFarads= 1.00e-15  D. ResistanceUnitToOhms= 1.00e+03  ClockGatingSetup= 0.00ns ClockGatingHold= 0.00ns  EDA EinsTimer Design Information
Part: IDCDSUC Analysis: Late and Early / Nominal Compiled: Wed Mar 24 22:00:23 19 Release Level: 03.01  DTA Adjust Mode is Edge Based Clock Limiting is ON PinToPinNetModel is FALSE Analysis mode is default TimeUnitToSeconds= 1.00e-12 InductanceUnitToHenries= 1.00e+00 ClockGatingPulseWidth= 0.00ns Sun Apr 18 22:09:38 1999 Part: IDCDSUC	EDA EinsTimer Design Information  *** General Information ***  LoadUnitToFarads= 1.00e-15  D. ResistanceUnitToOhms= 1.00e+03  ClockGatingSetup= 0.00ns ClockGatingHold= 0.00ns  EDA EinsTimer Design Information

Block	Tech Name
IDCDSUC	GENERIC

Sun Apr 18 22:09:38 1999

Part: IDCDSUC

Analysis: Late and Early / Nominal

**EDA EinsTimer Design Information** 

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

\*\*\* Vtt, Vdd, Temp \*\*\*

Delay Factor WorstCase BestCase Nominal

Technology	Type	Worst(	Case I	BestCa	ase Nominal	
GENERIC	Current Tei	mp	10	-10	10	
	Current VCM	2	2	2		•
	Current VDD	1	2	1		
	Current VDD150	1	2	2		
	Current VDD180	2	2	2		•
*	Current VDD2	3	4	-3		-
	Current VDD250	2	. 3	· 2	·. · · -	
	Current VDD330	3	4	3		~
جان المانسيان سدو داندان	Current VDDQ	. 1	2	2		- '
	Current VREF	2	2	2		
	Current VTT	1	2	2		
	Base Temp	10	<del>-</del> 10	10		
	Base VCM	2	2	2 ·	• • • •	
	Base VDD	2	3	2		
	Base VDD150	1	2	2		
	Base VDD180	2	2	2	· .	
	Base VDD2	3	4	3	•	
	Base VDD250	2	3	2	•	•
-	Base VDD330	3	4	3		
-	Base VDDQ	1	2	2	* * * * * * * * * * * * * * * * * * * *	-
•	Base VREF	2.	2	2		
	Base VTT	1	2	2		

## Sun Apr 18 22:09:38 1999

Part: IDCDSUC

Analysis: Late and Early / Nominal

**EDA EinsTimer Design Information** 

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

\*\*\* Voltage Island Information \*\*\*

Island	Technology	Rail	WorstCase BestCase Nominal
Cell	Island		

Block	Island			******				
Sun Apr 18 22:0  Part: IDCDSUC Analysis: Late a Compiled: Wed Release Level:  *Phase Tleading*	nd Early / Nomir Mar 24 22:00:23 03.01	3 1999	A EinsTime Phases Del	 r Design Info initions ***	rmation			
C3 0 C3L 0	600 1200 600 1200							
CLK_OVERRIDI *Clock ATr(L) *		L) SLwf(L)	ATr(E) A1	f(E) SLwr(E	E) SLwf(I	E)	- · · · · · · ·	
C3 160 C3L 160 *	750 60 750 60	60 160 60 160		60 60 60 60				
CLK_TREE_OVI *Clock ATr(L) * CLK_PAIR_EXC *Clock1 Clock2 *	ATf(L) SLwr(I	L) SLwf(L)		f(E) SLwr(E	E) SLwf(I	<b>É)</b>		
USER_DELTA_/ *Clock1 Clock2 E			Adjust	· · · · · · · · · · · · · · · · · · ·				ng Arman sa Ang Language sa sa
Sun Apr 18 22:09 Part: IDCDSUC Analysis: Late a Compiled: Wed Release Level: 0	nd Early / Nomin Mar 24 22:00:23	3 1999		Design Info				• 00 ••
Pin Signal/Net	Phase ATr(L)	ATf(L) SL	wr(L) SLw	(L) ATr(E)	ATf(E)	SLwr(E	E) SLwf(E)	
op_dsbl_after op_dsbl_after eu_iu_spare1 eu_iu_spare1 second_op_lat second_op_lat	C3+R 1 C3+R C3+R	022 1101 465 430 465 437		80 391 195 215 80 263	387 196 251	83 80 80	80 80 80	- <del></del>

						405	007	000	00	00 m or 41	tron		
	mcr41_trap	C3+R	700	674	125	105	287	283	80 02 - 3	_80 mcr41_ 87 ifet_xcpt	•		
	ifet_xcptn	C3+R	931			17 3 98	351 3 272	58 1 258	80	80 80	•		
	iu_eu_xcpt_pend		491	468	117	90	212	230	00	00			
	iu_eu_xcpt_pend	C3+R	580	570	108	110	278 2	274	80	80 iq_blk_d	1		
	iq_blk_d1	C3+R	401	401	151	151	101	101	151	151 clkl_m			
	clkl_mode7 dcd_op_44	C3+R	854	807	86					80 dcd_op_			
	ru_write_in_iq	C3+R	672	715	147	159	227	218	80	80			
	ru_write_in_iq	00111	. 0,2										
	a_clk	C3+R	401	401 1	51 15	51 10	)1 10			51 a_clk			
	b_clk	C3+R		101 1	151 15	51 10				51 b_clk			
	ru_iu_rcvy_rst	C3+R	700	700	151	151 9	99000	999000	15	1 151			
	ru_iu_rcvy_rst												
	eu_iu_enter_slow	v_md C3	+R 8	337 8	316 35	52 34	16 27	0 25	8 8	0 80			
	eu_iu_enter_slow			4400	470	400	400	406	129	80			
	id_instr_stores	C3+R	1149	1163	176	100	430	400	129	80			
	id_instr_stores	00 · D	000	384	112	108	210	212	80	80			
	op_inq_stores	C3+R	386	304	112	100	210	212	00				**
	op_inq_stores	C3+R	401	401	151 1	51 1	01 1	01 1	51 1	51 test_c1			
	test_c1 iq_blk_aa	C3+R	518	532	105					80 iq_blk_aa	a		
	aa_ofc_available					119	210	207	80	80			
	aa_ofc_available					•				••			
	eu_iu_mmode	C3+F	693	667	326	326	327	304	80	80			
	eu_iu_mmode		******	t, e tija	ingerie geweier Ta								
· · · · · ·	eu_iu_mcset_e1	C3+F	R 84	3 778	B 248	248	313	298	80	- 80			4
••,	eu_iu_mcset_e1				- 440	04	010	199	80	80 aa_ofc_	hold		
	aa_ofc_hold	C3+R	415	371 421	149	91	218 243 2			80 aa_0.c. 80 ru_98_43			
	ru_98_43	C3+R C3+R	428 1281			80 -		355	80	80 80	-		
	srlz_op_match srlz_op_match		120	,			•						
	JIL OF INGLO							•					
		C3+R	452	452	115	84 2	247 2	254		30 first_op_l	at		- ***
	first_op_lat	C3+R C3+R	452 556			84 2	247 2 314.	254 8 304	80 80	30 first_op_l 80	at	-	- ***
		C3+R IES	. 556	537	80	80	314.	304	80	80	at .		- ****
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk	C3+R	. 556	537	80						at :		
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk	C3+R IES C3+F	556 8 850	5 537 5 835	80 5 80	80	314 314	304	80	80	at		- ***
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy	C3+R IES C3+F C3+R	556 R 850	5 537 5 835	80 5 80	80	314.	304	80	80	at		
. · ·	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy	C3+R IES C3+F C3+R	556 8 850 817	5 537 0 835 7 863	80 80 193	80 80 193	314 314 368	304 311 360	80 80 80	80 80 80	at		
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t	C3+R HES C3+F C3+R	556 8 850 817	5 537 5 835	80 80 193	80 80 193	314 314 368	304	80 80 80	80 80 80	at		
. ·	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t du_iu_hold_aa_t	C3+R C3+F C3+R req C3+	556 8 850 817 -R 5	5 537 0 835 7 863 58 55	80 5 80 193 57 42	80 80 193 4 424	314 314 368 4 243	304 311 360 3 246	80 80 80 80	80 80 80 0 80	at		
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_l du_iu_hold_aa_l eu_iu_fpu_end_e	C3+R C3+F C3+R req C3+ req C3+ req C3+	556 8 850 817 -R 5	5 537 0 835 7 863 58 55	80 80 193	80 80 193 4 424	314 314 368 4 243	304 311 360 3 246	80 80 80 80	80 80 80 0 80	at		- *** 
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t du_iu_hold_aa_t eu_iu_fpu_end_eu_iu_fpu_end_eu_iu_fpu_end_e	C3+R C3+F C3+R req C3+ req C3+ req C3+ op C3+	556 8 850 817 -R 59	5 537 0 835 7 863 58 55 69 6	80 5 80 193 57 42 15 33	80 80 193 4 424 9 338	314 314 368 4 243 8 283	304 311 360 3 246	80 80 80 80	80 80 80 0 80			. *** 
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t du_iu_hold_aa_t eu_iu_fpu_end_eu_iu_fpu_end_eu_iu_misc_hold	C3+R C3+F C3+R req C3+ req C3+ req C3+ op C3+ d C3+I	556 8 850 817 -R 59	5 537 0 835 7 863 58 55 69 6	80 5 80 193 57 42 15 33 0 332	80 80 193 4 424 9 336 310	314 314 368 4 243 8 283 210	304 311 360 3 246 3 274 201	80 80 80 6 80 1 80	80 80 80 80 80 80	at		
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t du_iu_hold_aa_t eu_iu_fpu_end_eu_iu_fpu_end_eu_iu_fpu_end_e	C3+R C3+F C3+R req C3+ req C3+ req C3+ op C3+ d C3+I	556 8 850 817 -R 59 -R 60 -R 49	5 537 0 835 7 863 58 55 69 6 9 460	80 5 80 193 57 42 15 33 0 332	80 80 193 4 424 9 338	314 314 368 4 243 8 283	304 311 360 3 246 3 274	80 80 80 6 80 1 80	80 80 80 0 80 0 80			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_u du_iu_hold_aa_u eu_iu_fpu_end_u eu_iu_fpu_end_u eu_iu_misc_hold eu_iu_misc_hold	C3+R C3+F C3+R req C3+ req op C3+ op d C3+F	556 8 850 817 -R 55 -R 66 R 49	5 537 0 835 7 863 58 55 69 6 9 460 3 818	80 80 193 57 42 15 33 0 332 8 80	80 80 193 4 424 9 338 310 80	314 314 368 4 243 8 283 210 354	304 311 360 3 246 3 274 201 362	80 80 80 80 80 80	80 80 80 80 80 80			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_l du_iu_hold_aa_l eu_iu_fpu_end_eu_iu_fpu_end_eu_iu_misc_hold op_cmp_raw op_cmp_raw op_dsbl_before	C3+R C3+F C3+R req C3+ req C3+ req op C3+ op d C3+I	556 8 850 817 -R 55 -R 66 R 49	5 537 0 835 7 863 58 55 69 6 9 460 3 818	80 80 193 57 42 15 33 0 332 8 80	80 80 193 4 424 9 336 310	314 314 368 4 243 8 283 210	304 311 360 3 246 3 274 201	80 80 80 6 80 1 80	80 80 80 80 80 80			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t du_iu_hold_aa_t eu_iu_fpu_end_t eu_iu_fpu_end_t eu_iu_misc_hold op_cmp_raw op_cmp_raw op_dsbl_before op_dsbl_before	C3+R C3+F C3+R req C3+ req C3+ op C3+ d C3+F C3+F	556 8 850 817 R 55 R 66 R 49 R 858 R 755	5 537 0 835 7 863 58 55 69 6 9 466 8 818 5 728	80 80 193 57 42 15 33 0 332 8 80 8 80	80 80 193 4 424 9 338 310 80 80	314 314 368 4 243 8 283 210 354 407	304 311 360 3 246 3 274 201 362 394	80 80 80 80 80 80	80 80 80 80 80 80 80			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_l du_iu_hold_aa_l eu_iu_fpu_end_l eu_iu_fpu_end_l eu_iu_misc_hold op_cmp_raw op_cmp_raw op_dsbl_before op_drain	C3+R C3+R C3+R req C3+ req op C3+ op d C3+R C3+R C3+R	556 8 850 817 R 56 R 66 R 49 R 858 R 755	5 537 0 835 7 863 58 55 69 6 9 466 8 818 5 728	80 5 80 193 57 42 15 33 0 332 6 80 8 80	80 80 193 4 424 9 338 310 80 80	314 314 368 4 243 8 283 210 354 407	304 311 360 3 246 3 274 201 362 394	80 80 80 80 80 80 80	80 80 80 9 80 9 80 80 80 80			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_t du_iu_hold_aa_t eu_iu_fpu_end_eu_iu_misc_hold op_cmp_raw op_cmp_raw op_cmp_raw op_dsbl_before op_drain eu_iu_fxu_end_eu_iu_fxu_end_eu_iu_fxu_end_	C3+R C3+R C3+R req C3+ req op C3+ op C3+R C3+R C3+R C3+R op C3+R	556 8 850 817 R 56 R 66 R 49 R 858 R 755	5 537 0 835 7 863 58 55 69 6 9 466 8 818 5 728	80 80 193 57 42 15 33 0 332 8 80 8 80	80 80 193 4 424 9 338 310 80 80	314 314 368 4 243 8 283 210 354 407	304 311 360 3 246 3 274 201 362 394	80 80 80 80 80 80 80	80 80 80 9 80 9 80 80 80 80			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_I du_iu_hold_aa_I eu_iu_fpu_end_eu_iu_misc_holo eu_iu_misc_holo op_cmp_raw op_cmp_raw op_dsbl_before op_dsbl_before op_drain eu_iu_fxu_end_eu_iu_fxu_end_eu_iu_fxu_end_eu_iu_fxu_end_eu_iu_fxu_end_eu_iu_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_end_ex_fxu_e	C3+R C3+R C3+R req C3+ req op C3+ op C3+R C3+R C3+R C3+R op C3+ op C3+ op C3+	556 8 850 817 -R 56 -R 69 8 858 8 755 -R 6	5 537 0 835 7 863 58 55 69 6 9 466 3 818 5 728 809 72 65	80 5 80 193 57 42 15 33 0 332 6 80 8 80 8 80 8 82 51 28	80 80 193 4 424 9 336 310 80 80 80 3 6 28	314 314 368 4 243 8 283 210 354 407 879 3 1 276	304 311 360 3 246 3 274 201 362 394 32 1 6 280	80 80 80 80 80 80 80	80 80 80 80 80 80 80 102 op_drain			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_i du_iu_hold_aa_i eu_iu_fpu_end_i eu_iu_fpu_end_i eu_iu_misc_hold op_cmp_raw op_cmp_raw op_cmp_raw op_dsbl_before op_dsbl_before op_drain eu_iu_fxu_end_i eu_iu_fxu_end_i op_mcend_raw	C3+R C3+R C3+R req C3+ req op C3+ op C3+R C3+R C3+R C3+R op C3+R	556 8 850 817 -R 56 -R 69 8 858 8 755 -R 6	5 537 0 835 7 863 58 55 69 6 9 466 3 818 5 728 809 72 65	80 5 80 193 57 42 15 33 0 332 6 80 8 80 8 80 8 82 51 28	80 80 193 4 424 9 338 310 80 80	314 314 368 4 243 8 283 210 354 407	304 311 360 3 246 3 274 201 362 394	80 80 80 80 80 80 80	80 80 80 9 80 9 80 80 80 80			
	first_op_lat zero_branches ZERO_BRANChdcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_i du_iu_hold_aa_i eu_iu_fpu_end_eu_iu_fpu_end_eu_iu_misc_hold op_cmp_raw op_cmp_raw op_cmp_raw op_dsbl_before op_dsbl_before op_drain eu_iu_fxu_end_eu_iu_fxu_end_op_mcend_raw op_mcend_raw	C3+R dES C3+F C3+R req C3+ op C3+ op C3+F C3+F C3+F C3+R op C3+	556 8 850 817 -R 55 -R 66 8 858 8 755 -R 66 R 85	5 537 0 835 7 863 58 55 69 6 9 46 8 818 5 728 809 72 65 50 81	80 80 193 57 42 15 33 0 332 8 80 8 80 8 82 51 28 0 91	80 80 193 4 424 9 336 310 80 80 80 80 80 85	314 314 368 4 243 8 283 210 354 407 879 3 1 276 369	304 311 360 3 246 3 274 201 362 394 32 1 6 280	80 80 80 80 80 80 80	80 80 80 80 80 80 80 102 op_drain			
	first_op_lat zero_branches ZERO_BRANCH dcd_mcr41_blk dcd_mcr41_blk xu_iu_xlat_busy xu_iu_xlat_busy du_iu_hold_aa_i du_iu_hold_aa_i eu_iu_fpu_end_i eu_iu_fpu_end_i eu_iu_misc_hold op_cmp_raw op_cmp_raw op_cmp_raw op_dsbl_before op_dsbl_before op_drain eu_iu_fxu_end_i eu_iu_fxu_end_i op_mcend_raw	C3+R C3+F C3+R req C3+ req C3+ op C3+ d C3+F C3+F C3+R op C3+ op C3+ op C3+ cop C3+	556 8 850 817 -R 55 -R 66 8 858 8 755 -R 66 R 85	5 537 0 835 7 863 58 55 69 6 9 46 8 818 5 728 809 72 65 50 81	80 80 193 57 42 15 33 0 332 8 80 8 80 8 82 51 28 0 91	80 80 193 4 424 9 336 310 80 80 80 80 80 85	314 314 368 4 243 8 283 210 354 407 879 3 1 276 369	304 311 360 3 246 3 274 201 362 394 32 1 5 280 372	80 80 80 80 80 80 80 34 0 80	80 80 80 80 80 80 80 102 op_draid 9 80			

need_opnd_req	C3+R	384	368	80	80	219	209	80	80		
need_opnd_req											
legal_bht_br	C3+R	1358	1386	84	84	376	380	80	80 legal_bht	_br	
•	C3- 60		160	160	600	0	160	160 c			
bht_branch_req	C3+R	401	401	151	151	101	101	151	151		
bht_branch_req											
id_ex_in_mm	C3+R	1291	1371	123	92	450	475	80	80		
id_ex_in_mm	00. 0		-04	200							
du_iu_quiesced	C3+R	537	521	338	338	244	227	80	80		
du_iu_quiesced	C3+R	005	900	90	00	250	000	00	00		
iu_op_cmp_hit_a iu_op_cmp_hit_a	US+n	835	809	80	80	350	366	80	80		
iu_op_cmp_hit_b	C3+R	829	802	80	80	345	362	80	80		
iu_op_cmp_hit_b	00711	023	002	00	80	343	302	60	80		
iu_op_cmp_hit_c	C3+R	814	787	80	80	336	357	80	80		
iu_op_cmp_hit_c	00111	014	, 0,		00	000	037	00	00		
iu_op_cmp_hit_d	C3+R	808	780	80	80	335	355	80	80		
- iu_op_cmp_hit_d							000				
dcd_frc_milli	C3+R	1157	1158	80	80	370	395	80	80 dcd_frc_n	nilli	-
iq_empty	C3+R				108	307	296	80	80 iq_empty		
op_serialize	C3+R	802	756	80	80	372		80	80 op_serialize	e	
gptr_scan_in	C3+R	401	401	·151 ···	151 .	101	101	151	151		Agent Land
gptr_scan_in											
aa_agi_lat	C3+R				115	223	225		,80 aa_agi_lat	L	
branch_request	C3+R	386	385	118	113	_ 210	211	80	80		9 - 4 1 E
branch_request					· · · · · ·						
ru_9a_52	C3+R		358					80	80 ru_9a_52		
bu_iu_quiesced	C3+R	664	644	236	236	280	261	. 80	80	received the	Sharman Make Same
bu_iu_quiesced		000	000	00	. 00	004	050	- 00			
dcd_blk_dsucc dcd_blk_dsucc	C3+R	868	829	. 80	80	- 381	359	80	80		The second
op_eim_dcd	C3+R	1202	1217	82	80	331	366	80	80		-
op_eim_dcd	00711	1202	1217	02	80	331	300	60	<b>6</b> 0		
igmcode_mod_39	0gr C3+	-R 7	14 68	37 8	ი 8	0 29	93 29	15 A	80 80	:	
igmcode_mod_39							. 20		.00	,	
scan_in	C3+R	401 4	01 1	51 1	51	101	101	151	151	e e vige i se e e e vi	
scan_invec(0)		-							, , ,		
eu_iu_e1_exc_cor	nd C3+F	R 75	7 72	7 27 <sup>-</sup>	26	30	)1 27	'2 8	80 80		*
eu_iu_e1_exc_co											
aa_ofc_block_req											
aa_ofc_block_req	C3+R	405	402	129	129	211	210	80	80		
eu_iu_fpu_excpn	C3+R C3+R	405 537	402 512	129 183	129 183			80 80			
eu_iu_fpu_excpn eu_iu_fpu_excpn	C3+R	537	512	183	183	269	251	80	80		
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch						269	251	80	80		
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch	C3+R C3+R	537 506	512 520	183 114	183 114	269 280	251 292	80	80 80		
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch ru_iu_rq_blk	C3+R C3+R C3+R	537 506 780	512 520 740	183 114 184	183 114 184	269 280 348	251 292 339	80 80	80 80 80 ru_iu_rq_	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch ru_iu_rq_blk op_chkpt_synch	C3+R C3+R	537 506	512 520	183 114	183 114	269 280	251 292	80	80 80	blk ·	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch ru_iu_rq_blk op_chkpt_synch op_chkpt_synch	C3+R C3+R C3+R C3+R	537 506 780 800	512 520 740 773	183 114 184 80	183 114 184 80	269 280 348 366	251 292 339 351	80 80 80 80	80 80 80 ru_iu_rq_ 80	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch ru_iu_rq_blk op_chkpt_synch op_chkpt_synch ireg_valid	C3+R C3+R C3+R C3+R	537 506 780 800 779 7	512 520 740 773	183 114 184 80 05 1	183 114 184 80	269 280 348 366 275	251 292 339 351 278	80 80 80 80	80 80 80 ru_iu_rq_ 80 80 ireg_valid	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch ru_iu_rq_blk op_chkpt_synch op_chkpt_synch ireg_valid ru_9a_36	C3+R C3+R C3+R C3+R C3+R C3+R	537 506 780 800 779 7 371	512 520 740 773 99 1 363	183 114 184 80 05 1 81	183 114 184 80 17	269 280 348 366 275 204	251 292 339 351 278 199	80 80 80 80 80	80 80 ru_iu_rq_ 80 80 ireg_valid 80 ru_9a_36	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch rlu_iu_rq_blk op_chkpt_synch op_chkpt_synch ireg_valid rlu_9a_36 three_branches	C3+R C3+R C3+R C3+R	537 506 780 800 779 7	512 520 740 773	183 114 184 80 05 1	183 114 184 80	269 280 348 366 275	251 292 339 351 278	80 80 80 80	80 80 80 ru_iu_rq_ 80 80 ireg_valid	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch rlu_iu_rq_blk op_chkpt_synch op_chkpt_synch ireg_valid rlu_9a_36 three_branches three_branches	C3+R C3+R C3+R C3+R C3+R C3+R	537 506 780 800 779 7 371 583	512 520 740 773 99 1 363 598	183 114 184 80 05 1 81 110	183 114 184 80 17 2 81 81	269 280 348 366 275 204 302	251 292 339 351 278 199 284	80 80 80 80 80 80	80 80 ru_iu_rq_ 80 80 ireg_valid 80 ru_9a_36 80	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch rlu_iu_rq_blk op_chkpt_synch op_chkpt_synch ireg_valid rlu_9a_36 three_branches	C3+R C3+R C3+R C3+R C3+R C3+R	537 506 780 800 779 7 371	512 520 740 773 99 1 363	183 114 184 80 05 1 81	183 114 184 80 17	269 280 348 366 275 204	251 292 339 351 278 199	80 80 80 80 80	80 80 ru_iu_rq_ 80 80 ireg_valid 80 ru_9a_36	blk	
eu_iu_fpu_excpn eu_iu_fpu_excpn block_aa_branch block_aa_branch ru_iu_rq_blk op_chkpt_synch op_chkpt_synch ireg_valid ru_9a_36 three_branches three_branches bht_block_dcd	C3+R C3+R C3+R C3+R C3+R C3+R	537 506 780 800 779 7 371 583 401	512 520 740 773 99 1 363 598	183 114 184 80 05 1 81 110	183 114 184 80 17 81 81 81	269 280 348 366 275 204 302 101	251 292 339 351 278 199 284 101	80 80 80 80 80 80 86	80 80 ru_iu_rq_ 80 80 ireg_valid 80 ru_9a_36 80	blk	

	iu_eu_data_blocked	C3+R	410	406	125	123	223	224	80	80		
	iu_eu_data_blocked		- 10			404	10-	4 454	151			
	Jr	3+R 40					10			gptr_a_clk		
	J	3+R 40					10°			gptr_b_clk		
	, = -		39 93			507	475			_is_44		
					80 80					st_fetches		
	clkg2 C3-		0	160					0 clkg2	00		
	eu_iu_fxu_exc_cond	C3+R	988	953	390	390	371	354	80	80		
	eu_iu_fxu_exc_cond		0-			204	100	90	90 21	00.04		
				72 82		204	198			_9a_04 0		
	br_wrong_targ	C3+R	1171	1099	175	82 3	62	349 1	00 8	0		
	br_wrong_targ	22 D			^^ 0	·- 0001	ם פיי		80	80		
	<del>_</del>	C3+R	1045	1039	86 8	1 9991	1/2 v	99172	80	80		
	scan_enable		E A 1	508	289	289	252	231	80	80		
	du_iu_store_status(0)		541	500	20 <del>3</del>	20 <del>3</del>	202	201	00	00		
	du_iu_store_status(0) du_iu_store_status(1)		527	507	276	276	246	233	80	80		
	du_iu_store_status(1)	•	JL1	50,	210	210	240	200	00			
	du_iu_store_status(2)	•	691	649	500	500	256	236	500	500	-	
	du_iu_store_status(2)	•	00.	0.0	<b>000</b>	-			•••	•••		
	eu_iu_srlz_op_actn(0		544	557	366	374	225	218	80	80		
	eu_iu_srlz_op_actn(0	•	•	<del>-</del> -		-						
	eu_iu_srlz_op_actn(1		1344	1348	341	341	267	249	80	80	•	-
	eu_iu_srlz_op_actn(1	•		-								
	ru_9a_0001(0)	C3+R	387	381	86 8	6 207	7 2	03 80	80	· ,	• • • • •	
	ru_9a_0001(0)		i gg i	Compression (							 •	4 24
-	ru_9a_0001(1)	C3+R	387	381	86 8	6 20	7 2	02 80	80			-
	ru_9a_0001(1)	a in a more when,			72 172	2 236		 29         80	 20 i	reg_0_1(0)	and an order of the second sec	- united any refer to the
	ireg_0_1(0) C	C3+R 4	40 4	28 - 17	/ク 1/2	<i>)</i>	. ,	/U × × 1	80 1	rea u noi		_
	<del>0</del> · <i>,</i>											
	ireg_0_1(1) - C	C3+R 4	40 4	28 17	77 177	7 236	23	80 80	80 i	reg_0_1(1)		
	ireg_0_1(1) C num_dcd_cyl(0)	C3+R 4 C3+R				7 236	23	80 80	80 i			
The second play day of the second sec	ireg_0_1(1) C num_dcd_cyl(0) num_dcd_cyl(0)	C3+R 4 C3+R	140 4 1040	28 17 1088	77 177 80	7 236 80 4	6 23 114	80 80 453	80 ii 80 8	reg_0_1(1) 4		
· · · · · · · · · · · · · · · · · · ·	ireg_0_1(1) C num_dcd_cyl(0) num_dcd_cyl(0) num_dcd_cyl(1)	C3+R 4 C3+R	40 4	28 17	77 177	7 236 80 4	23	80 80 453	80 ii 80 8	reg_0_1(1)		
	ireg_0_1(1) C num_dcd_cyl(0) num_dcd_cyl(0) num_dcd_cyl(1) num_dcd_cyl(1)	C3+R 4 C3+R  C3+R	140 43 1040 1024	28 17 1088 1016	77 177 80 80	7 236 80 4 80 3	5 23 114 399	80 80 453	80 i 80 8 80 8	reg_0_1(1) 4 0		
	ireg_0_1(1) C num_dcd_cyl(0) num_dcd_cyl(0) num_dcd_cyl(1) num_dcd_cyl(1) ru_9a_3233(32)	C3+R 4 C3+R	140 4 1040	28 17 1088	77 177 80 80	7 236 80 4	5 23 114 399	30 80 453 387	80 i 80 8 80 8	reg_0_1(1) 4 0		
	ireg_0_1(1) num_dcd_cyl(0) num_dcd_cyl(0) num_dcd_cyl(1) num_dcd_cyl(1) ru_9a_3233(32) ru_9a_3233(32)	C3+R 4 C3+R C3+R C3+R	1040 1040 1024 373	28 17 1088 1016	77 177 80 80 81 8	7 236 80 4 80 3	6 23 114 399 07 2	30 80 453 387	80 i 80 8 80 8 0 80	reg_0_1(1) 4 0		
	ireg_0_1(1) C num_dcd_cyl(0) num_dcd_cyl(0) num_dcd_cyl(1) num_dcd_cyl(1) ru_9a_3233(32)	C3+R 4 C3+R  C3+R	140 43 1040 1024	28 17 1088 1016 365	77 177 80 80 81 8	7 236 80 4 80 3 81 20	3 23 114 399 07 2	30 80 453 387 203 8	80 i 80 8 80 8 0 80	reg_0_1(1) 4  0		
	ireg_0_1(1) num_dcd_cyl(0) num_dcd_cyl(1) num_dcd_cyl(1) ru_9a_3233(32) ru_9a_3233(33) ru_9a_3233(33)	C3+R 4 C3+R C3+R C3+R C3+R	1040 1040 1024 373	28 17 1088 1016 365	77 177 80 80 81 8	7 236 80 4 80 3 81 20	6 23 114 399 07 2	30 80 453 387 203 8	80 i 80 8 80 8 0 80	reg_0_1(1) 4 0		
	ireg_0_1(1) num_dcd_cyl(0) num_dcd_cyl(0) num_dcd_cyl(1) num_dcd_cyl(1) ru_9a_3233(32) ru_9a_3233(32) ru_9a_3233(33) ru_9a_3233(33) eu_iu_interrupt_info(0) eu_iu_interrupt_info(0)	C3+R 4 C3+R C3+R C3+R C3+R C3+R 0) C3+R	140 4: 1040 1024 373 375 1260	28 17 1088 1016 365 366 1237	77 177 80 80 81 8 81 8	7 236 80 4 80 3 31 20 31 20	3 23 114 399 07 2 08 2	30 80 453 387 203 8 203 8	80 i 80 8 80 8 0 80 0 80	reg_0_1(1) 4 0		
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ru_9a_4849(48)	00 B	0.70				222				•
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ireg_1631(22)	C3+R	423	-412	129	129	229	222	80 .	. 80	
ireg_1631(22) ireg_1631(23)	C3+R	410	400	101	101	224	218	80	00	
ireg_1631(23)	Co+n	410	400		. 101	224	218	- 80	80	
ireg_1631(24)	C3+R	422	. 111	107	127	228	222	80	80	
ireg_1631(24)	COTI	444	<del> </del>	121	12/	,220		οŲ	ου	*** * . * . * . * .
ireg_1631(25)	C3+R	422	411	126	126	224	217	80	80	
ireg_1631(25)	00111	76-6-				227			00	
ireg_1631(26)	C3+R	427	416	133	133	230	223	80	80	· · · · · · · · · · · · · · · · · · ·
ireg_1631(26)								, 00	-	
ireg_1631(27)	C3+R	420	410	118	118	230	224	80	80	
ireg_1631(27)			##						77-,	
ireg_1631(28)	C3+R	436	421	140	134	244	237	90	80	· · · · · · · · · · · · · · · · · · ·
ireg_1631(28)										•
ireg_1631(29)	C3+R	436	. 422	141	138	243	236	88	80	
ireg_1631(29)										
ireg_1631(30)	C3+R	439	423	144	134	245	239	93	80	
ireg_1631(30)										
***************************************										

Sun Apr 18 22:09:38 1999

Part: IDCDSUC

Analysis: Late and Early / Nominal

**EDA EinsTimer Design Information** 

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01 \*\*\* POs and Asserted Re

\*\*\* POs and Asserted Required Arrival Times and CAP data \*\*\*

Pin	Phase F	RATr(L) I	RATf(L)	RATr(E)	RATf(E	E) Cap	Signal/Net
iu_eu_opcode_ci iu_rcvry_reset iu_reset_op_c	mp C C3+R C3+F		1085		199	1099 N	

```
999
                                      999
                                             -999
                                                    -999 1001 dcd_succ_last_t1
                    C3+R
dcd_succ_last_t1
                  C3+R
                             400
                                    400
                                            126
                                                   125
                                                        633 N12
iu milli_mode
                                                    -999 1001 iu_reset_op_c_t1
                              999
                                     999
                                            -999
                    C3+R
iu reset_op_c_t1
                                            224
                                                   229 964 N2086
                             929
                                     879
dcd_succ_last
                   C3+R
                                       835
                                               84
                                                      69 1208 N26
                      C3+R
                                835
iu_eu_op_nomatch
                                             205
                                                        411 ds_1st_maybe
                    C3+R
                              866
                                     897
                                                    198
ds_1st_maybe
                                                   246 434 N34
                  C3+R
                             470
                                    400
                                           243
id_xcute_targ
                                                    142 365 N14
                              400
                                     400
                                            101
                   C3+R
xc_frc_ia_to_if_t1
                                           -999160 -999129 531 N2097
                                     1060
                              1060
dcd_success_tr
                    C3+R
                                                     237 786 dsucc_or_agi_n
                              1060
                                      1081
                                              230
dsucc_or_agi_n
                    C3+R
                             1006
                                     976
                                             197
                                                    192
                                                         441 dsucc_or_agi
                   C3+R
dsucc_or_agi
                                             182
                                                    175
                                                          538 NO
                    C3+R
                              468
                                     443
iu_slow_mode
                             1060
                                     1038
                                             131
                                                     139
                                                          258 slwmd blk n
                   C3+R
slwmd_blk_n
                                                 102 192 N16
                           569
                                  516
                                          114
xc frc milli
                 C3+R
                                     1067
                                              198
                                                     207
                                                           344 dcd_succ_first_t1
dcd_succ_first_t1
                    C3+R
                              1060
                 C3+R
                                                 188
                                                       746 iu reset all
                           980
                                   924
                                          202
iu_reset_all
                                             33
                                                    63
                                                        314 N2089
                              400
                                     400
iu_milli_mode_t1
                    C3+R
                                                     169 288 N72
                              1060
                                     1142
                                              181
iu_milli_mode_t2
                    C3+R
                                                    228 632 N2090 ·
                              708
                                     644
                                             235
iu_milli_mode_t3 --
                    C3+R
                                                   96 300 N42
                                    400
xc_frc_milli_t1
                            400
                                           104
                  C3+R
                                                    203 208 N2096
                             1060
                                     1223
                                             221
iu_exc_cond
                   C3+R
                                     1060 -999089 -999055 570 N80
                             1060
                   C3+R
slow_mode_tr
                                       1117
                                                       235 1195 N22
                                                238
                      C3+R
                               1060
iu eu slow mode
                                     1030
                                                     228 1112 dcd_success
                             1016
                                             234
dcd_success
                   C3+R
                                             83 .....
                                                    94 537 N70
                              596
                                     548
iu_milli_mode_tr
                   C3+R
                                                 121 206 N140
                           557
                                  628
                                          124
iu_reset_if
                 C3+R
                                          -999070 -999051 570 N78
exc_cond_tr
                   C3+R
                            1060
                                    1060
                                            184
                                                   187 406 N2088
dcd_succ_first
                   C3+R
                             816
                                    805
                                             207
                                                     184
                                                          278 N136
execute_recovery
                     C3+R
                               630
                                      594
                                     1225
                                              185
                                                     195
                                                           89 execute_xcptn
execute_xcptn
                   C3+R
                             1060
                                    732
                                                  149
                                                       437 N8
                  C3+R
                             763
                                           174
xc_frc_ia_to_if
                                             -999
                                                     -999 1001 N18
                     C3+R
                               999
                                       999
iu slow_mode_t1
                                                   -999 1000 gptr_scan_out&1
                   C3+R
                              999
                                     999
                                            -999
gptr_scan_out
                            400
                                   400
                                           187
                                                  180
                                                       218 N4
                  C3+R
iu_reset_fst
                            999
                                   999
                                          -999
                                                 -999
                                                        106 scan_out
                  C3+R
scan out
                               843
                                       769
                                               80
                                                      52 1160 N134
                     C3+R
iu_eu_dcd_succ_tr
                                    999
                                           -999
                                                  -999 1001 N146
                  C3+R
                            999
idcdsuc_err
                                 400
                                         134
                                                108
                                                     643 N10
                          400
                C3+R
frc milli
                                                    131
                                                         105 N2092
                                             135
                   C3+R
                             1060
                                     1020
iu_intrupt_info(0)
                                     888
                                             68
                                                   49
                                                        94 N2093
iu_intrupt_info(1)
                   C3+R
                             942
                                                    133
                                                          105 N2094
                   C3+R
                             1060
                                     1024
                                             134
iu_intrupt_info(2)
                             1060
                                     1016
                                             131
                                                    132
                                                          105 N2095
iu_intrupt_info(3)
                   C3+R
                                      1060
                                            -999153
                                                     -999134
                                                               543 N126
                              1060
                    C3+R
blk_dcd_info_tr(0)
                                            -999153
                                                     -999134
                                                               543 N128
                                      1060
                              1060
blk dcd info_tr(1)
                    C3+R
                                                     -999135
                                                               543 N130
                    C3+R
                              1060
                                      1060
                                           -999150
blk_dcd_info_tr(2)
                                      1060 -999153
                                                     -999133
                                                               544 N132
                              1060
blk_dcd_info_tr(3)
                    C3+R
                                                14
                                                      -4
                                                          132 N44
                                        746
iu srlz op encode(0)
                      C3+R
                                734
                                                      -17
                                                           132 N46
iu_srlz_op_encode(1)
                      C3+R
                                688
                                        652
                                               -11
                                                           141 N48
                                677
                                        679
                                               -19
                                                      -14
iu srlz_op_encode(2)
                      C3+R
                                                          98 N50
iu_srlz_op_encode(3)
                                        759
                                                7
                                                      1
                      C3+R
                                765
                                        806
                                                28
                                                      19
                                                          141 N52
iu_srlz_op_encode(4)
                      C3+R
                                812
                                646
                                        645
                                                       6
                                                          145 N54
                      C3+R
                                                15
iu srlz op encode(5)
                                                28
                                                       9
                                                          101 N56
                                789
                                        760
iu_srlz_op_encode(6)
                      C3+R
                                                           141 N58
                                789
                                        784
                                                31
                                                      16
                      C3+R
iu_srlz_op_encode(7)
                                                            98 N60
                                        786
                                                       12
                                 799
                                                19
iu srlz op encode(8)
                      C3+R
```

iu_srlz_op_encode	e(9) C3+F	73	6 6	81 50	22	153 N62
iu_srlz_op_encode	e(10) C3+	R 78	39 7	'83 18	3 11	98 N64
iu_srlz_op_encode	e(11) C3+	R 79	95 7	'85 12	2 11	98 N66
decode_ilc(0)	C3+R	476	504	38	29 35	6 N90
decode_ilc(1)	C3+R	458	489	52	39 40	4 N92
srlz_actn_tr(0)	C3+R	1060	1060	-999075	-99905	0 570 N30
srlz_actn_tr(1)	C3+R	1060	1060	-999075	-99905	0 542 N32
intrpt_info_tr(0)	C3+R	1060	1060	-999062	-99906	2 540 N104
intrpt_info_tr(1)	C3+R	1060	1060	-999066	-99905	3 568 N106
intrpt_info_tr(2)	C3+R	1060	1060	-999071	-99905	5 570 N108
intrpt_info_tr(3)	C3+R	1060	1060	-999071	-99905	5 568 N110
op_44_info_tr(0)	C3+R	626	481	98	71 5	52 N154
op_44_info_tr(1)	C3+R	624	548	96	93 5	39 N156
dcd_c_cnt(0)	C3+R	400	400	129	125 5	71 N148
dcd_c_cnt(1)	C3+R	400	400	140	126 6	01 N150

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Part: IDCDSUC

Analysis: Late and Early / Nominal EDA EinsTimer Design Information

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01 \*\*\* Don't Care, Data Adjust, Clock Adjust, Renamed Phase Tags \*\*\*

11010400 20101. 00.01	Don't Oarc,	Dala 7	nujusi, C	HOUR P	rujusi,	neik	ameu	rnase	ags	
Pin Name Signal/Net	DC AdjR	DC	AdjF Phs	s Ne	wPhs	DC	AdjR	DC Ad	F Phs	NewPhs
slow_mode.clockblock/c1				C3-	·	····	*	C3-	slow_n	node.c1_1
slow_mode.clockblock/c2			· _ *	C3+		_	_ *	C3+	slow_	mode.c2_1
slow_mode.clockblock_1/c1	and Martine Assessing 1997		_ **	C3-			_ *	C3-		in de la compania de Compania de la compania de la compa
slow_mode.c1_2										
slow_mode.clockblock_1/c2			*	C3+	-		*	C3+	400	
slow_mode.c2_2								_		
slow_mode.clockblock_2/c1		_	*	C3-		_	*	С3-		
slow_mode.c1_3										
slow_mode.clockblock_2/c2	* * * * * * * * * * * * * * * * * * *	_	*	C3+			*	C3+	,	
slow_mode.c2_3						_				.:
slow_mode.clockblock_3/c1			_ *	C3-			*	C3-	•	
slow_mode.c1_4						_	_			
slow_mode.clockblock_3/c2		_	*	C3+			*	C3+		
slow_mode.c2_4						_	_			
slow_mode.clockblock_4/c1		_	*	C3-			*	C3-		
slow_mode.c1_5			_			_				
slow_mode.clockblock_4/c2			*	C3+			*	C3+		
slow_mode.c2_5		_	_				_	•		
slow_mode.clockblock_5/c1			*	C3-			*	C3-	slow	mode.c1
slow_mode.clockblock_5/c2		_	*	C3+		_	- *	C3+	_	_mode.c2
		_				_		901	CIOW	_111000.02

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Part: IDCDSUC

Analysis: Late and Early / Nominal

**EDA EinsTimer Design Information** 

Compiled: Wed Mar 24 22:00:23 1999

Release Level: 03.01

\*\*\* User Selected Modes \*\*\*

```
Sun Apr 18 22:09:38 1999
Part: IDCDSUC
                                          EDA EinsTimer Design Information
Analysis: Late and Early / Nominal
Compiled: Wed Mar 24 22:00:23 1999
                                        *** User Defined Tests ***
Release Level: 03.01
                                                                                   BC
                                                                                          Norm
                                                                       Edge2
                                   Edge1 Pin2
Mode Pin1
WC
    *************** EinsTimer Parameters *
calculator.detail-calculator:
                                    CDC
                                   NOPATH
calculator.failure-calc:
                                   1E-09
calculator.tib-k1-term:
                                   1E-10
calculator.tib-k2-term:
                                   0
calculator.tib-k3-term:
                                       FALSE
cdc-flags.include-output-caps:
defaults.at-default:
                                  0
defaults.clock-gating-hold-time:
                                       0
defaults.clock-gating-mode:
                                       input-to-input
defaults.clock-gating-pulse-width-time:
defaults.clock-gating-setup-time:
defaults.rat-default:
                                  4E-09
defaults.rat-default-early:
                                    2E-06
defaults.rat-default-late:
                                   2E-06
                                    1.51E-07
defaults.slew-fall-default:
defaults.slew-rise-default:
                                     1.51E-07
                                       Nominal
delaymode.delay-mode:
                                        0
delaymode.lcd-best-early-value:
                                        0
delaymode.lcd-best-late-value:
delaymode.lcd-nominal-early-value:
                                          0 -
delaymode.lcd-nominal-late-value:
                                          0
                                        0
delaymode.lcd-pw-correction:
delaymode.lcd-worst-early-value:
                                         1
                                        1
delaymode.lcd-worst-late-value:
limits.global-cap-limit:
limits.global-slew-limit:
                                   4.55E-07
limits.use-global-cap-limit:
                                     FALSE
                                     TRUE
limits.use-global-slew-limit:
misc.bus-delimiter:
                                   ()
                                   10000
misc.cache-limit:
misc.debug-level:
misc.default-delimiter:
misc.default-divider:
misc.em_data_mult:
misc.frequency:
                                        610
misc.message-suppress:
                                       FALSE
misc.no-loop-message:
                                       TRUE
netcalc.cap-mode-external:
```

no-rcest

netcalc.net-delay-mode:

```
netcalc.pin-to-pin-net-model:
                                     FALSE
pd.incremental-pi-model:
                                    FALSE
process.best-case-temp:
                                     -10
process.best-case-vdd:
                                    1.7
process.best-case-vtt:
process.nominal-case-temp:
                                       10
process.nominal-case-vdd:
                                      1.45
                                     0
process.nominal-case-vtt:
process.use-default-temp:
                                     FALSE
process.use-default-vdd:
                                    FALSE
process.use-default-vtt:
                                   TRUE
process.worst-case-temp:
                                     10
process.worst-case-vdd:
                                     1.45
process.worst-case-vtt:
                                   0
report.decimal-places:
                                   0
rice.c-mult-bc:
rice.c-mult-nom:
rice.c-mult-wc:...
rice.r-mult-bc:
rice.r-mult-nom:
rice.r-mult-wc:
rice.rice-order:
timer.clock-limiting:
                                 TRUE
timer.domino-phase-creation:
                                      FALSE
timer.dta-adjust-mode:
                                   EdgeBased
timer.flush-propagate-on-dc-clock:
                                       TRUE
timer.perform-hold-tests:
                                    TRUE
timer.slew-dependency:
                                    path-slew
  > checkfan
```

## **Electrical Violations in Network 'IDCDSUC**

and the control of th	Capacitance Slew Sink
Fanout	
Pin/Port -> Net	Limit / AdjLim / Actual Limit / AdjLim / Actual
Limit / AdjLim / Actual	
eu_iu_enter_slow_md -> eu_iu_enter_slo	w_md 141.00 / 141.00 / 16.73 290.00
/ 290.00 / 352.00 * 12 / 12 / 1 1	
op_inq_stores -> op_inq_stores	141.00 / 141.00 / 159.72 * 290.00 /
290.00 / 112.00 12 / 12 / 3 1	
eu_iu_mmode -> eu_iu_mmode	141.00 / 141.00 / 32.56 290.00 /
290.00 / 326.00 * 12 / 12 / 2 1	
	eq
/ 290.00 / 424.00 * 12 / 12 / 2 1	
eu_iu_fpu_end_op -> eu_iu_fpu_end_o	p 141.00 / 141.00 / 30.80 290.00 /
290.00 / 339.00 * 12 / 12 / 1 1	
eu_iu_misc_hold -> eu_iu_misc_hold	141.00 / 141.00 / 19.15 290.00 /
290.00 / 332.00 * 12 / 12 / 1 1	
op_mcend_raw -> op_mcend_raw	141.00 / 141.00 / 144.35 * 290.00 /
290.00 / 91.00 12 / 12 / 3 1	
clkg -> clkg	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 12 / 12 / 3 1	,
du_iu_quiesced -> du_iu_quiesced	141.00 / 141.00 / 20.50 290.00 /
290.00 / 338.00 * 12 / 12 / 1 1	20000
iq_empty -> iq_empty	141.00 / 141.00 / 170.11 * 290.00 / 290.00

```
/116.00 12/ 12/ 4 1
                                                 141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                        -> gptr_scan_in
gptr_scan_in
       12/ 12/ 1 1
0.00
                                                141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                       -> gptr_a_clk
gptr_a_clk
0.00
       12/ 12/ 1 1
                                                141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                      -> gptr_b_clk
gptr_b_clk
0.00
       12/
             12/ 1 1
                                             141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                     -> clkg2
clkq2
      12/ 12/
                    3 1
60.00
                                                         141.00 / 141.00 / 15.67 290.00
eu_iu_fxu_exc_cond
                           -> eu_iu_fxu_exc_cond
                       12 / 1 1
/ 290.00 / 390.00 * 12 /
                                                 141.00 / 141.00 / 16.89 290.00 /
                          -> du_iu_store_status(2)
du iu store_status(2)
290.00 / 500.00 * 12 /
                       12 / 1 1
                                                       141.00 / 141.00 / 47.57 290.00 /
                          -> eu_iu_srlz_op_actn(0)
eu_iu_srlz_op_actn(0)
                        12/ 2 1
290.00 / 374.00 *
                                                        141.00 / 141.00 / 47.57 290.00 /
                           -> eu _iu_srlz_op_actn(1)
eu iu srlz op actn(1)
290.00 / 341.00 * 12 /
                       12/ 2 1
                                                     141.00 / 141.00 / 318.91 * 290.00 /
num dcd cyl(1)
                         -> num_dcd_cyl(1)
                12/ 12/ 1 1 1
290.00 / 80.00
                                                            141.00 / 141.00 / 16.89
                            -> eu_iu_srlz_op_encode(0)
eu_iu_srlz_op_encode(0)
290.00 / 290.00 / 401.00 *
                          12/ 12/ 1 1
                                                      141.00 / 141.00 / 16.89
                            -> eu_iu_srlz_op_encode(1)
eu_iu_srlz_op_encode(1)
                          12/ 12/ 1 1
290.00 / 290.00 / 400.00 *
                                                          141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(2)
                            -> eu_iu_srlz_op_encode(2)
290.00 / 290.00 / 420.00 * 12 / 12 / 1 1
                                                        141.00 / 141.00 / 16.89
                           -> eu_iu_srlz_op_encode(3)
eu_iu_srlz_op_encode(3)
290.00 / 290.00 / 302.00 *
                          12/ 12/ 1 1
                                                         141.00 / 141.00 / 16.89
                           -> eu_iu_srlz_op_encode(4)
eu_iu_srlz_op_encode(4)
                          12/ 12/ 1 1
290.00 / 290.00 / 406.00 *
                                                           -141.00 / 141.00 / 16.89 ·-
                           -> eu_iu_srlz_op_encode(5)
eu iu srlz op encode(5)
290.00 / 290.00 / 373.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(6) -> eu_iu_srlz_op_encode(6)
                                                            141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 *
                           12/ 12/ 1 1
                                                            141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(7)
                            -> eu_iu_srlz_op_encode(7)
290.00 / 290.00 / 398.00 * 12 / 12 / 1 1
eu_iu_srlz_op_encode(8) -> eu_iu_srlz_op_encode(8)
                                                            141.00 / 141.00 / 16.89 -
290.00 / 290.00 / 367.00 * 12 / 12 / 1 1
                            -> eu_iu_srlz_op_encode(9)
                                                            141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(9)
                           12/ 12/ 1 1
290.00 / 290.00 / 323.00 *
                                                            141.00 / 141.00 / 16.89
                           -> eu_iu_srlz_op_encode(11)
eu iu_srlz_op_encode(11)
290.00 / 290.00 / 500.00 *
                          12/ 12/ 1 1
                                                                78.50 / 78.50 / 220.92 *
c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1
                         12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
                                                                78.50 / 78.50 / 222.27 *
c2@slow mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                                                78.50 / 78.50 / 212.39 *
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                                                 78.50 / 78.50 / 237.92 *
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
                                                                 78.50 / 78.50 / 239.36 *
```

```
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2
                                                             78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1 3
                                                             78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3
                                                             78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3
                                                             78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4
                                                             78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                          Capacitance
                                                            Slew
                                                                          Sink
Fanout
                     -> Net
                                           Limit / AdjLim / Actual Limit / AdjLim / Actual
Pin/Port
Limit / AdjLim / Actual
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                            78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 - 12/--12 / - 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4
                                                             78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
                                                             78.50 / 78.50 / 237.91 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5
                                                            78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5
                                                             78.50 / 78.50 / 228.73 *
c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1
                                                            78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2
                                                            78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                                                            78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
y@C167:cs_invvv01c
                         -> dcd_succ_last_t1&0
                                                      70.00 / 70.00 / 1011.00 * 301.00
/ 301.00 / 3294.02 * 12 / 12 / 1 1 KEEP_BTR
y@C1994:cs invvn01c
                           -> N1531
                                                   68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02
                12/ 12/ 2 2
y@C2013:cs_invvn01c
                           -> N18&0
                                                   68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3608.92 * 12 / 12 / 1 1
y@C2082:cs_invvn01c
                           -> N146&0
                                                   68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 * 12 / 12 / 1 1
y@C2194:cs_invvn07c
                           -> N1681
                                                   261.00 / 261.00 / 271.46 * 290.00 /
```

```
290.00 / 261.53
                12/ 12/ 7 7
                                                          71.00 / 71.00 / 1044.40 *
y@C2393:cs_nnd2v02c
                             -> iu_reset_op_c_t1&0
290.00 / 290.00 / 3371.12 *
                          12/ 12/ 3 3
                                                     68.00 / 68.00 / 125.56 * 290.00 /
                            -> N1815
y@C2425:cs_invvn01c
290.00 / 451.90 * 12 /
                      12/ 1 1
                                                      85.00 / 85.00 / 97.67 * 290.00 /
y@C2496:cs_nnd4n03c
                             -> N1435
290.00 / 353.82 *
                12/
                       12/ 5 5
                            -> N1645
                                                     133.00 / 133.00 / 150.69 * 290.00 /
y@C2646:cs_invvn04c
                 12/
                       12/ 6 6
290.00 / 275.60
                                                         500.00 / 500.00 / 540.60 *
y@C2726:cs_nnd2n11c
                             -> dsucc_or_agi&0
                          12/ 12/ 2 2
290.00 / 290.00 / 258.01
                                                      996.00 / 996.00 / 1081.45 * 290.00
y@C2744:cs invvn13c
                            -> N2086&0
/ 290.00 / 271.62
                  12 / 12 / 7 7
                            -> N1290
y@C2800:cs_invvn08c
                                                     326.00 / 326.00 / 234.15 290.00 /
                      12 / 14 * 14
                 12/
290.00 / 193.42
                                                      167.00 / 167.00 / 183.47 * 290.00 /
                             -> N1097
y@C2728rwr:cs_invvn05c
290.00 / 266.58
                 12/
                       12/ 4 4
                                                      110.00 / 110.00 / 132.34 * 290.00 /
                             -> N2016
v@C2918:cs_nor2n04c
                       12/- 1 1
290.00 / 428.15 * 12 /
                                                      797.00 / 797.00 / 402.55 290.00 /
y@gbfocell_0:cs_invvn12c
                             -> gbfonet_0
                 12/ 12/ 20*20
290.00 / 149.98
I2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
                                                           247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45
                       12/ 12/ 8 8
[BD-500900]: (W) There were 64 electrical violations.
  > write_info_report
[ET-0018]: >Begin...Info Report
      for file /tmp/info_report..92476.
[ET-0019]: <End.....Info Report.
Sun Apr 18 22:09:40 1999
Part: IDCDSUC
Mode: Late and Early Mode / Nominal EDA EinsTimer Info Report
Release Level: 03.01 and Compile Date: Wed Mar 24 22:00:23 1999
```

*********** CA	APACITANCE VIOLATIONS ************************************	• • •
<b>.</b>	Over (+%)/ Sign	al/
Pin	Cell Power Cap Limit Under(-%) Source	Net
C2744/y	cs_invvn 13c 1081 996 9 N2086&0	
C2393/y	cs_nnd2v 02c 1044 71 1371 iu_reset_	op_c_t1&0
gptr_b_clk	1011 141 617 gptr_b_clk	
gptr_a_clk	1011 141 617 gptr_a_clk	
gptr_scan_in	1011 141 617 gptr_scan_in	- •
BOX750/OUT	IOPAD 1011 68 1387 N146	
BOX745/OUT	IOPAD 1011 68 1387 N18	
BOX716/OUT	IOPAD 1011 25 4025 iu_reset	
BOX714/OUT	IOPAD 1011 70 1344 dcd_suc	
BOX661/OUT	IOPAD 1011 141 617 gptr_b_	
BOX660/OUT	IOPAD 1011 141 617 gptr_a_	
BOX639/OUT	IOPAD 1011 141 617 gptr_sca	an_in&0
C2082/y	cs_invvn 01c 1011 68 1387 N146&0	
C2013/y	cs_invvn 01c 1011 68 1387 N18&0	
C167/y	cs_invvv 01c 1011 70 1344 dcd_succ_	
BOX746/OUT	IOPAD 1010 0 0 gptr_scan	_out&1

```
gptr_latch/gptr_scan_out
                                 XMODEBLOCK A
                                                     1010
                                                             0
                                                                    0 gptr_scan_out&0
 BOX717/OUT
                               IOPAD
                                              974
                                                   848
                                                            15 N2086
 C2726/v
                            cs_nnd2n 11c
                                             541
                                                  500
                                                            8 dsucc_or_agi&0
 BOX724/OUT
                               IOPAD
                                              451
                                                    396
                                                            14 dsucc_or agi
 num_dcd cyl(1)
                                          319 141
                                                        126 num_dcd_cyl(1)
                               IOPAD
 BOX679/OUT
                                              319
                                                    141
                                                           126 num_dcd_cyl&0(1)
frc_blk_1cyc.reg_n.lat_0/l2_out_n
                                    cl nnd2n
                                              07c
                                                     302
                                                          247
                                                                  22 frc_blk_1cyc q
 C2194/v
                                            271
                            cs_invvn 07c
                                                 261
                                                          4 N1681
slow_mode.clockblock_4/c2
                                   cb clk 32 1
                                                    239
                                                          78
                                                                205 slow_mode.c2_5
slow_mode.clockblock 2/c2
                                   cb_clk_32_1
                                                    239
                                                          78
                                                                205 slow_mode.c2 3
slow mode.clockblock_5/c2
                                   cb_clk_32_1
                                                    239
                                                          78
                                                                205 slow mode.c2
slow_mode.clockblock_1/c2
                                   cb clk 32 1
                                                    239
                                                          78
                                                                205 slow_mode.c2 2
slow_mode.clockblock 3/c2
                                   cb_clk_32_1
                                                    239
                                                          78
                                                                205 slow_mode.c2 4
slow_mode.clockblock_3/c1
                                   cb_clk_32_1
                                                    238
                                                                203 slow_mode.c1_4
                                                          78
slow_mode.clockblock_5/c1
                                   cb_clk_32_1
                                                    238
                                                          78
                                                                203 slow_mode.c1
slow_mode.clockblock_1/c1
                                   cb_clk_32_1
                                                    238
                                                          78
                                                                203 slow mode.c1 2
slow_mode.clockblock 2/c1
                                   cb clk 32 1
                                                    238
                                                          78
                                                                203 slow_mode.c1_3
slow_mode.clockblock_4/c1
                                   cb_clk 32 1
                                                    238.
                                                          .78
                                                                203 slow_mode.c1 5
slow_mode.clockblock_4/clka
                                   cb_clk_32 1
                                                    229
                                                                 191 slow_mode.clka_5
                                                          78
slow_mode.clockblock_3/clka
                                   cb_clk 32 1
                                                    229
                                                          78
                                                                 191 slow_mode.clka_4
slow_mode.clockblock_1/clka
                                   cb_clk_32_1
                                                    229
                                                          78
                                                                 191 slow_mode.clka 2
slow_mode.clockblock_5/clka
                                   cb_clk_32_1
                                                    229
                                                          78
                                                                 191 slow_mode.clka
slow_mode.clockblock_2/clka
                                   cb_clk_32_1
                                                    229
                                                          78
                                                                 191 slow_mode.clka_3
slow_mode.clockblock/c2
                                  cb_clk_32 1
                                                  222 ....78
                                                               183 slow_mode.c2_1
slow mode.clockblock/c1
                                  cb_clk_32_1
                                                  221 . 78
                                                               181 slow mode.c1 1
slow_mode.clockblock/clka
                                 __cb_clk_32_1
                                                   212
                                                         78 171 slow_mode.clka_1
C2728rwr/y
                            cs_invvn 05c
                                            - 183
                                                  167
                                                           10 N1097
iq_empty
                                       170. 141
                                                     21 iq_empty
BOX637/OUT
                               IOPAD
                                                           21 iq_empty&0
                                              170
                                                   141
op_inq_stores
                                              141
                                                       13 op_inq_stores
BOX604/OUT
                              IOPAD
                                              160
                                                   141
                                                           13 op_ing_stores&0
C2646/y
                           cs_invvn 04c
                                            151
                                                133
                                                          13 N1645
clkg2
                                          141
                                                   3 clkg2
                                     146
clkg
                                     146
                                          141
                                                   3 clkg
BOX664/OUT
                              IOPAD
                                              146
                                                   141
                                                            3 clkg2&0
BOX628/OUT
                              IOPAD
                                              146
                                                   141
                                                            3 clkg&0
op_mcend raw
                                              141
                                                        2 op_mcend_raw
BOX624/OUT
                              IOPAD
                                              144 141
                                                            2 op_mcend raw&0
du_iu_hold_aa_req
                                                         1 du_iu_hold_aa_req
                                           142 141
BOX617/OUT
                              IOPAD
                                              142 141
                                                            1 du_iu_hold_aa_req&0
C2918/y
                           cs_nor2n 04c
                                            132 110
                                                          20 N2016
gptr_latch/clkl_mode8
                               XMODEBLOCK A
                                                    128
                                                           0
                                                                 0 clkl_mode8
C2425/y
                           cs invvn 01c 126 68 85.N1815
gptr_latch/clkl_mode5
                               XMODEBLOCK A
                                                    103
                                                           0
                                                                 0 clkl mode5 0
gptr_latch/clkl_mode4
                               XMODEBLOCK A
                                                     99
                                                          0
                                                                 0 clkl_mode4_0
C2496/y
                           cs nnd4n 03c
                                             98
                                                  85
                                                         15 N1435
gptr_latch/clkl mode6
                               XMODEBLOCK A
                                                     96
                                                          0
                                                                 0 clkl_mode6_0
C1994/v
                           cs invvn
                                    01c
                                            77
                                                 68
                                                        14 N1531
iu_dsbl_ovrlp.reg_n.lat_0/l2_out_n
                                   cl nor2n
                                            06c
                                                    16
                                                         16
                                                                -2 iu_dsbl_ovrlp_q
dsbl_ovrlp_blk.reg_n.lat_0/l2 out n
                                   cl_nnd2n 07c
                                                     16
                                                                 -2 dsbi_ovrlp_blk_q
                                                          16
bht_block.reg_n.lat_0/l2_out_n
                                  cl_invvn 07d
                                                   16
                                                       16
                                                               -2 bht_block_q
slow_mode_t1.reg_n.lat_0/l2_out_n
                                     cl invvn
                                              07c
                                                                 -2 slow_mode_t1_q
                                                     16
                                                          16
eu_iu_spare.reg_n.lat_0/l2_out_n
                                   cl_invvn 07d
                                                    15
                                                         16
                                                                -6 eu_iu_spare_q
```

Sig Pin Net		Early Cell Powe		Over (+%)/ - D		Power Source
iu_ BO BO idc idc BO	slow_mode_t1 slow_mode_t1 X745/IN X745/IN dsuc_err dsuc_err VX750/IN	IOPAD IOPAD IOPAD IOPAD			1099 IOPAD 1099 IOPAD 693 cs_invvn 693 cs_invvn 098 IOPAD 098 IOPAD 692 cs_invvn 692 cs_invvn	01c N18&0 N146 N146 01c N146&0
iu_ iu_ BC iu_	reset_op_c_t1 reset_op_c_t1 X716/IN reset_op_c_t1&0	IOPAD	E R	3371 301 3371 455	1020 IOPAD 641 cs_nnd2v	
iu_ C2 iu_	555/b reset_op_c_t1&0 466/b reset_op_c_t1&0	cs_ao12n cs_nnd2n	03c E F	3371 290	1062 cs_nnd	
iu <u>.</u> BC iu_	reset_op_c_t1 reset_op_c_t1 0X716/IN reset_op_c_t1&0	IOPAD	L R	÷. *	629 cs_nnd2\	
iu_ C2 iu_	555/b reset_op_c_t1&0 466/b reset_op_c_t1&0	cs_ao12n cs_nnd2n	02c L F			
dc dc dc	d_succ_last_t1 d_succ_last_t1 d_succ_last_t1 d_succ_last_t1 d_succ_last_t1 DX714/IN	IOPAD	E R L R	3294 301 3294 455	994 IOPAD 624 cs_invvv	01c
dc B0 dc	d_succ_last_t1&0 )X714/IN d_succ_last_t1&0 _reset_op_c_t1	IOPAD	E R L F	3294 455 2484 301	624 cs_invvv	01c
iu BC iu_	reset_op_c_t1 DX716/IN reset_op_c_t1&0 2555/b	IOPAD cs_ao12n	L F	-	446 cs_nnd2	
iu C2 iu	_reset_op_c_t1&0 2466/b _reset_op_c_t1&0 _reset_op_c_t1	cs_nnd2n	02c L F	2484 290 2177 301	757 cs_nnd2	<u>≥</u> v 02c
iu B( iu	_reset_op_c_t1 DX716/IN _reset_op_c_t1&0 2555/b	IOPAD cs_ao12n	E F	2177 455 F 2177 290	378 cs_nnd2	
iu	_reset_op_c_t1&0 2466/b	cs_nnd2n		F 2177 290		2v 02c

	iu_reset_op_c_t1&0 iu_slow_mode_t1		L	F		301	555 IOPAD	N18
	iu_slow_mode_t1	IODAD	E.	F_		301	555 IOPAD	N18
	BOX745/IN	IOPAD	F	F	1973			
	BOX745/IN	IOPAD	. E	F	1973			
	idcdsuc_err		L F		61 301		552 IOPAD	N146
	idcdsuc_err		E F		61 30		552 IOPAD	N146
	BOX750/IN	IOPAD	<u>L</u>	F	1961	455	331 cs_invvn	
	BOX750/IN	IOPAD	E	F	1961	455	_	01c N146&0
	dcd_succ_last_t1		L	F	1874	301	523 IOPAD	
	dcd_succ_last_t1			_				
	BOX714/IN	IOPAD	L	۶F	1874	455	312 cs_invvv	01c
	dcd_succ_last_t1&0		_	_				
	BOX714/IN	IOPAD	Ε	F	1829	455	302 cs_invvv	01c
	dcd_succ_last_t1&0			_				
	dcd_succ_last_t1		Ε	F	1829	301	508 IOPAD	
	dcd_succ_last_t1		_	_				
	BOX699/IN	- IOPAD	· L	F	500	290 -	· -··-72	The same of the sa
	eu_iu_srlz_op_encode(11)							
	BOX699/IN	IOPAD	L	R	500	290	72	
	eu_iu_srlz_op_encode(11)	_						
· -	BOX699/IN	IOPAD	Ε	F	500	290	72	
	eu_iu_srlz_op_encode(11)						· i	
Charles Straight of	BOX699/IN	- IOPAD	Ε.	- R-	500	290	72	odia Tribulization or area estra
*.	eu_iu_srlz_op_encode(11)			ای د دور		-		
	BOX671/IN	IOPAD		F	500	290	72	
	du_iu_store_status(2)	**		1.4	* .			
1 42 5 6 1221	BOX671/IN	IOPAD	<u>L</u>	R	500	290	72	
	du_iu_store_status(2)	-				a a a a a a a a a a a a a a a a a a a	eri en lii, erie e Elisa en lii, erie en	in the Carlotte of the Carlott
	BOX671/IN			F	500	290	72	
	du_iu_store_status(2)		· · · · · · · · · · · · · · · · · · ·	· ::_ ·				
11 A 11 A	BOX671/IN	IOPAD	E	R	500	290	72	
	du_iu_store_status(2)	7					· · · · · · · · · · · · · · · · · · ·	
	C2763/a	cs_nnd2n	02c L	F	. 500	290	72 IOPAD	
	du_iu_store_status&0(2)			_			·	A Section of the Control of the Cont
	C2763/a	cs_nnd2n	02c L	R	500	290	72 IOPAD	
	du_iu_store_status&0(2)			_				
	C2763/a	cs_nnd2n	02c E	F	500	290	72 IOPAD	•
	du_iu_store_status&0(2)	10	00. 5	_				
	C2763/a	cs_nnd2n	02c E	R	500	290	72 IOPAD	
	du_iu_store_status&0(2)		00.	_		000	== 10= 1=	
	C2650/a	cs_nnd2n	02C L	F	500	290	72 IOPAD	
	eu_iu_srlz_op_encode&0(11)			_				the contract of the contract o
	C2650/a	cs_nnd2n	02c L	R	500	290	72 IOPAD	
	eu_iu_srlz_op_encode&0(11)	•		_				
	C2650/a	cs_nnd2n	02c E	F	500	290	72 IOPAD	
	eu_iu_srlz_op_encode&0(11)		aa =					
	C2650/a	cs_nnd2n	02c E	R	500	290	72 IOPAD	
	eu_iu_srlz_op_encode&0(11)			_				
	C2487/b		14e L	R	452		_	
	C2487/b	cs_nnd2x	14e E	R			_	
	C2917/b	cs_nnd2x	14c L	R	428		48 cs_nor2n	04c N2016
	BOX617/IN	IOPAD	L	F	424	290	46	
	du_iu_hold_aa_req			_				
	BOX617/IN	IOPAD	L	R	424	290	46	

	du_iu_hold_aa_req bce_hold_aa.reg_n.lat_0/a	cl_iı	nvvn 07	d L	F	424	290 46 IOPA	AD
	du_iu_hold_aa_req&0	اناه	overe 07	A 1	D	424	290 46 IOPA	AD.
	bce_hold_aa.reg_n.lat_0/a du_iu_hold_aa_req&0	CI_II	nvvn 07	u L	R	464	200 40 IOF	
•	C2020/a	cs_invvv	14c L	F	424	290	46 IOPAD	
	du_iu_hold_aa_req&0 C2020/a	cs_invvv	14c L	R	424	290	46 IOPAD	
	du_iu_hold_aa_req&0		140 5	В	400	200	46 oc norûn	04c N2016
	C2917/b BOX690/IN	cs_nnd2x IOPAD	14C E	R F	423 420	290 290	46 cs_nor2n 45	04C 1\2010
	eu_iu_srlz_op_encode(2) BOX690/IN	IOPAD	L	R	420	290	45	
	eu_iu_srlz_op_encode(2) C2665/a	cs_nnd2n	02c L	F	420	290	45 IOPAD	
	eu_iu_srlz_op_encode&0(2) C2665/a	cs_nnd2n	02c L	R	420	290	45 IOPAD	
	eu_iu_srlz_op_encode&0(2)	00	<b>5</b> _5 _					
	BOX692/IN	IOPAD	- L	R	406	290	40	
	eu_iu_srlz_op_encode(4) C2657/a	cs_nnd2n	02c L	R	406	290	40 IOPAD	
	eu_iu_srlz_op_encode&0(4) BOX692/IN	IOPAD	· · · L	F	405	290	40	
	eu_iu_srlz_op_encode(4) C2657/a	cs_nnd2n	02c L	F	405	290	40 IOPAD	
	eu_iu_srlz_op_encode&0(4) = BOX688/IN	IOPAD	L	F	401	290	38	
	eu_iu_srlz_op_encode(0) BOX688/IN	IOPAD	Ľ	R	401	290	38	
	eu_iu_srlz_op_encode(0) C2667/a	cs_nnd2n	02c L	F.	401	290	38 IOPAD	na ang sampagisah gilaman an Pilipah na bijih berilan
and the second second	eu_iu_srlz_op_encode&0(0) C2667/a	cs_nnd2n	02c L	 B	401	290	38 IOPAD	
•	eu_iu_srlz_op_encode&0(0)						• • • •	***
	BOX689/IN eu_iu_srlz_op_encode(1)	IOPAD	L	R	400	290	·. 38	
	C2666/a	cs_nnd2n	02c L	R	400	290	38 IOPAD	
	eu_iu_srlz_op_encode&0(1) BOX689/IN	IOPAD	L	F	399	290	38	
	eu_iu_srlz_op_encode(1) C2666/a	cs_nnd2n	02c L	F	399	290	38 IOPAD	
	eu_iu_srlz_op_encode&0(1) BOX695/IN	IOPAD	L	R	398	290	37	t kan garak k
	eu_iu_srlz_op_encode(7) C2659/a	cs_nnd2n	02c L	R	398	290	37 IOPAD	
	eu_iu_srlz_op_encode&0(7) BOX695/IN	IOPAD	L	F	395	290	36	
	eu_iu_srlz_op_encode(7) C2659/a	cs_nnd2n	02c L	F	395	290	36 IOPAD	
	eu_iu_srlz_op_encode&0(7) BOX665/IN	IOPAD	L	F	390	290	34	
	eu_iu_fxu_exc_cond BOX665/IN	IOPAD	L	R	390	290	34	
	eu_iu_fxu_exc_cond C1928/a	cs_invvn	01c L	F	390	290	34 IOPAD	

	eu_iu_fxu_exc_cond&0	i	04 a 1	_	200	220	O LIODAD			
	C1928/a	cs_invvn	UIC L	R	390	290	34 IOPAD			
	eu_iu_fxu_exc_cond&0 BOX672/IN	IOPAD	L	F	374	290	29			
	eu_iu_srlz_op_actn(0)		•							
	srlz_actn.reg_n.lat_0/a	cl_inv	n 07d	L	F 3	74 29	90 29 IOPAD			
	eu_iu_srlz_op_actn&0(0) C2651/a	cs_nnd2n	02c L	F	374	290	29 IOPAD			
	eu_iu_srlz_op_actn&0(0)	IODAD	•	_	070	000	00			
	BOX693/IN eu_iu_srlz_op_encode(5)	IOPAD	L	F	373	290	29			
	BOX693/IN	IOPAD	L	R	373	290	29			
	eu_iu_srlz_op_encode(5) C2656/a	cs_nnd2n	02c L	F	373	290	29 IOPAD			
	eu_iu_srlz_op_encode&0(5) C2656/a	cs_nnd2n	02c l	R	272	290	29 IOPAD			
	eu_iu_srlz_op_encode&0(5)		020 L	п						
	BOX696/IN eu_iu_srlz_op_encode(8)	IOPAD	-L	F	367	290-	27	and another and a second .	1871	
	BOX696/IN	IOPAD	L	R	367	290	27			
<i>:</i>	eu_iu_srlz_op_encode(8) C2660/a	cs_nnd2n	02c   I	F	367	290	27 IOPAD			
	eu_iu_srlz_op_encode&0(8)	3 <b></b>				_00	2, 131 /12			
	C2660/a	-cs_nnd2n	-02c L	R	367	290	27 IOPAD		The state of the s	
Silver March (1965) Silver March (1965) Silver March (1965) Silver March (1965) Silver March (1965)	eu_iu_srlz_op_encode&0(8) BOX672/IN	The second secon				e Sara		TO THE STATE OF TH	To the second se	
the second second	eu_iu_srlz_op_actn(0)	101715	i seit		_000-	230				
And the second of the second o	srlz_actn.reg_n.lat_0/a	cl inv	/n 07d	L	R - 3	66 29	90 26 IOPAD	ا ما محمد می داد. محمد با میگرش با اداران وجد ساد رفیسترسطیکم	en de la como esta en la como en la como esta	and the state of t
	eu_iu_srlz_op_actn&0(0)		· · · · · · · · · · · · · · · · · · ·	. –						
	C2651/a	cs_nnd2n	02c L	Ŕ	366	290	26 IOPAD	o provincia de la compania de la co La compania de la co	er om her til grade blad had had. Statemen som had had blad had blad had blad had blad blad had blad blad had blad blad blad had blad blad blad Till till till till till till till till	4
	eu_iu_srlz_op_actn&0(0)								and the second of the second o	
	BOX694/IN	IOPAD	L	R	354	290	22			- *
	eu_iu_srlz_op_encode(6) C2658/a	oo nadoa		D	254	000		***	ST T III	*
	eu_iu_srlz_op_encode&0(6)	cs_nnd2n	02C L	R	354	290	22 IOPAD			
	iu_dsbl_ovrlp.reg_n.lat_0/b	cl no	or2n 06	د ا	*R	354	290 22_cs_nr	nd4n 03c		
	N1435	GI_110	OO	J L		<b>557</b>	-UU	IG <del>-1</del> 11 000	**	
	C2622/b	cs_nor2n	02c L	R	354	290	22 cs_nnd4n	03c N1435		
	C2544/a	cs_invvn	01c L	R	354		22 cs_nnd4n			
	C2543/b	cs_nnd2n		R	354	290	22 cs_nnd4n	03c N1435		
	C2513/b	cs_nnd2n	02c L	R		290		03c N1435		
	BOX602/IN	IOPAD	L	R	352	290	21			
	eu_iu_enter_slow_md			-				4 - 4 N. 4		
	C2107/b	cs_nnd2n	02c L	R	352	290	21 IOPAD			
	eu_iu_enter_slow_md&0 BOX602/IN	IODAD		_	246	200	10			
	eu_iu_enter_slow_md	IOPAD	L	F	346	290	19			
	C2107/b	cs_nnd2n	02c L	F	346	290	19 IOPAD			
	eu_iu_enter_slow_md&0 BOX673/IN	IOPAD	L	F	341	290	18			
	eu_iu_srlz_op_actn(1)		_							
	BOX673/IN	IOPAD	L	R	341	290	18			
	eu_iu_srlz_op_actn(1) srlz_actn.reg_n.lat_1/a	cl inva	n 07d		F 34	41 29	90 18 IOPAD			
	eu_iu_srlz_op_actn&0(1)	CI_HTVV	ii U/U	_	1" 3"	+1 ZS	70 10 IOPAD			

				_				
	srlz_actn.reg_n.lat_1/a	cl_inv	/n 07d	L F	₹ 34	41 29	0 18 IOPAE	)
	eu_iu_srlz_op_actn&0(1)			_				
		cs_nnd2n	02c L	F	341	290	18 IOPAD	
	eu_iu_srlz_op_actn&0(1)			_	244		10.10040	
		cs_nnd2n	02c L	R	341	290	18 IOPAD	
	eu_iu_srlz_op_actn&0(1)			_	_		4 <b></b>	00-
	iu_dsbl_ovrlp.reg_n.lat_0/b	cl_no	or2n 06	ic E	R	340	290 17 cs_i	nnd4n 03c
	N1435			_			14	
	C2622/b	cs_nor2n	02c E	R		290		03c N1435
	C2544/a	cs_invvn				290		03c N1435
	C2543/b	cs_nnd2n				290		n 03c N1435
	C2513/b	cs_nnd2n				290	_	n 03c N1435
	BOX618/IN	IOPAD	L	R	339	290	17	
	eu_iu_fpu_end_op							
	C2017/a	cs_invvn	07c L	R	339	290	17 IOPAD	
	eu_iu_fpu_end_op&0			_				
	BOX631/IN	IOPAD	L	F	338	290	17	du_iu_quiesced
	BOX631/IN	IOPAD	L	R	338		17	du_iu_quiesced
	BOX618/IN	IOPAD	L	F	338	290	17 .	•
	eu_iu_fpu_end_op				····			
	C2017/a	cs_invvn	07c L	F	338	290	17 IOPAD	•
	eu_iu_fpu_end_op&0	**						
	C1987/a	cs_nnd2n	04c L	F.	338	290	17 IOPAD	
	du_iu_quiesced&0			andromer — e m Tallo Sala Sala Sala	,			· · · · · · · · · · · · · · · · · · ·
	C1987/a						17 IOPAD	
1900	du_iu_quiesced&0							
A STATE OF THE STA	BOX694/IN	IOPAD	L	F	336	_290	16	
	eu_iu_srlz_op_encode(6)							
	C2658/a	cs_nnd2n	02c L	<u> </u>	336	290	16 IOPAD	
	eu_iu_srlz_op_encode&0(6)				د چار <del>ت</del> ه د پر د	- 1,000		
		IOPAD		R	332	290	14	المنصفي المناف المعين والمرادي
-	eu_iu_misc_hold		20.71			220	4410040	we have the second of the second
•	C2310/a	cs_nor3n	03c L	H	332	290	14 IOPAD	
	eu_iu_misc_hold&0	:2545		_	220	222	40	:
	BOX608/IN	IOPAD	L	F	326		12	eu_iu_mmode
ı	BOX608/IN	IOPAD	L	R	326	290	12	eu_iu_mmode
**	C2466/a	cs_nnd2n	02c <u>L</u>	. F	326	290	12 IOPAD	
	eu_iu_mmode&0	10		_	200	200	40 100 40	
ı	C2466/a	cs_nnd2n	02c L	. н	320	290	12 IOPAD	
	eu_iu_mmode&0		24 . 1	_	222	220	40 IODAD	
	C2016/a	cs_invvn	01c L	F	326	290	12 IOPAD	
	eu_iu_mmode&0			_	200	200	40 IODAD :	
	C2016/a	cs_invvn	01c L	R	326	290	12 IOPAD	
	eu_iu_mmode&0			_				
	BOX697/IN	IOPAD	L	R	323	290	11	
	eu_iu_srlz_op_encode(9)			_	200	200	44 10040	
	C2661/a	cs_nnd2n	02c L	. R	323	290	11 IOPAD	
	eu_iu_srlz_op_encode&0(9)			_			. =	
	BOX697/IN	IOPAD	L	F	319	290	10	
	eu_iu_srlz_op_encode(9)							
	C2661/a	cs_nnd2n	02c l	_ F.	319	290	10 IOPAD	
	eu_iu_srlz_op_encode&0(9)							
	BOX619/IN	IOPAD	L	F		290	7	eu_iu_misc_hold
	C2310/a	cs_nor3n	03c L	. F	310	290	7 IOPAD	
	eu_iu_misc_hold&0							

1	BOX691/IN	IOPAD	L	R	302	290	4
i	eu_iu_srlz_op_encode(3)						
	C2664/a	cs_nnd2n	02c L	R	302	290	4 IOPAD
	eu_iu_srlz_op_encode&0(3)						
	BOX691/IN	IOPAD	L	F	295	290	2
	eu_iu_srlz_op_encode(3)						·
	C2664/a	cs_nnd2n	02c L	F	295	290	2 IOPAD
	eu_iu_srlz_op_encode&0(3)						
	BOX661/IN	IOPAD	L	F	151	0	0 gptr_b_clk
	BOX661/IN	IOPAD	L	R	151	0	0 gptr_b_clk
	BOX661/IN	IOPAD	Ε	F	151	0	0 gptr_b_clk
	BOX661/IN	IOPAD	Ε	R	151	0	0 gptr_b_clk
	BOX660/IN	IOPAD	L	F	151	0	0 gptr_a_clk
	BOX660/IN	IOPAD	L	R	151	0	0 gptr_a_clk
	BOX660/IN	IOPAD	E	F	151	0	0 gptr_a_clk
	BOX660/IN	IOPAD	E	R	151	0	0 gptr_a_clk
	BOX639/IN	IOPAD	L	F	151	0	0 gptr_scan_in
i	BOX639/IN	IOPAD	L	R	151	0	0 gptr_scan_in
i	BOX639/IN	IOPAD	E	F	151	0	0 gptr_scan_in
	BOX639/IN	IOPAD	E	R	151	0	0 gptr_scan_in
	gptr_latch/gptr_scan_in	XMOE	DEBLOCK	( A )		151	0 0 IOPAD
	gptr_scan_in&0						
	gptr_latch/gptr_scan_in	XMOL	DEBLOCK	( A	L R	151	0 0 IOPAD
	-gptr_scan_in&0	and the second second					
	gptr_latch/gptr_scan_in	XMOL	DEBLOCK	( A	E F	151	0 0 IOPAD
	gptr_scan_in&0			**	or reflectable	and softman	man and a second of the second
Control of the Contro	gptr_latch/gptr_scan_in	XMOE	DEBLOCK	( A	E R	151	0. 0 IOPAD:
**************************************	gptr_scan_in&0		The second of the second			The second secon	me salah dari dari dari dari dari dari dari dari
Latina Landa MAN	gptr_latch/gptr_b_clk	XMODE	EBLOCK	Α	L F	. 151	00 IOPAD
	gptr_b_clk&0						
roman r. Turkunan h. C	gptr_latch/gptr_b_clk	XMODE	EBLOCK	A	L R	151-	0 IOPAD
TO get the Mary leaves as an example of a	gptr_b_clk&0			177		TOTAL TO LEAD OF THE S	<u>and the second of the second </u>
14 15 14 14 14 14 14 14 14 14 14 14 14 14 14	gptr_latch/gptr_b_clk	XMODE	EBLOCK	Α	E F	151	0 0 IOPAD
	gptr_b_clk&0	4		*	*		
	gptr_latch/gptr_b_clk	XMODE	EBLOCK	A I	E R	151	0 0 IOPAD
	gptr_b_clk&0						
	gptr_latch/gptr_a_clk	XMODE	EBLOCK	A !	L F	151	0 0 IOPAD
-	gptr_a_clk&0						and the second of the second o
	gptr_latch/gptr_a_clk	XMODE	EBLOCK	A I	L R	151	0 0 IOPAD
i	gptr_a_clk&0						
	gptr_latch/gptr_a_clk	XMODE	EBLOCK	A f	E F	151	0 0 IOPAD
i	gptr_a_clk&0						
	gptr_latch/gptr_a_clk	XMODE	EBLOCK	A I	E R	151	0 0 IOPAD
	gptr_a_clk&0						
·	C2890rwr/a					30	-1 cs_nnd2v 13c N2005
	C2339/a	_		F		30	-1 cs_nnd2v 13c NET690
	dcd_succ_disable_scan.reg_n	ı.lat_1/a	cl_invvn	07d	J L F	F 30	) 30 -1 cs_invvn 07c
	N2060						
	dcd_succ_disable_scan.reg_n	ı.lat_1/a	cl_invvn	07d	JE F	F 30	0 30 -1 cs_invvn 07c
	N2060						
	C2909/b	cs_nnd2x		F	29	30	-2 cs_invvv 13c N2012
i	C2101/a	cs_nnd2n	04c L	F	29	30	-2 cs_invvn 07c N1643
	C2113/a	cs_nnd2n		F	29	30	-3 cs_invvn 07c N1644
i	C2113/a	cs_nnd2n		F	29	30	-3 cs_invvn 07c N1644
i	C2101/a	cs_nnd2n	04c E	F	29	30	-3 cs_invvn 07c N1643

	C2409/b	cs_nnd2n	∩4c F	F	29	30	-3 cs_invvn 07c N1707	
	C2212/b	cs_nnd2n		F	29	30	-3 cs_invvn 07c N139	
	blk_dcd.reg_n.lat_3/a1			Ĺ	F		30 -4 cs_invvv 13b N1119	
			21n 07c	Ē	F	29	30 -4 cs_invvv 13b N1119	
	blk_dcd.reg_n.lat_3/a1	cs_nor2n		F	29	30	-4 cs_invv 13b N1119	•
	C2509/b	cs_nor2n	02c E	F	29	30	-4 cs_invvv 13b N1119	
	C2509/b	cs_not2n	14c L	F	29	30	-4 cs_invvv 13b N1119	
	C2338/a	cs_nnd2x	140 E	F	29	30	-4 cs_invvv 13b N1119	
	C2338/a	cs_nnuzx	10e L	R	29	30	-4 cs_invvv 10c N2000	
	C2889/b	cs_oaz III	10e E	F	29	30	-5 cs_nnd2v 13c N2005	
	C2890rwr/a	cs_nivvv	10c E	R	28	30	-5 cs_invvv 10c N2000	
	C2889/b	cs_oaz111	02c L	F	28	30	-6 cs_invvn 07c N1693	
	C2284/b	cs_nnd2x	14e E	F	28	30	-6 cs_invvv 13c N2012	
	C2909/b	cs_nnd2v	13c E	F	28	30	-6 cs_invvv 14c N29	
	C2187/b		13c L	F.	27	30	-9 cs_nnd2x 14b N675	
	C2744/a	cs_invvn cs_invvn	13c E	F	27	30	-9 cs_nnd2x 14b N675	
	C2744/a	cs_nnd2n	02c L	F	27	30	-9 cs_nnd2x 14b N675	
	C2743/b C2743/b	cs_nnd2n	02C E	F	27	30	-9 cs_nnd2x 14b N675	
	C2743/b	cs_nnd2n		F	27	30	-9 cs_nnd2x 14b N675	
		.cs_nnd2n		F	27	30	-9 cs_nnd2x 14b N675	
•		cs_invvv		F		30	-9 cs_nnd2x 14b N675	
		cs_invvv		F	27	30	-9 cs_nnd2x 14b N675	
	C2269/b	cs_nnd3n		F	27	.30	-9 cs_invvn 07c N1688	
		cs_nnd3n			27	30	-9 cs_invvn 07c N1686	The summer was the second seco
	C2321/b	cs_nnd3n		. E		30	-9 cs_invvn 07c N1702	en den en e
	C2321/b			F.	27	30	-9 cs_invvn 07c N1702	and the same of th
	C2284/b	cs_nnd3n	02c E	F	27	30	-9 cs_invvn 07c N1693	
	C2269/b	cs_nnd3n		F	27	30		
	C2257/b	cs nnd3n	02c E	F	27	30		The same of the second
· • · • · • · · · · · · · · · · · · · ·	spare.reg_n.lat_0/a	cl_invv	n - 07d L	F	_ 27	7 30	011 cs_invvn 07c N2064	
	spare.reg_n.lat_0/a	cl_invv	<u>n 07</u> d E	: F	2	7 3		
	C2897/b	cs_ao12n	07c L	F	26	30	-12 cs_invvn 07c N2007	
	C2897/b	cs_ao12n	07c E	F.	26	30	-12 cs_invvn 07c N2007	
	dcd_succ_disable_scan.reg_n	.lat_2/a	cl_invvn	05d	I L	F	26 30 -13 cs_invvn 07c	•
	N2062				_	_	· · · · · · · · · · · · · · · · · · ·	
	dcd_succ_disable_scan.reg_n	.lat_2/a	cl_invvn	05d	ΙE	F	26 30 -13 cs_invvn 07c	
	N2062							-
	C2709rwr/a	cs_nor3v	10e L	F	26			
	C2709rwr/a		10e E			30		
	C2297/b	cs_nnd2n		F	25	30	-17 cs_invvn 07c N1683	
	C2297/b	cs_nnd2n		F	25	30		
	C2723rwr/a		n 05c L	F	24		<del></del>	
	C2723rwr/a	cs_nnd3		F			<del></del>	
	FANINV/a	cs_invvn		F	22 22	30 30	<del>_</del>	
	FANINV/a	cs_invvn		F	22	30	-28 cs_invvv 19b N1587	
	C2487/a	cs_nnd2x	14e L 14e E	F F	22	30	<del>_</del>	
	C2487/a	cs_nnd2x cs_ao22r		F	22 22		——————————————————————————————————————	
	C2406/b2 C2406/b2	cs_ao22r		F	22		<del>_</del>	
	C2406/02 C2217/a	cs_au22i		F	22	30	<del></del>	
	C2217/a C2217/a	cs_nnd2n		F	22	30	<del>-</del>	
	C2889/b	cs_nnu2n		F	19	30	-37 cs_invvv 10c N2000	
	C2889/b	cs_oa21n		F	19			
	02003/D	US_UAZ III	IUG L	•			33 33 100 112000	

<sup>\*\*\*\*\*\*\*\*\*\*</sup> Worst Slew per Phase \*\*\*\*\*\*\*\*\*\*\*

```
Early
Phase Worst Slew Pin
C3+
            60 slow_mode.clockblock/c2
C3-
           60 slow_mode.clockblock/clkg
C3+R
            3609 C2013/v
     Late
Phase Worst Slew Pin
C3+
            60 slow_mode.clockblock/c2
C3-
           60 slow_mode.clockblock/clkg
C3+R
            3609 C2013/y
****** SINKLESS -
                      Output pin not feeding into any other pins
Pin
                          Cell+Power
<<< No SINKLESS Pins >>>>
******** SOURCELESS -
                            Input pin not fed by any other pins
                          Cell+Power
<>< No SOURCELESS Pins >>>>
                  و المستروع المراجع المستويد و المستروع المستروع المستروع المستروع المستروع المستروع المستروع المستروع المستروع
       PATHLESS - Input pin without sink and Output pin without source
    Cell+Power
aptr latch/aptr a clk
                                 cb mode block
aptr latch/aptr b clk
                        cb mode block
gptr_latch/gptr_scan_in
                                  cb mode block
                                        cb_clk_32_1
slow_mode.clockblock/scan_enable
                                        cb clk 32 1
slow mode clockblock/clkl mode7
                                         cb_clk_32_1
slow_mode.clockblock_1/scan_enable
slow_mode.clockblock_1/clkl_mode7
                                         cb_clk_32_1
slow_mode.clockblock_2/scan_enable
                                         cb_clk_32_1
slow_mode.clockblock_2/clkl_mode7
                                         cb_clk_32_1
slow_mode.clockblock_3/scan_enable
                                         cb_clk_32_1
                                         cb_clk_32_1
slow_mode.clockblock_3/clkl_mode7
slow_mode.clockblock_4/scan_enable
                                         cb_clk_32_1
slow_mode.clockblock 4/clkl mode7
                                         cb_clk_32 1
slow mode.clockblock 5/scan enable
                                         cb clk 32 1
slow mode.clockblock 5/clkl mode7
                                         cb clk 32 1
slow_mode.reg_n.lat_0/clka
                                    cl_invvn07d
slow_mode.reg_n.lat_0/scan_in
                                      cl invvn07d
ru_rq_blk.reg_n.lat_0/clka
                                  cl invvn07d
ru_rq_blk.reg_n.lat_0/scan_in
                                    cl_invvn07d
iu rst fst.reg n.lat 0/clka
                                  cl invvn07c
iu_rst_fst.reg_n.lat_0/scan_in
                                   cl_invvn07c
iu_restart.reg_n.lat_0/clka
                                  cl nnd2n07c
iu_restart.reg_n.lat_0/scan_in
                                    cl_nnd2n07c
ia_to_if.reg_n.lat_0/clka
                                 cl_invvn07c
ia_to_if.reg_n.lat_0/scan in
                                   cl_invvn07c
frc_mmode.reg_n.lat_0/clka
                                    cl nnd2n07c
frc_mmode.reg_n.lat_0/scan_in
                                      cl_nnd2n07c
local milli.reg n.lat 0/clka
                                  cl invvn07c
```

local milli.reg\_n.lat\_0/scan\_in ia\_to\_if\_t1.reg\_n.lat\_0/clka ia\_to\_if\_t1.reg\_n.lat\_0/scan\_in mia\_to\_if.reg\_n.lat\_0/clka mia to if.reg\_n.lat\_0/scan\_in slow mode t1.reg\_n.lat\_0/clka slow mode\_t1.reg\_n.lat\_0/scan\_in ig empty\_dly.reg\_n.lat\_0/clka iq\_empty\_dly.reg\_n.lat\_0/scan\_in slow\_mode\_t2.reg\_n.lat\_0/clka slow\_mode\_t2.reg\_n.lat\_0/scan\_in s390\_updt\_blk.reg\_n.lat\_0/clka s390\_updt\_blk.reg\_n.lat\_0/scan\_in srlz\_nomatch.reg\_n.lat\_0/clka srlz\_nomatch.reg\_n.lat\_0/scan\_in bce\_hold\_aa.reg\_n.lat\_0/clka bce\_hold\_aa.reg\_n.lat\_0/scan\_in srlz actn.reg n.lat\_0/clka srlz\_actn.reg\_n.lat\_0/scan\_in srlz\_actn.reg\_n.lat\_1/clka srlz actn.reg\_n.lat\_1/scan\_in op\_44\_dcd.reg\_n.lat\_0/clka op\_44\_dcd.reg\_n.lat\_0/scan\_in op\_cmp\_tr.reg\_n.lat\_0/clka op\_cmp\_tr.reg\_n.lat\_0/scan\_in num\_dcd.reg\_n.lat\_0/clka num dcd.reg\_n.lat\_0/scan\_in num\_dcd.reg\_n.lat\_1/clka num\_dcd.reg\_n.lat\_1/scan\_in mia\_to\_if\_t1.reg\_n.lat\_0/clka mia\_to\_if\_t1.reg\_n.lat\_0/scan\_in eu op encode.reg\_n.lat\_0/clka eu op encode.reg n.lat\_0/scan\_in eu\_op\_encode.reg\_n.lat\_1/clka eu\_op\_encode.reg\_n.lat\_1/scan\_in eu\_op\_encode.reg\_n.lat\_2/clka eu op\_encode.reg\_n.lat\_2/scan\_in eu op encode.reg\_n.lat\_3/clka eu\_op\_encode.reg\_n.lat\_3/scan\_in eu\_op\_encode.reg\_n.lat\_4/clka eu\_op\_encode.reg\_n.lat\_4/scan\_in eu\_op\_encode.reg\_n.lat\_5/clka eu op\_encode.reg\_n.lat\_5/scan\_in eu op encode.reg\_n.lat\_6/clka eu\_op\_encode.reg\_n.lat\_6/scan\_in eu op\_encode.reg\_n.lat\_7/clka eu op encode.reg\_n.lat\_7/scan\_in eu op\_encode.reg\_n.lat\_8/clka eu\_op\_encode.reg\_n.lat\_8/scan\_in eu\_op\_encode.reg\_n.lat\_9/clka eu\_op\_encode.reg\_n.lat\_9/scan\_in eu op encode.reg\_n.lat\_10/clka eu op encode.reg n.lat 10/scan\_in eu op encode.reg\_n.lat\_11/clka eu\_op\_encode.reg\_n.lat\_11/scan\_in

cl\_invvn07c cl\_invvn07c cl\_invvn07c cl invvn07c cl invvn07c cl\_invvn07c cl\_invvn07c cl\_invvn05c cl invvn05c cl invvn07d cl invvn07d cl nnd2n07c cl nnd2n07c cl\_nnd2n07c cl\_nnd2n07c cl invvn07d cl\_invvn07d cl\_invvn07d cl inyvn07d cl invvn07d cl invvn07d cl ao22n07c cl\_ao22n07c cl nnd2n07c cl nnd2n07c cl\_ao22n07c cl\_ao22n07c cl ao22n07c cl ao22n07c cl\_invvn07c-... -cl\_invvn07c-cl\_invvn06d cl invvn06d cl invvn06d cl invvn06d cl invvn06d cl invvn06d cl invvn06d cl\_invvn06d cl invvn06d cl invvn06d cl\_invvn06d cl invvn06d cl\_invvn06d cl invvn06d cl invvn06d cl\_invvn06d cl invvn06d cl\_invvn06d cl\_invvn07d cl invvn07d cl\_invvn06d cl\_invvn06d cl invvn06d cl invvn06d

```
frc_blk_1cyc.reg_n.lat_0/clka
                                    cl nnd2n07c
frc_blk_1cyc.reg_n.lat_0/scan_in
                                     cl_nnd2n07c
local_milli_t1.reg_n.lat_0/clka
                                   cl_invvn07c
local_milli_t1.reg_n.lat_0/scan_in
                                     cl invvn07c
local_milli_t2.reg n.lat_0/clka
                                   cl_invvn07c
local milli t2.reg n.lat 0/scan in
                                    cl invvn07c
bht_block.reg_n.lat_0/clka
                                   cl_invvn07d
bht_block.reg n.lat 0/scan_in
                                    cl_invvn07d
srlz_blk.reg_n.lat_0/clka
                                 cl_nnd2n07c
srlz_blk.reg_n.lat_0/scan_in
                                   cl_nnd2n07c
exc cond.reg n.lat 0/clka
                                   cl invvn07d
exc_cond.reg_n.lat_0/scan_in
                                     cl_invvn07d
slow_mode_dly.reg_n.lat_0/clka
                                      cl_invvn07d
slow mode dly.reg n.lat 0/scan in
                                       cl invvn07d
dcd_succ_disable_scan.reg_n.lat_0/clka
                                         cl invvn07d
dcd_succ_disable_scan.reg_n.lat_0/scan_in_cl_invvn07d
dcd succ disable scan.reg n.lat 1/clka
                                         cl invvn07d
dcd_succ_disable_scan.reg_n.lat_1/scan_in_cl_invvn07d
dcd_succ disable scan.reg n.lat 2/clka
                                        cl invvn05d
dcd succ disable scan.reg n.lat 2/scan in cl invvn05d
drain_blk.reg_n.lat_0/clka
                                  cl_nnd2n07c
drain_blk.reg_n.lat_0/scan_in
                                    cl_nnd2n07c
dcd_ilc.req_n.lat_0/clka
                                 cl_nnd2n07c
dcd_ilc.reg_n.lat_0/scan_in-
                             -----cl<u>-</u>nnd2n07c
dcd_ilc.reg_n.lat_1/clka cl_nnd3n07c
dcd_ilc.reg_n.lat_1/scan_in
                                   cl nnd3n07c
slow_mode_blk.reg_n.lat_0/clka
                                      cl nnd2n07c
slow_mode_blk.reg_n.lat_0/scan_in cl_nnd2n07c
op_cmp_44.reg_n.lat_0/clka_
                              cl invvn07d
op_cmp_44.reg_n.lat_0/scan_in
                                      cl invvn07d
                                     cl_nnd2n07c
op_cmp_dsbl.reg_n.lat_0/clka
op_cmp_dsbl.reg_n.lat_0/scan_in
                                       cl nnd2n07c
eu_frc_milli.reg_n.lat_0/clka
                                   cl invvn07d
                                    cl_invvn07d
eu_frc_milli.reg_n.lat_0/scan_in
bcr store stat.reg n.lat 0/clka
                                    cl ao22n07c
bcr_store_stat.reg_n.lat_0/scan_in
                                      cl_ao22n07c
                                  cl_ao22n07c
exc_info.reg_n.lat_0/clka
exc_info.reg_n.lat_0/scan_in
                                    cl_ao22n07c
exc_info.reg_n.lat_1/clka
                                  cl ao22n07c
exc_info.reg_n.lat_1/scan_in
                                    cl ao22n07c
exc info.reg n.lat 2/clka
                                  cl ao22n07c
exc_info.reg_n.lat_2/scan_in
                                    cl ao22n07c
exc_info.reg_n.lat_3/clka
                                  cl ao22n07c
exc_info.reg_n.lat_3/scan_in
                                    cl ao22n07c
spare.reg_n.lat_0/clka
                                 cl invvn07d
spare.reg_n.lat_0/scan_in
                                   cl invvn07d
mcset_e1.reg_n.lat_0/clka
                                   cl invvn07c
mcset_e1.reg_n.lat_0/scan_in
                                     cl invvn07c
eu_iu_spare.reg_n.lat_0/clka
                                    cl invvn07d
eu_iu_spare.reg_n.lat_0/scan_in
                                      cl_invvn07d
dsbl_ovrlp_blk.reg_n.lat_0/clka
                                    cl_nnd2n07c
dsbl ovrlp blk.reg n.lat 0/scan in
                                      cl nnd2n07c
                                  cl_invvn07d
inst_fetch.reg_n.lat_0/clka
                                    cl invvn07d
inst_fetch.reg_n.lat_0/scan_in
iu_dsbl_ovrlp.reg_n.lat_0/clka
                                    cl nor2n06c
```

iu\_dsbl\_ovrlp.reg\_n.lat\_0/scan\_in cl nor2n06c cl\_nnd2n07c ex\_in\_prog.reg\_n.lat\_0/clka ex\_in\_prog.reg\_n.lat\_0/scan\_in cl nnd2n07c cl\_invvn06d blk\_dcd.reg\_n.lat\_0/clka cl invvn06d blk dcd.reg\_n.lat\_0/scan\_in cl\_invvn06d blk\_dcd.reg\_n.lat\_1/clka cl\_invvn06d blk dcd.reg n.lat 1/scan\_in blk dcd.reg\_n.lat\_2/clka cl invvn06d blk dcd.req\_n.lat\_2/scan\_in cl\_invvn06d cl\_ao21n07c blk\_dcd.reg\_n.lat\_3/clka blk\_dcd.reg\_n.lat\_3/scan\_in cl ao21n07c cl\_invvn07c dcd succ dly.req\_n.lat\_0/clka dcd\_succ\_dly.reg\_n.lat\_0/scan\_in cl\_invvn07c exec\_recov.reg\_n.lat\_0/clka cl nnd2n07c cl\_nnd2n07c exec\_recov.reg\_n.lat\_0/scan\_in ru\_updt\_dly.reg\_n.lat\_0/clka cl\_invvn07d cl\_invvn07d ru updt\_dly.reg\_n.lat\_0/scan\_in cl\_invvn07c iu rst\_fst\_t1.reg\_n.lat\_0/clka cl\_invvn07c iu\_rst\_fst\_t1.reg\_n.lat\_0/scan\_in cl\_invvn07d inst\_store.reg\_n.lat\_0/clka cl\_invvn07d inst store.reg n.lat 0/scan\_in cl invvn07d eu dsbl\_aftr.reg\_n.lat\_0/clka cl invvn07d eu\_dsbl\_aftr.reg\_n.lat\_0/scan\_in dcdsuc err.reg n.lat\_0/clka cl\_nnd2n07c dcdsuc\_err.reg\_n.lat\_0/scan\_in cl\_nnd2n07c cl\_nnd2n07c dcd\_cyl\_cnt.reg\_n.lat\_0/clka dcd\_cyl\_cnt.reg\_n.lat\_0/scan\_in cl\_nnd2n07c dcd\_cyl\_cnt.reg\_n.lat\_1/clkacl\_nnd3n07c dcd\_cyl\_cnt.reg\_n.lat\_1/scan\_in cl\_nnd3n07c cl\_nnd2n07c blk\_mcend.reg\_n.lat\_0/clka cl\_nnd2n07c blk-mcend.reg\_n.lat\_0/scan\_in cl\_invvn06c op 44 info.reg\_n.lat\_0/clka cl\_invvn06c op 44 info.reg n.lat\_0/scan\_in op\_44\_info.reg\_n.lat\_1/clka cl invvn06c cl invvn06c op 44\_info.reg\_n.lat\_1/scan\_in cl\_invvn07d rcvrv reset.reg\_n.lat\_0/clka rcvry\_reset.reg\_n.lat\_0/scan\_in cl\_invvn07d cl oa21n07c br\_wrongs.reg\_n.lat\_0/clka cl\_oa21n07c br wrongs.reg\_n.lat\_0/scan\_in cl\_invvn07d rstrt\_reset.reg\_n.lat\_0/clka cl invvn07d rstrt\_reset.reg\_n.lat\_0/scan\_in cl\_nnd2n07c br dcd\_pend.reg\_n.lat\_0/clka br\_dcd\_pend.reg\_n.lat\_0/scan\_in ci\_nnd2n07c

\*\*\*\*\*\*\*\*\*\*\*\* Timing Checks Not Performed \*

## <<< none >>>

## \*\*\*\*\*\* SUMMARY \*\*\*\*\*\*\*\*

Total Number of CAP violations :: 69
Total Number of Early SLEW violations :: 79
Total Number of Late SLEW violations :: 159
Total Number of Sourceless Pins :: 0
Total Number of Sinkless Pins :: 0
Total Number of Pathless Pins :: 181
Total Number of Timing checks not performed :: 0

## **Timing Correction Accounting Results**

Transform - repower

Tested: 4048, Applied: 123, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0822, Max: 140.6079, Avg: 14.9094 % -> Min: 0.0247, Max: 1204.4907, Avg: 26.2961 (Crit) % -> Min: 0.0044, Max: 6.1281, Avg: 0.7524

Area Cost -> Min: -4.0000, Max: 11.0000, Avg: 0.6098 % -> Min: -0.0859, Max: 0.2388, Avg: 0.0133

**Total Averages** 

Run Time:

0.0000

Slack Gain: 1833.8529

Area Cost:

75.0000

Transform - clone

Tested: 57, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time:

0.0000

Transform - fantom

Tested: 39, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time:

0.0000

Transform - faniny

Tested: 39, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 12.0017, Max: 12.0017, Avg: 12.0017 % -> Min: 0.6101, Max: 0.6101, Avg: 0.6101 (Crit) % -> Min: 0.6101, Max: 0.6101, Avg: 0.6101

Area Cost -> Min: 2.0000, Max: 2.0000, Avg: 2.0000 % -> Min: 0.0434, Max: 0.0434, Avg: 0.0434

**Total Averages** Run Time: 0.0000 Slack Gain: 12.0017 Area Cost: 2.0000 Transform - onebuff Tested: 2467, Applied: 0, Corrected: 0 Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 **Total Averages** Run Time: 0.0000 Transform - dinv Tested: 2454, Applied: 22, Corrected: 0 Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 Slack Gain -> Min: 0.0500, Max: 2042.1168, Avg: 164.9743 %-> Min: 0.0074, Max: 95.4595, Avg: 26.1605 (Crit) % -> Min: 0.0026, Max: 91.0505, Avg: 7.5052 Area Cost -> Min: -17.0000, Max: 0.0000, Avg: -3.8182 % -> Min: -0.3668, Max: 0.0000, Avg: -0.0836 Total Averages Run Time: 0.0000 Slack Gain: 3629.4342 -84.0000 Area Cost: Transform - tpushb Tested: 6, Applied: 0, Corrected: 0 Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 **Total Averages** 

Total Averages

Run Time: 0.0000

Transform - tpushl
Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time: 0.0000

Transform - tpushr

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time: 0.0000

Transform - tbmove

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time: 0.0000

Transform - tswap

Tested: 836, Applied: 59, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0001, Max: 20.6266, Avg: 4.2551 % -> Min: 0.0000, Max: 2.9882, Avg: 0.7086 (Crit) % -> Min: 0.0000, Max: 1.2355, Avg: 0.2272

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time: 0.0000

Slack Gain: 251.0519

Area Cost: 0.0000

Transform - tsteal

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time: 0.0000

Transform - tcte

Tested: 364, Applied: 4, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 13.5331, Max: 39.8060, Avg: 30.0562 % -> Min: 3.4911, Max: 33.9806, Avg: 14.4824 (Crit) % -> Min: 0.6789, Max: 1.9969, Avg: 1.5078

Area Cost -> Min: -2.0000, Max: -2.0000, Avg: -2.0000 % -> Min: -0.0442, Max: -0.0441, Avg: -0.0442

**Total Averages** 

Run Time:

0.0000

Slack Gain:

120.2248

Area Cost:

-8.0000

Transform - texpand

Tested: 1428, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 1.0000, Max: 1.0000, Avg: 1.0000 % -> Min: 0.0667, Max: 0.0667, Avg: 0.0667 (Crit) % -> Min: 0.0506, Max: 0.0506, Avg: 0.0506

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time:

Slack Gain:

Area Cost:

Transform - trecover

Tested: 683, Applied: 3, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 5.3128, Max: 20.5709, Avg: 12.3908 % -> Min: 0.6576, Max: 1.9107, Avg: 1.3506 (Crit) % -> Min: 0.2701, Max: 1.0457, Avg: 0.6299

Area Cost -> Min: -1.0000, Max: 4.0000, Avg: 1.3333 % -> Min: -0.0217, Max: 0.0870, Avg: 0.0290

**Total Averages** 

Run Time:

0.0000

Slack Gain:

37.1723

Area Cost:

4.0000

Transform - texpao

Tested: 12, Applied: 0, Corrected: 0

**Total Averages** 

Run Time:

0.0000

Transform - tmerge

Tested: 353, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time:

0.0000

Transform - tncube

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time:

0.0000

Transform - tdual\_correct

Tested: 702, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Total Averages

Run Time:

0.0000

Transform - speedreg

Tested: 598, Applied: 28, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0005, Max: 4.8468, Avg: 0.8625 % -> Min: 0.0001, Max: 1.9721, Avg: 0.2321 (Crit) % -> Min: 0.0000, Max: 0.2479, Avg: 0.0441

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**Total Averages** 

Run Time:

0.0000

Slack Gain:

24.1497

Area Cost:

0.0000

Transform - absrbreg

Tested: 598, Applied: 0, Corrected: 0

Total Averages.

Run Time:

0.0000

Information By Driver

Transform - repower

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 494, Applied: 31, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.5562, Max: 140.6079, Avg: 12.6121 % -> Min: 0.0247, Max: 6.1281, Avg: 0.5969 (Crit) % -> Min: 0.0247, Max: 6.1281, Avg: 0.5919

Area Cost -> Min: -4.0000, Max: 11.0000, Avg: 2.5484 % -> Min: -0.0859, Max: 0.2388, Avg: 0.0554

NonCritical

Tested: 3554, Applied: 92, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0822, Max: 66.5485, Avg: 15.6834 % -> Min: 0.0265, Max: 1204.4907, Avg: 34.9557 (Crit) % -> Min: 0.0044, Max: 3.4038, Avg: 0.8065

Area Cost -> Min: -4.0000, Max: 0.0000, Avg: -0.0435 % -> Min: -0.0859, Max: 0.0000, Avg: -0.0009

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - clone

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 57, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - fantom

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 39, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - faniny

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 39, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 12.0017, Max: 12.0017, Avg: 12.0017 % -> Min: 0.6101, Max: 0.6101, Avg: 0.6101 (Crit) % -> Min: 0.6101, Max: 0.6101, Avg: 0.6101

Area Cost -> Min: 2.0000, Max: 2.0000, Avg: 2.0000 % -> Min: 0.0434, Max: 0.0434, Avg: 0.0434

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - onebuff

Quick

Tested: 1266, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 1189, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - dinv

Quick

Tested: 1256, Applied: 15, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 50.2148, Max: 2042.1168, Avg: 241.9390 % -> Min: 2.3647, Max: 95.4595, Avg: 38.3639 (Crit) % -> Min: 2.2389, Max: 91.0505, Avg: 11.0064

Area Cost -> Min: -17.0000, Max: 0.0000, Avg: -4.2667 % -> Min: -0.3668, Max: 0.0000, Avg: -0.0939

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical.

Tested: 1186, Applied: 7, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: \_0.0000

Slack Gain -> Min: 0.0500, Max: 0.0500, Avg: 0.0500 % -> Min: 0.0074, Max: 0.0156, Avg: 0.0103 (Crit) % -> Min: 0.0026, Max: 0.0026, Avg: 0.0026

Area Cost -> Min: -4.0000, Max: -2.0000, Avg: -2.8571 % -> Min: -0.0862, Max: -0.0430, Avg: -0.0615

Correct

Tested: 0, Applied: 0, Corrected: 0

,,\_\_\_\_

Transform - tpushb

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tpushl

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tpushr

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tbmove

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tswap

Quick

Tested: 737, Applied: 52, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0001, Max: 20.6266, Avg: 3.9889 % -> Min: 0.0000, Max: 2.9882, Avg: 0.7845

(Crit) % -> Min: 0.0000, Max: 1.2355, Avg: 0.2213

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 99, Applied: 7, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.3071, Max: 14.5166, Avg: 6.2324 % -> Min: 0.0000, Max: 0.6232, Avg: 0.1450 (Crit) % -> Min: 0.0134, Max: 0.6232, Avg: 0.2706

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tsteal

Quick .....

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tcte

Quick

Tested: 358, Applied: 4, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 13.5331, Max: 39.8060, Avg: 30.0562 % -> Min: 3.4911, Max: 33.9806, Avg: 14.4824 (Crit) % -> Min: 0.6789, Max: 1.9969, Avg: 1.5078

Area Cost -> Min: -2.0000, Max: -2.0000, Avg: .-2.0000 % -> Min: -0.0442, Max: -0.0441, Avg: -0.0442

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - texpand

Quick

Tested: 1410, Applied: 1, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 1.0000, Max: 1.0000, Avg: 1.0000 % -> Min: 0.0667, Max: 0.0667, Avg: 0.0667 (Crit) % -> Min: 0.0506, Max: 0.0506, Avg: 0.0506

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 18, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical:

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - trecover

Quick

Tested: 683, Applied: 3, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 5.3128, Max: 20.5709, Avg: 12.3908 % -> Min: 0.6576, Max: 1.9107, Avg: 1.3506 (Crit) % -> Min: 0.2701, Max: 1.0457, Avg: 0.6299

Area Cost -> Min: -1.0000, Max: 4.0000, Avg: 1.3333 % -> Min: -0.0217, Max: 0.0870, Avg: 0.0290

Critical

Tested: 0, Applied: 0, Corrected: 0

NonCritical

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - texpao

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 12, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tmerge

Quick

Tested: 353, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Critical

Tested: 0, Applied: 0, Corrected: 0

NonCritical ----

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tncube

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - tdual\_correct

Quick

Tested: 702, Applied: 0, Corrected: 0

Critical

Tested: 0, Applied: 0, Corrected: 0

**NonCritical** 

Tested: 0, Applied: 0, Corrected: 0

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - speedreg

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time. -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

NonCritical

Tested: 592, Applied: 28, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Slack Gain -> Min: 0.0005, Max: 4.8468, Avg: 0.8625 % -> Min: 0.0001, Max: 1.9721, Avg: 0.2321 (Crit) % -> Min: 0.0000, Max: 0.2479, Avg: 0.0441

Area Cost -> Min: 0.0000, Max: 0.0000, Avg: 0.0000 % -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Correct

Tested: 0, Applied: 0, Corrected: 0

Transform - absrbreg

Quick

Tested: 0, Applied: 0, Corrected: 0

Critical

Tested: 6, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

**NonCritical** 

Tested: 592, Applied: 0, Corrected: 0

Run Time -> Min: 0.0000, Max: 0.0000, Avg: 0.0000

Correct

Tested: 0, Applied: 0, Corrected: 0

> write\_end\_point\_report -points 2
[ET-0018]: >Begin...New EndPoint Report

for file /tmp/end\_point\_report..92476. [ET-0019]: <End.....New Endpoint Report.

0 dcd\_succ\_last\_t1&0

----> C167/a 1594 N675

---->{a} C2738/y

----> C2738/a 19 last\_cycle

0 N675

Sun Apr 18 22:09:41 1999 Part: IDCDSUC **EDA EinsTimer EndPoint Report** Mode: Late Mode / Nominal Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Max. Slack: 1.13427E+38 Min. Slack: -1.13427E+38 Max. Endpoints: 2 Sort Field: Slack Abbreviation Comparison/Description Cause of Slack Slack due to a point downstream on path SlkCont Slack Continuation ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) RAT Required Arrival Time ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL Asserted Required Arrival Time AssrtRAT ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK ClkGSet **Clock Gating Setup** ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK CIkGHId Clock Gating Hold ARRIVAL TIME + ADJUST ) ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK Clock Tree Pulse Width **CIKTPW** TRAILING EDGE ) ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + Setup Setup ADJUST) ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + Hold Hold ADJUST) ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + EndOfCycle · **EndOfC** ADJUST) ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK **CIkPW** ClockPulseWidth TRAILING EDGE) ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ClockSeparation ClkSep ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM **ALTest** Loop CLOCK + ADJUST ) Slack discontinuity due to failed test **ATLimit** Arrival Time Limiting Delay/ Failed Test/ LimitedAT/ Num/ AT Slack Slew CL FO Cell P Func T.Adj E Phase Test PinName NetName 2668 -1669 3294 1011 1 PO 0 R C3+R 1 dcd\_succ\_last\_t1 dcd\_succ\_last\_t1 999 RAT 2668 -1669 3294 1011 1 IOPAD **IOPAD** R C3+R ----> BOX714/OUT 0 dcd succ last\_t1 **IOPAD** 2668 -1669 3294 1011 1 IOPAD RC3+R ---> BOX714/IN 0 dcd\_succ\_last\_t1&0 2668 -1669 3294 1011 1 cs\_invvv 01c NOT R C3+R ----> C167/y

FC3+R

FC3+R

RC3+R

1075 -1669

1075 -1669

1056 -1669

27

27 139 4 cs\_invvv 01c NOT

139 4 cs\_nnd2x 14b NAND

33 114 1 cs\_nnd2x 14b NAND

```
---->{b} C2487/y
                                        1056 -1669
                               RC3+R
                                                     33 114 1 cs_nnd2x 14e NAND
0 last_cycle
----> C2487/a
                              FC3+R
                                        1035 -1669
                                                     22 145 3 cs_nnd2x 14e NAND
21 N1587
----> C1952/y
                                                     22 145 3 cs_invvv 19b NOT
                              FC3+R
                                        1035 -1669
                                                                                   0
N1587
----> C1952/a
                              R C3+R
                                        1024 -1669
                                                     80
                                                        319 1 cs invvv 19b NOT
11 num_dcd_cyl&0(1)
----> BOX679/OUT
                                 RC3+R
                                           1024 -1669
                                                        80 319 1 IOPAD
                                                                            IOPAD
0 num_dcd_cyl&0(1)
----> BOX679/IN
                                RC3+R
                                         1024 -1669
                                                      80 319 1 IOPAD
                                                                          IOPAD
                                                                                   0
num_dcd_cyl(1)
----> num_dcd_cyl(1)
                                 RC3+R
                                          1024 -1669
                                                       80 319 1 PI
                                                                               0
num_dcd_cyl(1)
   2 iu_reset_op_c_t1
                                R C3+R
                                          2399 -1400 3318 1011 1 PO
                                                                                 0
iu_reset_op_c_t1
RAT
                                  999
----> BOX716/OUT
                                 R C3+R
                                          2399 -1400 3318 1011 1 IOPAD
                                                                          JOPAD
0 iu_reset op c t1
----> BOX716/IN
                               RC3+R
                                         2399 -1400 3318 1044 3 IOPAD
                                                                            IOPAD
0 iu_reset_op_c_t1&0
---->{a} C2393/y
                                        2399 -1400 3318 1044 3 cs_nnd2v 02c NAND
                               R C3+R
0 iu_reset_op_c_t1&0
----> C2393/a
                              FC3+R
                                        536 -1400 100 196 6 cs_nnd2v
                                                                        02c NAND
1863 gbfonet_6
----> gbfocell_6/y
                              F.C3+R 536 -1400 100 196 6 cs_invvv
                                                                       09c NOT
0 gbfonet 6
----> gbfocell_6/a
                              R C3+R
                                        472 -1400 184 44 1 cs invvv 09c NOT
64 N2031
---->{b} C2162/v
                              R C3+R 472 -1400 184 44 1 cs nnd3v 02c NAND
0 N2031
----> C2162/a
                              FC3+R
                                        358 -1400 144 217 5 cs_nnd3v 02c NAND ....
114 rcvry reset a
----> rcvry_reset.reg_n.lat_0/l2_out_n
                                    FC3+R
                                              358 -1400 144 217 5 cl invvn 07d
SRL
       0 rcvry_reset_q
----> rcvry_reset.reg_n.lat_0/c2
                                  R C3+
                                         160
                                                 N/C
                                                       60 222 13 cl_invvn 07d SRL
198 slow_mode.c2_1
----> slow_mode.clockblock/c2
                                    R C3+
                                             160
                                                  N/C
                                                        60 222 13 cb_clk_32_1 LCB
0 slow_mode.c2_1
```

[padnet]: Added 0 IOPADs.

Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte\_utils.tcl

<sup>&</sup>gt; tiegen FOLIM(1)

<sup>&</sup>gt; padnet

<sup>&</sup>gt; idm::get\_active\_network

<sup>&</sup>gt; idm::foreach\_proto\_pin po -protobox \_\_CiType\_16\_30a98de8...

<sup>&</sup>gt; idm::object\_name \_\_CiType\_17\_30aac34c

<sup>&</sup>gt; idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac34c > idm::object\_name \_\_CiType\_20\_3057fc90

<sup>[</sup>CTE::fixup\_po\_nets]: (I) PO net 'N36' doesn't match PO 'iu\_eu\_opcode\_cmp' -> attempting to rename > idm::locate\_net -name iu\_eu\_opcode\_cmp -proto\_box \_\_CiTy...

<sup>&</sup>gt; idm::set\_net\_name -net \_\_CiType\_20\_3057fc90 -name iu\_eu\_...

```
> idm::object_name __CiType_17_30aac328
     > idm::get_net_from_proto_pin __CiType_17_30aac328
       > idm::object_name __CiType_20_30590568
[CTE::fixup_po_nets]: (I) PO net 'N158' doesn't match PO 'iu_rcvry_reset' -> attempting to rename
        > idm::locate_net -name iu_rcvry_reset -proto_box __CiType...
         > idm::set_net_name -net __CiType_20_30590568 -name iu_rcv...
     > idm::object_name __CiType_17_30aac304
     > idm::get_net_from_proto_pin __CiType_17_30aac304
       > idm::object_name __CiType_20_3058f6e0
     > idm::object_name __CiType_17_30aac2e0
     > idm::get_net_from_proto_pin __CiType_17_30aac2e0
> idm::object_name __CiType_20_3057f6c8
     > idm::object_name __CiType_17_30aac2bc
      > idm::get_net_from_proto_pin __CiType_17_30aac2bc
       > idm::object_name __CiType_20_3057fe48
[CTE::fixup_po_nets]: (I) PO net 'N12' doesn't match PO 'iu_milli_mode' -> attempting to rename
        > idm::locate_net -name iu_milli_mode -proto_box __CiType_...
         > idm::set_net_name -net __CiType_20_3057fe48 -name iu_mil...
      > idm::object_name __CiType_17_30aac298
      > idm::get_net_from_proto_pin __CiType_17_30aac298
       > idm::object_name __CiType_20_3059af68
      > idm::object_name __CiType_17_30a4bda8
     > idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
[CTE::fixup_po_nets]: (I) PO net 'N2086' doesn't match PO 'dcd_succ_last' -> attempting to rename
        > idm::locate_net -name dcd_succ_last -proto_box ___CiType_...
         > idm::set_net_name -net __CiType_20_3059ae78 -name dcd_su...
     > idm::object_name __CiType_17_30a4bd84
      > idm::get_net_from_proto_pin __CiType_17_30a4bd84
_> idm::object_name __CiType_20_3057fd58
[CTE::fixup_po_nets]: (I) PO net 'N26' doesn't match PO 'iu_eu_op_nomatch' -> attempting to rename
        > idm::locate net -name iu_eu_op_nomatch -proto_box __CiTy...
          > idm::set_net_name -net __CiType_20_3057fd58 -name iu_eu_...
      > idm::object_name __CiType_17_30a4bd60
      > idm::get_net_from_proto_pin __CiType_17_30a4bd60
> idm::object_name __CiType_20_30568e50
      > idm::object_name __CiType_17_30a4bd3c
      > idm::get_net_from_proto_pin __CiType_17_30a4bd3c
       > idm::object_name __CiType_20_3057fcb8
[CTE::fixup_po_nets]: (I) PO net 'N34' doesn't match PO 'id_xcute_targ' -> attempting to rename
        > idm::locate_net -name id_xcute_targ -proto_box __CiType_...
          > idm::set_net_name -net __CiType_20_3057fcb8 -name id_xcu...
      > idm::object_name __CiType_17_30a4bd18
      > idm::get_net_from_proto_pin __CiType_17_30a4bd18
       > idm::object_name __CiType_20_3057fdf8
[CTE::fixup_po_nets]: (I) PO net 'N14' doesn't match PO 'xc_frc_ia_to_if_t1' -> attempting to rename
        > idm::locate_net -name xc_frc_ia_to_if_t1 -proto_box __Ci...
          > idm::set_net_name -net __CiType_20_3057fdf8 -name xc_frc...
      > idm::object_name __CiType_17_30a4bcf4
      > idm::get_net_from_proto_pin __CiType_17_30a4bcf4
       > idm::object_name __CiType_20_3057f6a0
[CTE::fixup_po_nets]: (I) PO net 'N2097' doesn't match PO 'dcd_success_tr' -> attempting to rename
         > idm::locate_net -name dcd_success_tr -proto_box __CiType...
          > idm::set_net_name -net __CiType_20_3057f6a0 -name dcd_su...
      > idm::object_name __CiType_17_30a4bcd0
```

```
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
       > idm::object_name __CiType_20_3056a2c8
      > idm::object_name __CiType_17_30a4bcac
      > idm::get_net_from_proto_pin __CiType_17_30a4bcac
       > idm::object_name __CiType_20_30568d88
      > idm::object_name __CiType_17_30a4bc88
      > idm::get_net_from_proto_pin __CiType_17_30a4bc88
       > idm::object_name __CiType_20_3057ff60
[CTE::fixup_po_nets]: (I) PO net 'N0' doesn't match PO 'iu_slow_mode' -> attempting to rename
        > idm::locate_net -name iu_slow_mode -proto_box ___CiType_1...
          > idm::set_net_name -net __CiType_20_3057ff60 -name iu_slo...
      > idm::object_name __CiType_17_30a4bc64
  ----> idm::get_net_from_proto_pin __CiType_17_30a4bc64
       > idm::object_name __CiType_20_3058fe60
      > idm::object_name __CiType_17_30a4bc40
      > idm::get_net_from_proto_pin __CiType_17_30a4bc40
       > idm::object_name __CiType_20_3057fdd0
[CTE::fixup_po_nets]: (I) PO net 'N16' doesn't match PO 'xc_frc_milli' -> attempting to rename
      > idm::locate_net -name xc_frc_milli -proto_box __CiType_1...
         > idm::set_net_name -net __CiType_20_3057fdd0 -name xc_frc...
      > idm::get_net_from_proto_pin __CiType_17_30a4bc1c
      > idm::object_name __CiType_17_30a4bc1c
     > idm::object_name __CiType_17_30a4bbf8
> idm::object_name __CiType_17_30a4bbf8
> idm::object_name __CiType_17_30a4bbf8
> idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
   > idm::get_net_from_proto_pin __CiType_17_30a4bbb0
> idm::object_name __CiType_20_3057fa60

E::fixup_po_netsl: (i) PO_pet Negocial
[CTE::fixup_po_nets]: (I) PO net 'N2089' doesn't match PO 'iu_milli_mode_t1' -> attempting to rename
        > idm::locate_net -name iu_milli_mode_t1 -proto_box __CiTy...
> idm::set_net_name -net __CiType_20_3057fa60 -name iu_mil...
      > idm::object_name __CiType_17_30a4bb8c
     > idm::get_net_from_proto_pin __CiType_17_30a4bb8c
> idm::object_name __CiType_20_3057f628
[CTE::fixup_po_nets]: (I) PO net 'N72' doesn't match PO 'iu_milli_mode_t2' -> attempting to rename
         > idm::locate_net -name iu_milli_mode_t2 -proto_box __CiTy...
          > idm::set_net_name -net __CiType_20_3057f628 -name iu_mil...
      > idm::object_name __CiType_17_30a4bb44
      > idm::get_net_from_proto_pin __CiType_17_30a4bb44
> idm::object_name __CiType_20_3057fa38
[CTE::fixup_po_nets]: (I) PO net 'N2090' doesn't match PO 'iu_milli_mode_t3' -> attempting to rename
         > idm::locate_net -name iu_milli_mode_t3 -proto_box __CiTy...
          > idm::set_net_name -net __CiType_20_3057fa38 -name iu_mil...
      > idm::object_name __CiType_17_30a4bb20
      > idm::get_net_from_proto_pin __CiType_17_30a4bb20
> idm::object_name __CiType_20_3057fc68
[CTE::fixup_po_nets]: (I) PO net 'N42' doesn't match PO 'xc_frc_milli_t1' -> attempting to rename
         > idm::locate_net -name xc_frc_milli_t1 -proto_box __CiTyp...
          > idm::set_net_name -net __CiType_20_3057fc68 -name xc_frc...
      > idm::object_name __CiType_17_30a4bad8
      > idm::get_net_from_proto_pin __CiType_17_30a4bad8
        > idm::object_name __CiType_20_3057f600
[CTE::fixup_po_nets]: (I) PO net 'N2096' doesn't match PO 'iu_exc_cond' -> attempting to rename
         > idm::locate_net -name iu_exc_cond -proto_box __CiType_16...
```

```
> idm::set_net_name -net __CiType_20_3057f600 -name iu_exc...
      > idm::object_name __CiType_17_30a4bab4
      > idm::get_net_from_proto_pin __CiType_17_30a4bab4
       > idm::object_name __CiType_20_3057fa10
[CTE::fixup_po_nets]: (I) PO net 'N80' doesn't match PO 'slow_mode_tr' -> attempting to rename
        > idm::locate_net -name slow_mode_tr -proto_box __CiType_1...
         > idm::set_net_name -net __CiType_20_3057fa10 -name slow_m...
      > idm::object_name __CiType_17_30a4ba90
      > idm::get_net_from_proto_pin __CiType_17_30a4ba90
       > idm::object_name __CiType_20_3057fd80
[CTE::fixup_po_nets]: (I) PO net 'N22' doesn't match PO 'iu_eu_slow_mode' -> attempting to rename
        > idm::locate_net -name iu_eu_slow_mode -proto_box __CiTyp...
         > idm::set_net_name -net __CiType_20_3057fd80 -name iu_eu_...
      > idm::object_name __CiType_17_30a4ba6c
      > idm::get_net_from_proto_pin __CiType_17_30a4ba6c
       > idm::object_name __CiType_20_30568c98
      > idm::object_name __CiType_17_30a4ba48
      > idm::get_net_from_proto_pin __CiType_17_30a4ba48
> idm::object_name __CiType_20_3057f650
[CTE::fixup_po_nets]: (I) PO net 'N70' doesn't match PO 'iu_milli_mode_tr' -> attempting to rename
        > idm::locate_net -name iu_milli_mode_tr -proto_box __CiTy...
         > idm::set_net_name -net __CiType_20_3057f650 -name iu_mil...
     > idm::object_name __CiType_17_30a4ba24 ----
     > idm::get_net_from_proto_pin __CiType_17_30a4ba24
       > idm::object_name __CiType_20_3057f7b8
[CTE::fixup_po_nets]: (I) PO net 'N140' doesn't match PO 'iu_reset_if' -> attempting to rename
        > idm::locate_net -name iu_reset_if -proto_box __CiType_16...
         > idm::set_net_name -net CiType_20_3057f7b8 -name iu_res...
      > idm::object_name __CiType_17_30a4ba00
     > idm::get_net_from_proto_pin __CiType_17_30a4ba00
       > idm::object_name __CiType_20_3058fbb8
[CTE::fixup_po_nets]: (I) PO net 'N78' doesn't match PO 'exc_cond_tr' -> attempting to rename
        > idm::locate_net -name exc_cond_tr -proto_box __CiType_16...
         > idm::set_net_name -net __CiType_20_3058fbb8 -name exc_co...
      > idm::object_name __CiType_17_30a4b9dc
      > idm::get_net_from_proto_pin __CiType_17_30a4b9dc
> idm::object_name __CiType_20_3059b1c0
[CTE::fixup_po_nets]: (I) PO net 'N2088' doesn't match PO 'dcd_succ_first' -> attempting to rename
        > idm::locate_net -name dcd_succ_first -proto_box __CiType...
         > idm::set_net_name -net __CiType_20_3059b1c0 -name dcd_su...
      > idm::object_name __CiType_17_30a4b9b8
      > idm::get_net_from_proto_pin __CiType_17_30a4b9b8
> idm::object_name __CiType_20_3057f808
[CTE::fixup_po_nets]: (I) PO net 'N136' doesn't match PO 'execute_recovery' -> attempting to rename
        > idm::locate net -name execute_recovery -proto_box __CiTy...
          > idm::set_net_name -net __CiType_20_3057f808 -name execut...
      > idm::object_name __CiType_17_30a4b994
      > idm::get_net_from_proto_pin __CiType_17_30a4b994
       > idm::object_name __CiType_20_3059b648
      > idm::object_name __CiType_17_30a4b970
      > idm::get_net_from_proto_pin __CiType_17_30a4b970
       > idm::object_name __CiType_20_3057fec0
[CTE::fixup_po_nets]: (I) PO net 'N8' doesn't match PO 'xc_frc_ia_to_if' -> attempting to rename
         > idm::locate_net -name xc_frc_ia_to_if -proto_box __CiTyp...
          > idm::set_net_name -net __CiType_20_3057fec0 -name xc_frc...
```

```
> idm::object_name __CiType_17_30a4b94c
             > idm::get_net_from_proto_pin __CiType_17_30a4b94c
               > idm::object_name __CiType_20_3057fda8
       [CTE::fixup_po_nets]: (I) PO net 'N18' doesn't match PO 'iu_slow_mode_t1' -> attempting to rename
                > idm::locate_net -name iu_slow_mode_t1 -proto_box __CiTyp...
                 > idm::set_net_name -net __CiType_20_3057fda8 -name iu_slo...
             > idm::get_net_from_proto_pin __CiType_17_30a4b928
               > idm::object_name __CiType_20_3059b7d8
       [CTE::fixup_po_nets]: (I) PO net 'gptr_scan_out&1' doesn't match PO 'gptr_scan_out' -> attempting to
       rename
                > idm::locate_net -name gptr_scan_out -proto_box __CiType_...
                 > idm::set_net_name -net __CiType_20_3059b7d8 -name qptr s...
             > idm::object_name __CiType_17_30a4b904
             > idm::get_net_from_proto_pin __CiType_17_30a4b904
> idm::object_name __CiType_20_3057ff10
       [CTE::fixup_po_nets]: (I) PO net 'N4' doesn't match PO 'iu_reset_fst' -> attempting to rename
                > idm::locate net -name iu reset fst -proto box CiType 1...
                 > idm::set_net_name -net __CiType_20_3057ff10 -name iu_res...
     > idm::get_net_from_proto_pin __CiType_17_30a4b8bc
> idm::object_name __CiType_20_3059b8f0
  > idm::object_name __CiType_17_30a4b898

> idm::get_net_from_proto_pin __CiType_17_30a4b898

> idm::object_name __CiType_20_30590540

[CTE::fixup_po_nets]: (I) PO net 'N134' doesn't match PO 'iu_eu_dcd_succ_tr' -> attempting to rename

> idm::locate_net -name iu_eu_dcd_succ_tr -proto_box __CiT...

> idm::set_net_name -net__CiType_20_30590540 -name iu_eu_...
   > idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
-- [CTE::fixup_po_nets]: (I) PO net 'N146' doesn't match PO 'idcdsuc_err' -> attempting to rename
             > idm::object_name __CiType_17_30a4b874
> idm::object_name __CiType_20_3057f790
                > idm::locate_net -name idcdsuc_err -proto_box __CiType_16...
                 > idm::set_net_name -net __CiType_20_3057f790 -name idcdsu...
             > idm::object_name __CiType_17_30a4b850
             > idm::get_net_from_proto_pin __CiType_17_30a4b850
               > idm::object name CiType 20 3057fe70
       [CTE::fixup_po_nets]: (I) PO net 'N10' doesn't match PO 'frc_milli' -> attempting to rename
                > idm::locate_net -name frc_milli -proto_box __CiType_16_3...
             > idm::set_net_name -net __CiType_20_3057fe70 -name frc_milli
> idm::object_name __CiType_17_30a4b82c
             > idm::get_net_from_proto_pin __CiType_17_30a4b82c
               > idm::object_name __CiType_20_3057f998
       [CTE::fixup_po_nets]: (I) PO net 'N2092' doesn't match PO 'iu intrupt info(0)' -> attempting to rename
                > idm::locate_net -name iu_intrupt_info(0) -proto_box __Ci...
                 > idm::set_net_name -net __CiType_20_3057f998 -name iu_int...
             > idm::object_name __CiType_17_30a4b808
             > idm::get_net_from_proto_pin __CiType_17_30a4b808
               > idm::object_name __CiType_20_3057f970
       [CTE::fixup_po_nets]: (I) PO net 'N2093' doesn't match PO 'iu_intrupt_info(1)' -> attempting to rename
                > idm::locate_net -name iu_intrupt_info(1) -proto_box __Ci...
                 > idm::set_net_name -net __CiType_20_3057f970 -name iu_int...
             > idm::object_name __CiType_17_30a4b7e4
             > idm::get_net_from_proto_pin __CiType_17_30a4b7e4
               > idm::object_name __CiType_20_3057f948
```

```
[CTE::fixup_po_nets]: (I) PO net 'N2094' doesn't match PO 'iu_intrupt_info(2)' -> attempting to rename
        > idm::locate_net -name iu_intrupt_info(2) -proto_box __Ci...
         > idm::set_net_name -net __CiType_20_3057f948 -name iu_int...
     > idm::object_name __CiType_17_30a4b7c0
     > idm::get_net_from_proto_pin __CiType_17_30a4b7c0
      > idm::object_name __CiType_20_3057f920
[CTE::fixup_po_nets]: (I) PO net 'N2095' doesn't match PO 'iu_intrupt_info(3)' -> attempting to rename
        > idm::locate_net -name iu_intrupt_info(3) -proto_box __Ci...
         > idm::set net name -net __CiType_20_3057f920 -name iu_int...
     > idm::object_name __CiType_17_30a4b79c
     > idm::get_net_from_proto_pin __CiType_17_30a4b79c
       > idm::object_name __CiType_20_3057f8d0
[CTE::fixup_po_nets]: (I) PO net 'N126' doesn't match PO 'blk_dcd_info_tr(0)' -> attempting to rename
        > idm::locate_net -name blk_dcd_info_tr(0) -proto_box __Ci...
         > idm::set_net_name -net __CiType_20_3057f8d0 -name blk_dc...
      > idm::object_name __CiType_17_30a4b778
     > idm::get_net_from_proto_pin __CiType_17_30a4b778
       > idm::object_name __CiType_20_3057f880
[CTE::fixup_po_nets]: (I) PO net 'N128' doesn't match PO 'blk_dcd_info_tr(1)' -> attempting to rename
        > idm::locate_net -name blk_dcd_info_tr(1) -proto_box __Ci...
         > idm::set_net_name -net __CiType_20_3057f880 -name blk_dc...
      > idm::object_name __CiType_17_30a4b754
     > idm::get_net_from_proto_pin __CiType_17_30a4b754
      > idm::object_name __CiType_20_3057f858
[CTE::fixup_po_nets]: (I) PO net 'N130' doesn't match PO 'blk_dcd_info_tr(2)' -> attempting to rename
        > idm::locate_net -name blk_dcd_info_tr(2) -proto_box ....Ci...
         > idm::set_net_name -net __CiType_20_3057f858 -name blk_dc...
      > idm::object_name __CiType_17_30a4b730
      > idm::get_net_from_proto_pin __CiType_17_30a4b730
   > idm::object_name __CiType_20_3057f830
[CTE::fixup_po_nets]: (I) PO net 'N132' doesn't match PO 'blk_dcd_info_tr(3)' -> attempting to rename
        > idm::locate_net -name blk_dcd_info_tr(3) -proto_box___Ci...
         > idm::set_net_name -net __CiType_20_3057f830 -name blk_dc...
      > idm::object_name __CiType_17_30a4b70c
      > idm::get_net_from_proto_pin __CiType_17_30a4b70c
       > idm::object_name __CiType_20_3057fc40
[CTE::fixup_po_nets]: (I) PO net 'N44' doesn't match PO 'iu_srlz_op_encode(0)' -> attempting to rename
        > idm::locate_net -name iu_srlz_op_encode(0) -proto_box __...
         > idm::set_net_name -net __CiType_20_3057fc40 -name iu_srl...
      > idm::object_name __CiType_17_30a4b6e8
      > idm::get_net_from_proto_pin __CiType_17_30a4b6e8
       > idm::object_name __CiType_20_3057fc18
[CTE::fixup_po_nets]: (I) PO net 'N46' doesn't match PO 'iu_srlz_op_encode(1)' -> attempting to rename
      > idm::locate_net -name iu_srlz_op_encode(1) -proto_box __...
          > idm::set_net_name -net __CiType_20_3057fc18 -name iu_srl...
      > idm::object_name __CiType_17_30a4b6c4
      > idm::get_net_from_proto_pin __CiType_17_30a4b6c4
       > idm::object_name __CiType_20_3057fbf0
[CTE::fixup_po_nets]: (I) PO net 'N48' doesn't match PO 'iu_srlz_op_encode(2)' -> attempting to rename
         > idm::locate_net -name iu_srlz_op_encode(2) -proto_box __...
          > idm::set_net_name -net __CiType_20_3057fbf0 -name iu_srl...
      > idm::object_name __CiType_17_30a4b6a0
      > idm::get_net_from_proto_pin __CiType_17_30a4b6a0
       > idm::object_name __CiType_20_3057fbc8
[CTE::fixup_po_nets]: (I) PO net 'N50' doesn't match PO 'iu_srlz_op_encode(3)' -> attempting to rename
```

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> idm::locate_net -name iu_srlz_op_encode(3) -proto_box ___...
                        > idm::set_net_name -net __CiType_20_3057fbc8 -name iu_srl...
                    > idm::object_name __CiType_17_30a4b67c
                    > idm::get_net_from_proto_pin __CiType_17_30a4b67c
                      > idm::object_name __CiType_20_3057fba0
              [CTE::fixup_po_nets]: (I) PO net 'N52' doesn't match PO 'iu_srlz_op_encode(4)' -> attempting to rename
                       > idm::locate_net -name iu_srlz_op_encode(4) -proto_box ...
                        > idm::object_name __CiType_17_30a4b634
                    > idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
              [CTE::fixup_po_nets]: (I) PO net 'N54' doesn't match PO 'iu_srlz_op_encode(5)' -> attempting to rename
                   > idm::locate_net -name iu_srlz_op_encode(5) -proto_box_____
                        > idm::set_net_name -net __CiType_20_3057fb78 -name iu_srl...
                    > idm::object_name __CiType_17_30a4b5ec
                    > idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
              [CTE::fixup_po_nets]: (I) PO net 'N56' doesn't match PO 'iu_srlz_op_encode(6)' -> attempting to rename
                       > idm::locate net -name iu srlz op encode(6) -proto box ...
                        > idm::set_net_name -net __CiType_20_3057fb50 -name iu_srl...
                    > idm::object_name __CiType_17_30a4b5c8
                    > idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_20_3057fb28
          [CTE::fixup_po_nets]: (I) PO net 'N58' doesn't match PO 'iu_srlz_op_encode(7)' -> attempting to rename
              > idm::locate_net -name iu_srlz_op_encode(7) -proto_box __...
> idm::set_net_name -net __CiType_20_3057fb28 -name iu_srl...
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580

> idm::object_name __CiType_20_3057fb00
[CTE::fixup_po_nets]: (I) PO net 'N60' doesn't match PO 'iu_srlz_op_encode(8)' -> attempting to rename
                   > idm::set_net_name -net__CiType_20_3057fb00 -name iu_srl...
                    > idm::object_name __CiType_17_30a4b55c
                    > idm::get_net_from_proto_pin __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
              [CTE::fixup_po_nets]: (I) PO net 'N62' doesn't match PO 'iu_srlz_op_encode(9)' -> attempting to rename
                       > idm::locate_net -name iu_srlz_op_encode(9) -proto_box___...
                        > idm::set_net_name -net __CiType_20_3057fad8 -name iu_srl...
                    > idm::object_name __CiType_17_30a4b538
                    > idm::get_net_from_proto_pin __CiType_17_30a4b538
> idm::object_name __CiType_20_3057fab0
              [CTE::fixup_po_nets]: (I) PO net 'N64' doesn't match PO 'iu_srlz_op_encode(10)' -> attempting to rename
                       > idm::locate_net -name iu_srlz_op_encode(10) -proto_box _...
                        > idm::set_net_name -net __CiType_20_3057fab0 -name iu_srl...
                    > idm::object_name __CiType_17_30a4b514
                    > idm::get_net_from_proto_pin __CiType_17_30a4b514
                      > idm::object_name __CiType_20_3057fa88
              [CTE::fixup_po_nets]: (I) PO net 'N66' doesn't match PO 'iu_srlz_op_encode(11)' -> attempting to rename
                       > idm::locate_net -name iu_srlz_op_encode(11) -proto_box _...
                        > idm::set_net_name -net __CiType_20_3057fa88 -name iu_srl...
                     > idm::object_name __CiType_17_30a4b4f0
                    > idm::get_net_from_proto_pin __CiType_17_30a4b4f0
                      > idm::object_name __CiType_20_3057f9e8
              [CTE::fixup_po_nets]: (I) PO net 'N90' doesn't match PO 'decode_ilc(0)' -> attempting to rename
                       > idm::locate_net -name decode_ilc(0) -proto_box __CiType_...
```

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> idm::set_net_name -net __CiType_20_3057f9e8 -name decode...
     > idm::object_name __CiType_17_30a4b4cc
     > idm::get_net_from_proto_pin __CiType_17_30a4b4cc
      > idm::object_name __CiType_20_3057f9c0
[CTE::fixup_po_nets]: (I) PO net 'N92' doesn't match PO 'decode_ilc(1)' -> attempting to rename
        > idm::locate_net -name decode_ilc(1) -proto_box __CiType_...
         > idm::set_net_name -net __CiType_20_3057f9c0 -name decode...
     > idm::object_name __CiType_17_30a4b4a8
     > idm::get_net_from_proto_pin __CiType_17_30a4b4a8
      > idm::object_name __CiType_20_3057fd08
[CTE::fixup_po_nets]: (I) PO net 'N30' doesn't match PO 'srlz_actn_tr(0)' -> attempting to rename
        > idm::locate_net -name srlz_actn_tr(0) -proto_box __CiTyp...
         > idm::set_net_name -net __CiType_20_3057fd08 -name srlz_a...
      > idm::object_name __CiType_17_30a4b484
      > idm::get_net_from_proto_pin __CiType_17_30a4b484
       > idm::object_name __CiType_20_3057fce0
[CTE::fixup_po_nets]: (I) PO net 'N32' doesn't match PO 'srlz_actn_tr(1)' -> attempting to rename
        > idm::locate_net -name srlz_actn_tr(1) -proto_box __CiTyp...
         > idm::set_net_name -net __CiType_20_3057fce0 -name srlz_a...
      > idm::object_name __CiType_17_30a4b460
      > idm::get_net_from_proto_pin __CiType_17_30a4b460
       > idm::object_name __CiType_20_3057f5d8
[CTE::fixup_po_nets]: (I) PO net 'N104' doesn't match PO 'intrpt_info_tr(0)' -> attempting to rename
        > idm::locate_net -name intrpt_info_tr(0) -proto_box __CiT...
> idm::set_net_name -net __CiType_20_3057f5d8 -name intrpt...
     > idm::object_name __CiType_17_30a4b43c
     > idm::get_net_from_proto_pin __CiType_17_30a4b43c
       > idm::object_name __CiType_20_3057f5b0
[CTE::fixup_po_nets]: (I) PO net 'N106' doesn't match PO 'intrpt_info_tr(1)' -> attempting to rename
> idm::locate_net -name intrpt_info_tr(1) -proto_box __CiT...
         > idm::iocate_net_name -net __CiType_20_3057f5b0 -name intrpt...
      > idm::object_name __CiType_17_30a4b418
      > idm::get_net_from_proto_pin __CiType_17_30a4b418
       > idm::object_name __CiType_20_3057f588
[CTE::fixup_po_nets]: (I) PO net 'N108' doesn't match PO 'intrpt_info_tr(2)' -> attempting to rename
        > idm::locate_net -name intrpt_info_tr(2) -proto_box __CiT...
         > idm::set_net_name -net __CiType_20_3057f588 -name intrpt...
      > idm::object_name __CiType_17_30a4b3f4
      > idm::get_net_from_proto_pin __CiType_17_30a4b3f4
       > idm::object_name __CiType_20_3057f560
[CTE::fixup_po_nets]: (I) PO net 'N110' doesn't match PO 'intrpt_info_tr(3)' -> attempting to rename
        > idm::locate_net -name intrpt_info_tr(3) -proto_box __CiT...
         > idm::set_net_name -net __CiType_20_3057f560 -name intrpt...
      > idm::object_name __CiType_17_30a4b3d0
      > idm::get_net_from_proto_pin __CiType_17_30a4b3d0
       > idm::object_name __CiType_20_3057f718
[CTE::fixup_po_nets]: (I) PO net 'N154' doesn't match PO 'op_44_info_tr(0)' -> attempting to rename
        > idm::locate_net -name op_44_info_tr(0) -proto_box __CiTy...
         > idm::set_net_name -net __CiType_20_3057f718 -name op_44_...
      > idm::object_name __CiType_17_30a4b3ac
      > idm::get_net_from_proto_pin __CiType_17_30a4b3ac
       > idm::object_name __CiType_20_3057f6f0
[CTE::fixup_po_nets]: (I) PO net 'N156' doesn't match PO 'op_44_info_tr(1)' -> attempting to rename
         > idm::locate_net -name op_44_info_tr(1) -proto_box __CiTy...
          > idm::set net_name -net __CiType_20_3057f6f0 -name op_44_...
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> idm::object_name __CiType_17_30a4b364
      > idm::get_net_from_proto_pin __CiType_17_30a4b364
       > idm::object_name __CiType_20_3057f768
 [CTE::fixup_po_nets]: (I) PO net 'N148' doesn't match PO 'dcd_c_cnt(0)' -> attempting to rename
        > idm::locate_net -name dcd_c_cnt(0) -proto_box __CiType_1...
         > idm::set_net_name -net __CiType 20 3057f768 -name dcd c ...
      > idm::object_name __CiType 17 30a4b340
      > idm::get_net_from_proto_pin __CiType_17_30a4b340
       > idm::object_name __CiType_20_3057f740
 [CTE::fixup_po_nets]: (I) PO net 'N150' doesn't match PO 'dcd_c_cnt(1)' -> attempting to rename
        > idm::locate_net -name dcd_c_cnt(1) -proto_box __CiType_1...
         > idm::set_net_name -net __CiType_20_3057f740 -name dcd c ...
   > write_end_point_report -points 2
 [ET-0018]: >Begin...New EndPoint Report
        for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.
 Sun Apr 18 22:09:42 1999
 Part: IDCDSUC
 Mode: Late Mode / Nominal
                                     EDA EinsTimer EndPoint Report
 Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
 Min. Slack: -1.13427E+38
                                  Max. Slack: 1.13427E+38
                               Max. Endpoints: 2
 Sort Field: Slack
 Cause of Slack Abbreviation Comparison/Description
                                   Slack due to a point downstream on path
                       SIkCont Slack due to a point downstream on path
RAT (ARRIVAL TIME < REQUIRED ARRIVAL TIME)
  Slack Continuation
 Required Arrival Time
 Asserted Required Arrival Time AssrtRAT (ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 TIME)
Clock Gating Setup
                         ClkGSet (DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
 ARRIVAL TIME + ADJUST )
 Clock Gating Hold
                     CIKGHID (DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 ARRIVAL TIME + ADJUST )
  Clock Tree Pulse Width ClkTPW ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE )
  Setup
                              ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
                    Setup
 ADJUST)
  Hold ----
                    Hold
                             ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
 ADJUST)
  EndOfCycle
                       EndOfC
                                  ( DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
 ADJUST)
 ClockPulseWidth
                         ClkPW
                                   ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
 TRAILING EDGE)
  ClockSeparation
                        ClkSep
                                   ( CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
 ARRIVAL TIME + ADJUST )
 Loop
                              ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
                    ALTest
 CLOCK + ADJUST )
  Arrival Time Limiting
                                   Slack discontinuity due to failed test
                        ATLimit
  Num/
                                  LimitedAT/
                                                                    Delay/ Failed Test/
  Test PinName
                                  E Phase
                                             AT Slack Slew CL FO Cell
                                                                            P Func T.Adi
 NetName
```

dcd_succ_last_t1 RAT	999 0	
> BOX714/OUT	R C3+R 2668 -1669 3294 1011 1 IOPAD	IOPAD
0 dcd_succ_last_t1		
> BOX714/IN	R C3+R 2668 -1669 3294 1011 1 IOPAD	IOPAD
0 dcd_succ_last_t1&0		
> C167/y	R C3+R 2668 -1669 3294 1011 1 cs_invvv 0	11c NOT
0 dcd_succ_last_t1&0		
> C167/a	F C3+R 1075 -1669 27 139 4 cs_invvv 010	C NOT .
1594 N675		
>{a} C2738/y	F C3+R 1075 -1669 27 139 4 cs_nnd2x	14b NAND
0 N675		
> C2738/a	R C3+R 1056 -1669 33 114 1 cs_nnd2x 1	4b NAND
19 last_cycle		4.4 - NIANID
>{b} C2487/y	R C3+R 1056 -1669 33 114 1 cs_nnd2x	14e NAND
0 last_cycle	5 00 D 4005 4000 00 445 0	4 - NIANID
> C2487/a	F C3+R 1035 -1669 22 145 3 cs_nnd2x 1	4e NAND
21 N1587	F.O.D. 4005 4000 00 445 0 an impact 40	b NOT 0
> C1952/y	F C3+R 1035 -1669 22 145 3 cs_invvv 19	DINOI U
	R C3+R 1024 -1669 80 319 1 cs_invvv 19	Sh NOT
	N C3+N 1024 -1009 60 319 1 C5_IIIVVV 18	JUNOI -
11 num_dcd_cyl&0(1)	R C3+R 1024 -1669 80 319 1 IOPAD	IOPAD -
0-num dod cyll 0/1)	1 COTI 1024 1009 00 019 1101 / ID	
0 num_dcd_cyl&0(1)> BOX679/IN	R C3+R 1024 -1669 80 319 1 IOPAD	IOPAD 0
num ded cyl(1)		
num ded cvl(1)	R C3+R 1024 -1669 80 319 1 PI	0
num_dcd_cyl(1)	the contract of the state of the contract of t	

2399 -1400 3318 1011 1 PO R.C3+R 2 iu\_reset\_op\_c\_t1 iu\_reset\_op\_c\_t1 999 RAT -2399 -1400 3318 1011 1 IOPAD **IOPAD** RC3+R ----> BOX716/OUT 0 iu\_reset\_op\_c\_t1 2399 -1400 3318 1044 3 IOPAD **IOPAD** RC3+R ----> BOX716/IN 0 iu\_reset\_op\_c\_t1&0 2399 -1400 3318 1044 3 cs\_nnd2v 02c NAND RC3+R ---->{a} C2393/y 0 iu\_reset\_op\_c\_t1&0 FC3+R 536 -1400 100 196 6 cs\_nnd2v 02c NAND ----> C2393/a 1863 gbfonet\_6 196 6 cs\_invvv 09c NOT FC3+R 536 -1400 100 ----> gbfocell\_6/y 0 gbfonet\_6 R C3+R 472 -1400 184 44 1 cs\_invvv 09c NOT ----> gbfocell\_6/a 64 N2031 44 1 cs\_nnd3v 02c NAND RC3+R 472 -1400 184 ---->{b} C2162/v 0 N2031 144 217 5 cs\_nnd3v 02c NAND FC3+R 358 -1400 ----> C2162/a 114 rcvry\_reset\_q 144 217 5 cl\_invvn 07d ----> rcvry\_reset.reg\_n.lat\_0/l2\_out\_n FC3+R 358 -1400 SRL 0 rcvry\_reset\_q 60 222 13 cl\_invvn 07d SRL R C3+ 160 N/C ----> rcvry\_reset.reg\_n.lat\_0/c2 198 slow\_mode.c2\_1 R C3+ 160 N/C 60 222 13 cb\_clk\_32\_1 LCB ----> slow\_mode.clockblock/c2 0 slow\_mode.c2\_1

```
> load_xrule -file /afs/apd/func/vlsi/alliance00/bscc8/pro...
[BD-450042]: Reading XRULE file '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule'
[BD-450041]: File '/afs/apd/func/vlsi/alliance00/bscc8/prod/xrule/bscc8.xrule' is being read under VIEW
'XPANDVIEW'
[BD-450037]: (E) (Line 3) Macro proto (M record) of name 'cs_buffe01a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 6) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 9) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 13) Macro proto (M record) of name 'cs_buffe02a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 16) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 19) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 23) Macro proto (M record) of name 'cs_buffe03a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 26) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 29) No currently active macro box (M Record), X Record ignored.
[BD-450037]: (E) (Line 33) Macro proto (M record) of name 'cs_buffe04a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 36) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 39) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 43) Macro proto (M record) of name 'cs_buffe05a' with view " already exists. M
record ignored.
[BD-450036]: (E) (Line 46) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 49) No currently active macro box (M Record). X Record ignored.
[BD-450037]: (E) (Line 53) Macro proto (M record) of name 'cs_buffe06a' with view " already exists. M
[BD-450036]: (E) (Line 56) No currently active macro box (M Record). X Record ignored.
[BD-450036]: (E) (Line 59) No currently active macro box (M Record). X Record ignored.
    > nextbox synexpand(XPANDVIEW)
>>]: nextbox( synexpand(XPANDVIEW) );
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 1129 signals, 906 usage boxes and 1744 connections.
>>]: nextbox( SASname(PROTECT) );
[synsasname]: Protected 180 BRKPT net names
[synsasname]: Protected 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[synexpand]: expanded 0 boxes
  > checkfan
Electrical Violations in Network 'IDCDSUC'
                                                  Capacitance
                                                                        Slew
                                                                                          Sink
Fanout
Pin/Port
                         -> Net
                                                    Limit / AdjLim / Actual Limit / AdjLim / Actual
Limit / AdjLim / Actual
eu_iu_enter_slow_md
                                -> eu_iu_enter_slow_md
                                                                  141.00 / 141.00 / 16.73 290.00
```

```
/ 290.00 / 352.00 * 12 / 12 / 1 1
                                                   141.00 / 141.00 / 159.72 * 290.00 /
                        -> op_inq_stores
op ing_stores
                       12/ 3 1
290.00 / 112.00
                                                       141.00 / 141.00 / 32.56 290.00 /
                          -> eu iu_mmode
eu iu_mmode
290.00 / 326.00 *
                  12/
                        12/ 2 1
                                                        141.00 / 141.00 / 141.99 * 290.00
                           -> du iu hold_aa_req
du_iu_hold_aa_req
                        12/ 2 1
/ 290.00 / 424.00 *
                   12/
                                                        141.00 / 141.00 / 30.80 290.00 /
                           -> eu_iu_fpu_end_op
eu iu fpu end_op
                        12 / 1 1
290.00 / 339.00 *
                  12/
                                                       141.00 / 141.00 / 19.15 290.00 /
eu iu misc_hold
                          -> eu_iu_misc_hold
290.00 / 332.00 *
                  12/
                        12 / 1 1
                                                       141.00 / 141.00 / 144.35 * 290.00 /
                          -> op_mcend_raw
op_mcend_raw
                 12/ 12/ 3 1
290.00 / 91.00
                                             141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                     -> clkq
clkg
         12/
60.00
               12/ 3 1
                         -> du_iu_quiesced
                                                      141.00 / 141.00 / 20.50
                                                                              290.00 /
du iu_quiesced
290.00 / 338.00 *
                  12/
                       12 / 1 1
                                                 141.00 / 141.00 / 170.11 * 290.00 / 290.00
                       -> iq_empty
iq empty
           12/ 12/
                       4 1
/ 116.00
                                                   141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                        -> gptr_scan_in
gptr_scan_in
     12/ 12/ 1
0.00
                                                 141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
gptr_a_clk
                       -> gptr_a_clk
       12/ 12/
0.00
                    1 1
                                                 141.00 / 141.00 / 1011.00 * -0.00 / 0.00 /
gptr_b_clk
                       -> gptr_b_clk
0.00 12/ 12/ 1 1
                                   141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                     -> clkq2
clkg2
-60:00::--- 12 / 12 / 3 1
                                                         . 141.00 / :141.00 / 15.67 290.00 - --
eu_iu_fxu_exc_cond-----
                          -> eu_iu_fxu_exc_cond
/ 290.00 / 390.00 * 12 / 12 / 1 1
                                                         141.00 / 141.00 / 16.89 __ 290.00 / __
                         -> du_iu_store_status(2)
du_iu_store_status(2)
                 12/ 12/ 1 1
290.00 / 500.00 *
                                                      141.00 / 141.00 / 47.57 290.00 /
eu_iu_srlz_op_actn(0)
                            -> eu_iu_srlz_op_actn(0)
290.00 / 374.00 * 12 /
                        12/ 2 1
                                                      141.00 / 141.00 / 47.57 290.00 /
eu_iu_srlz_op_actn(1) -> eu_iu_srlz_op_actn(1)
                        12/ 2 1
290.00 / 341.00 * 12 /
                                                       141.00 / 141.00 / 318.91 * 290.00 /
num dcd_cyl(1)
                          -> num_dcd_cyl(1)
                 12/ 12/ 1 1
290.00 / 80.00
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(0)
eu_iu_srlz_op_encode(0)
290.00 / 290.00 / 401.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
eu iu srlz op encode(1)
                             -> eu_iu_srlz_op_encode(1)
290.00 / 290.00 / 400.00 *
                           12 / 12 / 1 1
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(2)
eu iu_srlz_op_encode(2)
290.00 / 290.00 / 420.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(3)
                             -> eu iu_srlz_op_encode(3)
                           12/ 12/ 1 1
290.00 / 290.00 / 302.00 *
                                                             141.00 / 141.00 / 16.89
 eu iu srlz op encode(4)
                             -> eu_iu_srlz_op_encode(4)
 290.00 / 290.00 / 406.00 1
                           12/ 12/ 1 1
                             -> eu_iu_srlz_op_encode(5)
                                                             141.00 / 141.00 / 16.89
 eu iu srlz op encode(5)
 290.00 / 290.00 / 373.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
 eu_iu_srlz_op_encode(6)
                             -> eu_iu_srlz_op_encode(6)
                           12/ 12/ 1 1
 290.00 / 290.00 / 354.00 *
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(7)
 eu_iu_srlz_op_encode(7)
 290.00 / 290.00 / 398.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
                              -> eu_iu_srlz_op_encode(8)
 eu iu srlz op encode(8)
 290.00 / 290.00 / 367.00 *
                           12 / 12 / 1 1
```

```
eu iu srlz op encode(9)
                             -> eu_iu_srlz_op_encode(9)
                                                             141.00 / 141.00 / 16.89
   290.00 / 290.00 / 323.00 *
                            12/ 12/ 1 1
   eu_iu_srlz_op_encode(11)
                               -> eu_iu_srlz_op_encode(11) 141.00 / 141.00 / 16.89
                            12/ 12/ 1 1
   290.00 / 290.00 / 500.00 *
   c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1
                                                                 78.50 / 78.50 / 220.92 *
   200.00 / 200.00 / 60.00
                           12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
   NO_SERIAL
   c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
                                                                 78.50 / 78.50 / 222.27 *
   200.00 / 200.00 / 60.00
                           12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
   NO SERIAL
   clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
                                                                 78.50 / 78.50 / 212.39 *
  200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
   NO SERIAL
  c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1 2
                                                                 78.50 / 78.50 / 237.92 *
                         12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  200.00 / 200.00 / 60.00
  NO SERIAL
  c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
                                                                 78.50 / 78.50 / 239.36 *
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka 2
                                                                 78.50 / 78.50 / 228.73 *
  200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO PARALLEL
  NO_SERIAL
  c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
                                                                78.50 / 78.50 / 237.92 *
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO SERIAL
  c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3 78.50 / 78.50 / 239.37
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO SERIAL
  clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
  200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO SERIAL
 NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4
                                                                 78.50 / 78.50 / 237.92 *
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO_SERIAL
                                             Capacitance
                                                                Slew
                                                                               Sink
  Fanout
---Pin/Port
                        -> Net
                                              Limit / AdjLim / Actual Limit / AdjLim / Actual
  Limit / AdjLim / Actual
  c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                                 78.50 / 78.50 / 239.36 *
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO_SERIAL
  clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4
                                                                 78.50 / 78.50 / 228.73 *
  200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO SERIAL
  c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
                                                                 78.50 / 78.50 / 237.91 *
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO_SERIAL
  c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5
                                                                 78.50 / 78.50 / 239.37 *
  200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  NO SERIAL
  clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5
                                                                 78.50 / 78.50 / 228.73 *
  200.00 / 200.00 / 198.79
                         12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
  c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1
                                                                78.50 / 78.50 / 237.92 *
```

```
12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
                                                               78.50 / 78.50 / 239.37 *
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2
                       12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
                                                              78.50 / 78.50 / 228.73 *
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                         12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 198.79
NO_SERIAL
                                                         70.00 / 70.00 / 1011.00 * 301.00
                           -> dcd_succ_last_t1&0
y@C167:cs_invvv01c
/ 301.00 / 3294.02 * 12 / 12 / 1 1 KEEP_BTR
                                                     68.00 / 68.00 / 77.40 * 290.00 /
y@C1994:cs_invvn01c
                            -> N1531
290.00 / 286.02
                            2 2
                 12/ 12/
                                                     68.00 / 68.00 / 1011.00 * 301.00 /
v@C2013:cs_invvn01c
                            -> N18&0
301.00 / 3608.92 *
                 12 /
                        12/ 1 1
                            -> N146&0
                                                      68.00 / 68.00 / 1011.00 * 301.00 /
v@C2082:cs_invvn01c
301.00 / 3604.78 * 12 /
                        12/ 1 1
                                                     261.00 / 261.00 / 271.46 * 290.00 /
                            -> N1681
y@C2194:cs_invvn07c
290.00 / 261.53
                 12/ 12/ 7 7
                                                          71.00 / 71.00 / 1044.40 *
                             -> iu_reset_op_c_t1&0
v@C2393:cs_nnd2v02c
290.00 / 290.00 / 3371.12 *
                           12/ 12/ 3 3
                                                     68.00 / 68.00 / 125.56 * 290.00 /
                            -> N1815
v@C2425:cs invvn01c
290.00 / 451.90 * 12 /
                       12 /
                            1 1
                                                      85.00 - / 85.00 - / 97.67 * 290.00 /
                             -> N1435 --- ---
v@C2496:cs_nnd4n03c
290.00 / 353.82 *
                 12/ 12/ 5 5
                                                     133.00 / 133.00 / 150.69 * 290.00 /-
                       -> N1645
v@C2646:cs invvn04c
290.00 / 275.60 - 12 / 12 / 6 6
500.00 / 500.00 / 540.60 - *-
                          12/ 12/ 2 2
290.00 / 290.00 / 258.01
                                                      996.00 /-996.00 / 1081.45 * 290.00
y@C2744:cs_invvn13c
                            -> N2086&0
                   12/-- 12/-- 7--7
/ 290.00 / 271.62
                                                     326.00 / 326.00 / 234.15
                                                                              290.00 /
y@C2800:cs_invvn08c
                            -> N1290
                       12/ 14*14
290.00 / 193.42
                 12/
                                                      167.00 / 167.00 / 183.47 * 290.00 /
v@C2728rwr:cs invvn05c
                             -> N1097
                             4 4
290.00 / 266.58
                  12/
                       12/
                                                      110.00 / 110.00 / 132.34 * 290.00 /
y@C2918:cs_nor2n04c
                             -> N2016
290.00 / 428.15 * 12 / 12 /
                            1 1
                                                      797.00 / 797.00 / 402.55
                                                                               290.00 /
y@gbfocell_0:cs_invvn12c_
                             -> gbfonet_0
                       12 / 20 * 20
290.00 / 149.98
                 12/
                                                           247.00 / 247.00 / 301.71 *
I2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
290.00 / 290.00 / 242.45
                          12/ 12/
[BD-500900]: (W) There were 64 electrical violations.
  > checkfan
Electrical Violations in Network 'IDCDSUC'
                                            Capacitance
                                                               Slew
                                                                              Sink
Fanout
                                             Limit / AdjLim / Actual Limit / AdjLim / Actual
Pin/Port
                      -> Net
Limit / AdjLim / Actual
```

-> eu iu enter\_slow\_md

-> op ing stores

-> eu\_iu\_mmode

12/ 12/ 3 1

eu\_iu\_enter\_slow\_md

op\_inq\_stores 290.00 / 112.00

eu\_iu\_mmode

/ 290.00 / 352.00 \* 12 / 12 / 1 1

141.00 / 141.00 / 16.73 290.00

141.00 / 141.00 / 159.72 \* 290.00 /

141.00 / 141.00 / 32.56 290.00 /

```
290.00 / 326.00 * 12 / 12 / 2 1
du_iu_hold_aa req
                          -> du_iu hold aa reg
                                                     141.00 / 141.00 / 141.99 * 290.00
/ 290.00 / 424.00 *
                   12/
                       12/ 2 1
eu_iu_fpu_end_op
                          -> eu_iu_fpu_end_op
                                                       141.00 / 141.00 / 30.80
                                                                              290.00 /
290.00 / 339.00 *
                  12/
                       12 / 1 1
eu_iu_misc_hold
                         -> eu_iu_misc_hold
                                                    141.00 / 141.00 / 19.15 290.00 /
290.00 / 332.00 *
                  12/
                       12 / 1 1
op_mcend_raw
                          -> op mcend raw
                                                      141.00 / 141.00 / 144.35 * 290.00 /
290.00 / 91.00
                12/ 12/ 3 1
clkg
                    -> clkg
                                           141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00
         12/
              12/ 3 1
du_iu_quiesced
                        -> du_iu_quiesced
                                                    141.00 / 141.00 / 20.50 290.00 /
290:00 / 338.00 *
                  12/
                       12 / 1 1
iq_empty
                      -> iq_empty
                                               141.00 / 141.00 / 170.11 * 290.00 / 290.00
/ 116.00
           12/
                12/
                      4 1
gptr_scan_in
                       -> gptr_scan_in
                                                141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00
       12/
             12/
gptr_a_clk
                      -> gptr a clk
                                               141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
       12 /
             12 / 1 1
0.00
gptr_b_clk
                      -> gptr_b_clk
                                               141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 - 12/ 12/ 1 1
                                            141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
clkq2
                     -> clka2
60.00 12 / 12 / 3 1
                                                     141.00 / 141.00 / 15.67 290.00
eu_iu_fxu_exc_cond
                          -> eu_iu_fxu_exc_cond
/ 290.00 / 390.00 * 12 / 12 / 1...1
du_iu_store_status(2) -> du_iu_store_status(2)
                                                       141.00 / 141.00 / 16.89 - 290.00 /
290.00 / 500.00 * 12 / 12 / 1 1
eu_iu_srlz_op_actn(0) -> eu_iu_srlz_op_actn(0)
                                                    141.00 / 141.00 / 47.57 290.00 /
290.00 / 374.00 * 12 /-- 12 / 2 1
                       -> eu_iu_srlz_op_actn(1) 141.00 / 141.00 / 47.57 290.00 /
eu_iu_srlz_op_actn(1)
290.00 / 341.00 * 12 / 12 / 2 1
num_dcd_cyl(1)
                   -> num_dcd_cyl(1) 141.00 / 141.00 / 318.91 * 290.00 /
290.00 / 80.00 12 / 12 / 1 1
eu_iu_srlz_op_encode(0)
                            -> eu_iu_srlz_op_encode(0) 141.00 / 141.00 / 16.89
290.00 / 290.00 / 401.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(1)
                           -> eu_iu_srlz_op_encode(1)
                                                        141.00 / 141.00 / 16.89
290.00 / 290.00 / 400.00 *
                          12 / 12 / 1 1
eu iu srlz op encode(2)
                            -> eu_iu_srlz_op_encode(2) 141.00 / 141.00 / 16.89
290.00 / 290.00 / 420.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(3)
                            -> eu_iu_srlz_op_encode(3)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(4)
                            -> eu_iu_srlz_op_encode(4)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 406.00 *
                          12 / 12 / 1 1
eu_iu_srlz_op_encode(5)
                            -> eu_iu_srlz_op_encode(5)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 373.00 *
                          12 / 12 / 1 1
eu_iu srlz op encode(6)
                           -> eu_iu_srlz_op_encode(6)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 354.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(7)
                            -> eu_iu_srlz_op_encode(7)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 398.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(8)
                           -> eu_iu_srlz_op_encode(8)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 367.00 1
                          12 / 12 / 1 1
eu_iu_srlz_op_encode(9)
                            -> eu_iu_srlz_op_encode(9)
                                                           141.00 / 141.00 / 16.89
290.00 / 290.00 / 323.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(11)
                            -> eu_iu_srlz_op_encode(11)
                                                          141.00 / 141.00 / 16.89
290.00 / 290.00 / 500.00 *
                          12/ 12/ 1 1
```

```
78.50 / 78.50 / 220.92 *
         c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1
         200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO_SERIAL
         c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
                                                                   78.50 / 78.50 / 222.27 *
         200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 212.39 *
         clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
         200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 237.92 *
         c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
         200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO_SERIAL
                                                                   78.50 / 78.50 / 239.36 *
         c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
         200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 228.73 *
         cika@slow_mode.clockblock_1:cb_cik_3 -> slow_mode.clka_2
         200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 237.92 *
         c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
        200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 239.37 *
       ... c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3
       200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
       NO SERIAL
      clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73
 200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC.NO_PARALLEL
      NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4
   NO_SERIAL
                                                                   78.50 / 78.50 / 237.92 *--
        200.00 / 200.00 / 60.00 ... 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
            - Capacitance Slew Sink
         Fanout
                                                Limit / AdjLim / Actual Limit / AdjLim / Actual
         Pin/Port
                            -> Net
         Limit / AdjLim / Actual
                                                                   78.50 / 78.50 / 239.36 *
         c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
         200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 228.73 *
         clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4
         200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO_SERIAL
                                                                    78.50 / 78.50 / 237.91 *
         c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
         200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                    78.50 / 78.50 / 239.37 *
         c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5
         200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
         NO SERIAL
                                                                   78.50 / 78.50 / 228.73 *
         clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka_5
         200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO_SERIAL
          c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1
                                                                   78.50 / 78.50 / 237.92 *
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
          NO SERIAL
                                                                   78.50 / 78.50 / 239.37 *
          c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2
          200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
```

```
NO SERIAL
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                                                               78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
v@C167:cs invvv01c
                            -> dcd_succ_last_t1&0
                                                         70.00 / 70.00 / 1011.00 * 301.00
/ 301.00 / 3294.02 * 12 / 12 / 1 1 KEEP_BTR
y@C1994:cs_invvn01c
                             -> N1531
                                                     68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02
                 12/ 12/ 2 2
y@C2013:cs_invvn01c
                            -> N18&0
                                                      68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3608.92 * 12 /
                         12 / 1 1
y@C2082:cs_invvn01c
                            -> N146&0
                                                      68.00 / 68.00 / 1011.00 * 301.00 /
301.00 / 3604.78 * 12 /
                        12 / 1 1
v@C2194:cs invvn07c
                            -> N1681
                                                     261.00 / 261.00 / 271.46 * 290.00 /
290.00 / 261.53
                12/ 12/ 7 7
y@C2393:cs_nnd2v02c
                             -> iu_reset_op_c_t1&0
                                                          71.00 / 71.00 / 1044.40 *
290.00 / 290.00 / 3371.12 *
                           12/ 12/ 3 3
y@C2425:cs_invvn01c
                            -> N1815
                                                     68.00 / 68.00 / 125.56 * 290.00 /
290.00 / 451.90 * 12 /
                       12/ 1 1
y@C2496:cs_nnd4n03c
                             -> N1435
                                                      85.00 / 85.00 / 97.67 * 290.00 /
290.00 / 353.82 * 12 /
                       12/ 5 5
y@C2646:cs_invvn04c
                            -> N1645
                                                    133.00 / 133.00 / 150.69 * 290.00 /
                 12/ 12/ 6 6
290.00 / 275.60
                      -> dsucc_or_agi&0
y@C2726:cs nnd2n11c
                                                        500.00 / 500.00 / 540.60 *
290.00 / 290.00 / 258.01 12 / 12 / 2 2
v@C2744:cs invvn13c
                          -> N2086&0
                                                      996.00 / 996.00 / 1081.45 * 290.00
/ 290.00 / 271.62
                  12/ 12/ 7 7
                       -> N1290
y@C2800:cs invvn08c
                                             326.00 / 326.00 / 234.15 | 290.00 / 3
                 8c -> N1290
12 / 12 / 14 * 14
290.00 / 193.42
v@C2728rwr:cs_invvn05c
                                                   167.00 / 167.00 / 183.47 * 290.00 /
                      -> N1097
290.00 / 266.58 12 /
v@C2918:cs nor2n04c
                        -> N2016
                                           110.00 / 110.00 / 132.34 * 290.00 /
290.00 / 428.15 * 12 / 12 / 1 1
y@gbfocell_0:cs_invvn12c
                            -> gbfonet_0
                                                      797.00 / 797.00 / 402.55 290.00 /
290.00 / 149.98
                 12 / 12 / 20 * 20
l2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
                                                           247.00 / 247.00 / 301.71 *
290.00 / 290.00 / 242.45
                          12/
                              12/88
[BD-500900]: (W) There were 64 electrical violations.
  > nextbox fastslew
>>]: nextbox( fastslew );
[BD-500000]: fastslew CMVC version 1.9 compiled on Apr 13 1999 at 18:30:51
[BD-501600]: 7 gates repowered.
 > checkfan
Electrical Violations in Network 'IDCDSUC'
                                           Capacitance
                                                               Slew
                                                                              Sink
Fanout
Pin/Port
                     -> Net
                                             Limit / AdjLim / Actual Limit / AdjLim / Actual
Limit / AdiLim / Actual
eu_iu_enter_slow_md
                           -> eu_iu_enter_slow_md
                                                          141.00 / 141.00 / 16.73 290.00
/ 290.00 / 352.00 * 12 / 12 / 1 1
op ing stores
                        -> op_inq_stores
                                                  141.00 / 141.00 / 159.72 * 290.00 /
```

290.00 / 112.00

12/ 12/ 3 1

```
141.00 / 141.00 / 32.56 290.00 /
                          -> eu iu mmode
eu iu mmode
                  12/ 12/ 2 1
290.00 / 326.00 *
                           -> du_iu_hold_aa_req
                                                        141.00 / 141.00 / 141.99 * 290.00
du iu_hold_aa_req
/ 290.00 / 424.00 *
                    12/ 12/ 2 1
                                                        141.00 / 141.00 / 30.80
                                                                                290.00 /
                           -> eu_iu_fpu_end_op
eu_iu_fpu_end_op
                       12/ 1 1
290.00 / 339.00 *
                  12/
                                                       141.00 / 141.00 / 19.15 290.00 /
                          -> eu_iu_misc_hold
eu_iu_misc_hold
290.00 / 332.00 *
                        12/ 1 1
                                                       141.00 / 141.00 / 144.35 * 290.00 /
op mcend_raw
                          -> op_mcend_raw
                 12/ 12/ 3 1
290.00 / 91.00
                                             141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                     -> clka
clkg
              12/
                    3 1
60.00
         12/
                                                      141.00 / 141.00 / 20.50 290.00 /
du_iu_quiesced
                          -> du_iu_quiesced
290.00 / 338.00 *
                  12/
                       12 / 1 1
                                                 141.00 / 141.00 / 170.11 * 290.00 / 290.00
                       -> iq_empty
iq_empty
/116.00
           12/
               12/
                                                   141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                        -> gptr_scan_in
gptr_scan_in
             12/
       12/
0.00
                                                 141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
                       -> gptr_a_clk
gptr_a_clk
       12/
             12/
0.00
                                                141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
aptr_b_clk
                       -> gptr_b_clk
             12/
       12 / 12
0.00
                                  141.<del>00 / 14</del>1.00 / 145.52 * 100.00 / 100.00 /
                     -> clka2
clkg2
141.00 / 141.00 / 15.67
                                                                                 -290.00
                           -> eu_iu_fxu_exc_cond
/ 290.00 / 390.00 * 12./ 12./ 1 1
                                                         141.00 / 141.00 / 16.89
                                                                                 290.00 /
du_iu_store_status(2) -> du_iu_store_status(2)
290.00 / 500.00 * 12 / 12 / 1 1 - - -
                                                       141.00 / 141.00 / 47.57
                                                                                 290.00 /
eu_iu_srlz_op_actn(0) -> eu_iu_srlz_op_actn(0)
290.00 / 374.00 * 12 / 12 / 2 1
                                                         141.00 / 141.00 / 47.57
                                                                                  290.00 /
                           -> eu_iu_srlz_op_actn(1)
eu iu srlz_op_actn(1)
290.00 / 341.00 * 12 /
                        12/ 2 1
                                                      141.00 / 141.00 / 318.91 * 290.00 /
                          -> num_dcd_cyl(1)
num dcd cvl(1)
290.00 / 80.00
                 12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(0)
                             -> eu_iu_srlz_op_encode(0)
290.00 / 290.00 / 401.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(1)
eu iu srlz op encode(1)
                           12 / 12 / 1 1
290.00 / 290.00 / 400.00 *
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(2)
eu_iu_srlz_op_encode(2)
                           12/ 12/ 1 1
290.00 / 290.00 / 420.00 *
                                                             141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(3)
                             -> eu_iu_srlz_op_encode(3)
                           12/ 12/ 1 1
290.00 / 290.00 / 302.00 *
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(4)
eu_iu_srlz_op_encode(4)
290.00 / 290.00 / 406.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
eu iu srlz op_encode(5)
                             -> eu_iu_srlz_op_encode(5)
290.00 / 290.00 / 373.00 *
                           12 / 12 / 1 1
                                                             141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(6)
eu_iu_srlz_op_encode(6)
                           12/ 12/ 1 1
290.00 / 290.00 / 354.00 *
                                                             141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(7)
                             -> eu_iu_srlz_op_encode(7)
290.00 / 290.00 / 398.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(8)
                             -> eu_iu_srlz_op_encode(8)
290.00 / 290.00 / 367.00 *
                           12/ 12/ 1 1
                             -> eu_iu_srlz_op_encode(9)
                                                             141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(9)
290.00 / 290.00 / 323.00 *
                           12/ 12/ 1 1
                                                             141.00 / 141.00 / 16.89
                              -> eu_iu_srlz_op_encode(11)
eu_iu_srlz_op_encode(11)
```

```
290.00 / 290.00 / 500.00 * 12 / 12 / 1 1
        c1@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1 78.50 / 78.50 / 220.92 *
        200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO_SERIAL
        c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
                                                                   78.50 / 78.50 / 222.27 *
        200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO_SERIAL
        clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
                                                                   78.50 / 78.50 / 212.39 *
        200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO SERIAL
        c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
                                                                    78.50 / 78.50 / 237.92 *
        200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO PARALLEL
        NO-SERIAL
        c2@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
                                                                    78.50 / 78.50 / 239.36 *
        200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO_SERIAL
        clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2
                                                                    78.50 / 78.50 / 228.73 *
        200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
                                                                   78.50 / 78.50 / 237.92 *
       200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO_SERIAL
       c2@slow_mode.clockblock_2:cb_clk_32_-> slow_mode.c2_3 78.50 / 78.50 / 239.37 *
       200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO SERIAL
       clka@slow_mode.clockblock_2:cb_clk_3 -> slow_mode.clka_3 78.50 / 78.50 / 228.73 *
       200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c1_4
                                                                    78.50 / 78.50 / 237.92 *
   200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
                                                               Slew
                                                Capacitance
       Fanout
                            -> Net
        Pin/Port
                                                  Limit / AdjLim / Actual Limit / AdjLim / Actual
       Limit / AdjLim / Actual
       c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                                    78.50 / 78.50 / 239.36 *
        200.00 / 200.00 / 60.00 -- 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka 4
                                                                   78.50 / 78.50 / 228.73 *
        200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO PARALLEL
       NO SERIAL
       c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
                                                                   78.50 / 78.50 / 237.91 *
       200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
       NO_SERIAL
        c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5
                                                                   78.50 / 78.50 / 239.37 *
       200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
       NO SERIAL
        clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka 5
                                                                   78.50 / 78.50 / 228.73 *
        200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO SERIAL
       c1@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c1
                                                                   78.50 / 78.50 / 237.92 *
       200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
        NO SERIAL
       c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2
                                                                  78.50 / 78.50 / 239.37 *
```

```
12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
                                                               78.50 / 78.50 / 228.73 *
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                          12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 198.79
NO_SERIAL
                            -> dcd_succ_last_t1&0
                                                          638.00 / 638.00 / 1011.00 *
y@C167:cs_invvv11e
301.00 / 301.00 / 300.47
                          12/ 12/ 1 1 KEEP_BTR
                                                      68.00 / 68.00 / 77.40 * 290.00 /
y@C1994:cs_invvn01c
                             -> N1531
                       12/ 2 2
290.00 / 286.02
                  12/
                                                      796.00 / 796.00 / 1011.00 * 301.00 /
                             -> N18&0
v@C2013:cs_invvn12d
301.00 / 279.84
                  12/
                       12/
                            1 1
                                                       796.00 / 796.00 / 1011.00 * 301.00 /
y@C2082:cs_invvn12d
                             -> N146&0
                            1 1
301.00 / 281.78
                 12/
                       12/
                                                      261.00 / 261.00 / 271.46 * 290.00 /
                             -> N1681
y@C2194:cs_invvn07c
290.00 / 261.53
                  12/
                       12 / 7 7
                                                           813.00 / 813.00 / 1044.40 *
y@C2393:cs_nnd2v13d
                             -> iu_reset_op_c_t1&0
290.00 / 290.00 / 267.22
                          12/ 12/
                                     3 3
                                                      133.00 / 133.00 / 150.69 * 290.00 /
y@C2646:cs_invvn04c
                             -> N1645
290.00 / 275.60
                 12 /
                      12/ 6 6
                             -> dsucc_or_agi&0
                                                          500.00 / 500.00 / 540.60 *
y@C2726:cs_nnd2n11c
                          12/ 12/ 2 2
290.00 / 290.00 / 258.01
                             -> N2086&0
                                                       996.00 / 996.00 / 1081.45 * 290.00
y@C2744:cs_invvn13c
/ 290.00 / 269.95 12 /
                         12/ 7 7
                                                     ..326.00 / 326.00 / 234.15 | 290.00 /
                             -> N1290
y@C2800:cs_invvn08c
290.00 / 193.42 12 / 12 / 14 * 14
                             -> N1097
                                                    ___ 167.00 / 167.00 / 183.47 * 290.00 /
y@C2728rwr:cs_invvn05c
290.00 / 266.58 12 / 12 / 4 4
                                                       797.00 / 797.00 / 402.55 - 290.00 /
                             -> gbfonet_0
y@gbfocell_0:cs_invvn12c
247.00 / 247.00 / 301.71
I2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
290.00 / 290.00 / 242.45
                          12/ 12/ 8 8
[BD-500900]: (W) There were 61 electrical violations.
  > write_end_point_report -points 2
[ET-0018]: >Begin...New EndPoint Report
       for file /tmp/end_point_report..92476.
[ET-0019]: <End....New Endpoint Report.
Sun Apr 18 22:09:47 1999
Part: IDCDSUC
                                    EDA EinsTimer EndPoint Report
Mode: Late Mode / Nominal
Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999
Min. Slack: -1.13427E+38
                                 Max. Slack: 1.13427E+38
                              Max. Endpoints: 2
Sort Field: Slack
                       Abbreviation Comparison/Description
 Cause of Slack
                                  Slack due to a point downstream on path
                        SlkCont
 Slack Continuation
                                  ( ARRIVAL TIME < REQUIRED ARRIVAL TIME)
                         RAT
 Required Arrival Time
                                      ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL
 Asserted Required Arrival Time AssrtRAT
TIME)
                                   ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK
                        ClkGSet
 Clock Gating Setup
ARRIVAL TIME + ADJUST )
                        CIKGHId
                                   ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK
 Clock Gating Hold
ARRIVAL TIME + ADJUST )
                                     ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
                          CIKTPW
 Clock Tree Pulse Width
```

	TRAILING EDGE ) Setup Setup	( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME +
	ADJUST) Hold Hold	( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME +
	ADJUST)	
	EndOfCycle EndO ADJUST)	DFC (DATA ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME +
	•	PW (CLOCK LEADING EDGE + PULSE WIDTH < CLOCK
		Sep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2
	Loop ALTest CLOCK + ADJUST )	( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM
		Limit Slack discontinuity due to failed test
	Num/ Test PinName NetName	LimitedAT/ Delay/ Failed Test/ E Phase AT Slack Slew CL FO Cell P Func T.Adj
en e	47 N1013	a F C3+R 1761 -448 88 31 1 cl_invvn 07d SRL
المتي بي او العجم المداد الأستند. الماد الماد ا	Setup eu_dsbl_aftr.reg_n.lat_1200 slow_mode.c1_1	0/c1 F.C3- 160 - 60 221 13 cl_invvn 07d
	>{a} C2856/y	F C3+R 1761 -448 88 31 1 cs_nnd2n 02c NAND
	0 N1013	1 COTTI 1701 -440 00 31 (S_IIIIUZII UZCINAIVI)
	> C2856/b	R C3+R 1699 -448 104 17 1 cs_nnd2n 02c NAND
	62 N522	
المناسب وأنهن الخرا	>{b} C2833/y	R C3+R 1699 -448 104 17 1 cs_nnd2n 02c NAND
	0 N522 > C2833/b	F C3+R 1625 -448 129 234 14 cs_nnd2n 02c NAND
	74 N1290	F C3+H 1025 -446 129 234 14 CS_HIIOZN U2C NAND
-	> C2800/y	F C3+R 1625 -448 129 234 14 cs_invvn 08c NOT
And the second second	0 N1290	and the control of th
	> C2800/a	R C3+R 1533 -448 170 37 1 cs_invvn 08c NOT
	92 N1648	D 00 D 4500 440 470 07 4 10 10 10 10 10 10 10 10 10 10 10 10 10
4 - 4 <b>-</b>	>{c} C2779/y 0 N1648	R C3+R 1533 -448 170 37 1 cs_nnd2n 02c NAND
	> C2779/b	F C3+R 1419 -448 164 151 6 cs_nnd2n 02c NAND
	114 N1645	
	> C2646/y	F C3+R 1419 -448 164 151 6 cs_invvn 04c NOT 0
	N1645 > C2646/a	D.CO. D. 1005 440 440 04 4 as import 04 NOT
	114 N1746	R C3+R 1305 -448 110 21 1 cs_invvn 04c NOT
	>{d} C2620/y	R C3+R 1305 -448 110 21 1 cs_nnd2n 02c NAND
	0 N1746	00111 1000 110 110 E1 1 00_1110E11 02014/114D
	> C2620/a	F C3+R 1230 -448 133 67 4 cs_nnd2n 02c NAND
	75 N1740	
	> C2602/y N1740	F C3+R 1230 -448 133 67 4 cs_invvn 02c NOT 0
	> C2602/a 95 N905	R C3+R 1135 -448 146 37 2 cs_invvn 02c NOT
	>{e} C2546/y	R C3+R 1135 -448 146 37 2 cs_nnd2n 02c NAND
	0 N905 > C2546/a	F C3+R 1045 -448 96 17 1 cs_nnd2n 02c NAND

90 N1647 > C1928/y	F C3+R	1045 -448 9	96 17 1 cs_invvn	01c NOT	0
N1647	1 00111		_		
> C1928/a	R C3+R	988 -448 3	90 16 1 cs_invvn	1 01c NOT	57
eu_iu_fxu_exc_c		R 988 -448	390 16 1 IOPA	AD IOPAD	
> BOX665/C		R 988 -448	390 16 11077	ND IOPAD	
0 eu_iu_fxu_exc > BOX665/II		988 -448	390 16 1 IOPAD	IOPAD	0
eu_iu_fxu_exc_c					
> eu_iu_fxu_		+R 988 -448	8 390 16 1 PI	0	
eu_iu_fxu_exc_c	ond				
	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			,
2 eu_frc_mill 47 N994	i.reg_n.lat_0/a F C3+	R 1761 -448	88 31 1 cl_in	vvn 07d SRL	
Setup eu_frc_m 1200 slow_mode	nilli.reg_n.lat_0/c1	3- 160	60 238 14 cl_in	vvn 07d	
>{a} C2857/y	F C3+R	1761 -448	88 31 1 cs_nnd2	2n 02c NAND	
0 N994		4000 455	104 47 4	0- 00-11415	
> C2857/b	R C3+R	1699 -448 1	104 17 1 cs_nnd2	2n U2C NAND	• •
62 N505	D C2 - D	1600 449	104 17 1 cs_nnd	ION NO NIANID	
>{b} C2834/y 0 N505	H C3+H	1099 -440			
> C2834/h	F C3+R	1625 -448 1	29 234 14 cs nnc	d2n 02c NAND	!
74 N1290		•			1. Table 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.
> C2800/y	F C3+R	1625 -448 1	29 234 14 cs_inv	vn 08c NOT	
0 N1290					
> C2800/a	R C3+R	1533 -448 1	170 37 1 cs_invv	n OBC NOT	
92 N1648 >{c} C2779/y	R C3+R	1533 -448	170 37 1 cs_nnd	l2n 02c NAND	
0 N1648		1410 440 4	ICA 151 6	ion Oon NAND	
> C2779/b	F U3+H	1419 <del>-44</del> 8 1	164 151 6 cs_nnd	ZII UZU INAINU	
114 N1645 > C2646/y	F C3±R	1419 -448 1	64 151 6 cs_invv	n 04c NOT	. 0
N1645	1 GOFIT	, 110 - 170 1	J. 151 0 00_#144		Ţ
> C2646/a	R C3+R	1305 -448 1	110 21 1 cs_invv	n 04c NOT	
114 N1746					
>{d} C2620/y	R C3+R	1305 -448	110 21 1 cs_nnc	J2n 02c NAND	••
0 N1746		4000 440 4	100 07 4	0- 00- NAND	
> C2620/a	F C3+R	1230 -448 1	133 67 4 cs_nnd2	20 UZC NAND	
75 N1740	F C3+R	1230 -448 1	133 67 4 cs_invvi	n O2c NOT	0
> C2602/y N1740	1 00+n	1200 - <del>11</del> 0 1	00 07 4 00_IIIVVI	. 0201101	•
> C2602/a	R C3+R	<b>1135</b> -448 1	146 37 2 cs_invv	n 02c NOT	
95 N905		_	_	•	
>{e} C2546/y	R C3+R	1135 -448	146 37 2 cs_nnc	d2n 02c NAND	!
0 N905					
> C2546/a	F C3+R	1045 -448	96 17 1 cs_nnd2	2n 02c NAND	
90 N1647	E 00: D	1045 440	06 17 1 an insam	NOT	0
> C1928/y	F C3+R	1045 -448	96 17 1 cs_invvn	I OICHOI	J
N1647 > C1928/a	R C3+R	988 -448 3	390 16 1 cs_invvr	n 01c NOT	57
eu_iu_fxu_exc_0		<del>5000</del> 0	,55 10 105_11441	. 0.00.	<del>- ,</del>
		D 000 -440	390 16 1 IOP/	AD IOPAD	
> BOX665/0	JU   1 UST	'n 300 -440	330 10 11017	אוטו ער	

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**IOPAD** 

the tripley of the same as they appropriate the con-

> idm::get\_active\_network
> idm::foreach\_proto\_pin po -protobox \_\_CiType\_16\_30a98de8...

> idm::object\_name \_\_CiType\_17\_30aac34c
> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac34c

> idm::object\_name \_\_CiType 20 3057fc90

> idm::object\_name \_\_CiType\_17\_30aac328

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac328

> idm::object\_name \_\_CiType\_20\_30590568

> idm::object\_name \_\_CiType\_17\_30aac304

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac304

> idm::object\_name \_\_CiType\_20\_3058f6e0

> idm::object\_name \_\_CiType\_17\_30aac2e0

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac2e0

> idm::object\_name \_\_CiType\_20\_3057f6c8

> idm::object\_name \_\_CiType\_17\_30aac2bc

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac2bc

> idm::object\_name \_\_CiType\_20\_3057fe48

> idm::object\_name \_\_CiType\_17\_30aac298

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30aac298

> idm::object\_name \_\_CiType\_20\_3059af68

> idm::object\_name \_\_CiType\_17\_30a4bda8

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bda8

> idm::object\_name \_\_CiType\_20\_3059ae78

> idm::object\_name \_\_CiType\_17\_30a4bd84

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bd84

> idm::object\_name \_\_CiType\_20\_3057fd58

> idm::object\_name \_\_CiType\_17\_30a4bd60

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bd60

> idm::object name CiType 20 30568e50

> idm::object\_name \_\_CiType\_17\_30a4bd3c

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bd3c

> idm::object\_name \_\_CiType\_20\_3057fcb8

> idm::object\_name \_\_CiType\_17\_30a4bd18

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bd18

> idm::object\_name \_\_CiType\_20\_3057fdf8

> idm::object\_name \_\_CiType\_17\_30a4bcf4

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bcf4

> idm::object\_name \_\_CiType\_20\_3057f6a0

> idm::object\_name \_\_CiType\_17\_30a4bcd0

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bcd0

> idm::object\_name \_\_CiType\_20\_3056a2c8

> idm::object\_name \_\_CiType\_17\_30a4bcac

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bcac

> idm::object\_name \_\_CiType\_20\_30568d88

> idm::object\_name \_\_CiType 17 30a4bc88

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bc88

> idm::object\_name \_\_CiType\_20\_3057ff60

> idm::object\_name \_\_CiType\_17\_30a4bc64

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bc64

```
> idm::object_name __CiType_20_3058fe60
   > idm::object_name __CiType_17_30a4bc40
   > idm::get_net_from_proto_pin __CiType_17_30a4bc40
    > idm::object_name __CiType_20_3057fdd0
   > idm::object_name __CiType_17_30a4bc1c
   > idm::get_net_from_proto_pin __CiType_17_30a4bc1c
    > idm::object_name __CiType_20_3057f678
   > idm::object_name __CiType_17_30a4bbf8
   > idm::get_net_from_proto_pin __CiType_17_30a4bbf8
    > idm::object_name __CiType_20_3058f960
   > idm::object_name __CiType_17_30a4bbb0
   > idm::get_net_from_proto_pin __CiType_17_30a4bbb0
    > idm::óbject_name __CiType_20_3057fa60
   > idm::object_name __CiType_17_30a4bb8c
   > idm::get_net_from_proto_pin __CiType_17_30a4bb8c
    > idm::object_name __CiType_20_3057f628
   > idm::object_name __CiType_17_30a4bb44
   > idm::get_net_from_proto_pin __CiType_17_30a4bb44
    > idm::object_name __CiType_20_3057fa38
   > idm::object_name __CiType_17_30a4bb20
   > idm::get_net_from_proto_pin __CiType_17_30a4bb20
    > idm::object_name __CiType_20_3057fc68
                                              > idm::object_name __CiType_17_30a4bad8
   > idm::get_net_from_proto_pin __CiType_17_30a4bad8
 > idm::object_name __CiType_20_3057f600
   > idm::object_name __CiType_17_30a4bab4
   > idm::get_net_from_proto_pin __CiType_17_30a4bab4
---- > idm::object_name __CiType_20_3057fa10
   > idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin__CiType_17_30a4ba90
    > idm::object_name __CiType_20_3057fd80
   > idm::object_name __CiType_17_30a4ba6c
   > idm::get_net_from_proto_pin __CiType_17_30a4ba6c
    > idm::object_name __CiType_20_30568c98
   > idm::object_name __CiType_17_30a4ba48
   > idm::get_net_from_proto_pin __CiType_17_30a4ba48
    > idm::object_name __CiType_20_3057f650
   > idm::object_name __CiType_17_30a4ba24
   > idm::get_net_from_proto_pin __CiType_17_30a4ba24
     > idm::object_name __CiType_20_3057f7b8
   > idm::object_name __CiType_17_30a4ba00
   > idm::get_net_from_proto_pin __CiType_17_30a4ba00
     > idm::object_name __CiType_20_3058fbb8
    > idm::object_name __CiType_17_30a4b9dc
    > idm::get_net_from_proto_pin __CiType_17_30a4b9dc
     > idm::object_name __CiType_20_3059b1c0
    > idm::object_name __CiType_17_30a4b9b8
    > idm::get_net_from_proto_pin __CiType_17_30a4b9b8
     > idm::object_name __CiType_20_3057f808
    > idm::object_name __CiType_17_30a4b994
    > idm::get_net_from_proto_pin __CiType_17_30a4b994
     > idm::object_name __CiType_20_3059b648
    > idm::object_name __CiType_17_30a4b970
    > idm::get_net_from_proto_pin __CiType_17_30a4b970
     > idm::object_name __CiType_20_3057fec0
```

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> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
 > idm::object_name __CiType_20_3057fda8
> idm::get_net_from_proto_pin __CiType_17_30a4b928
 > idm::object_name __CiType_20_3059b7d8
> idm::object_name __CiType_17_30a4b904
> idm::get_net_from_proto_pin __CiType_17_30a4b904
 > idm::object_name __CiType_20_3057ff10
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto pin CiType 17 30a4b8bc
 > idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::object_name __CiType_20_30590540
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
 > idm::object_name __CiType_20_3057f790
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
 > idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17 _30a4b82c
 > idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17_30a4b808
> idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17 30a4b7e4
 > idm::object_name __CiType_20_3057f948
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
> idm::object_name __CiType_20_3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType_17_30a4b778
 > idm::object_name __CiType_20_3057f880
> idm::object_name __CiType_17_30a4b754
> idm::get_net_from_proto_pin __CiType_17_30a4b754
> idm::object_name __CiType_20_3057f858
> idm::object_name __CiType_17_30a4b730
> idm::get_net_from_proto_pin __CiType_17_30a4b730
 > idm::object_name __CiType_20_3057f830
> idm::object_name __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
```

> idm::object\_name \_ CiType\_17\_30a4b6c4

> idm::object\_name \_\_CiType\_20\_3057fbf0
> idm::object\_name \_\_CiType\_17\_30a4b6a0

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b6c4

```
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
> idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
> idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
 > idm::object_name __CiType_20_3057fb50
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
 > idm::object_name __CiType_20_3057fb28
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
 > idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538.
> idm::object_name ___CiType_20_3057fab0-_---
> idm::object_name    CiType 17 30a4b514 ...
> idm::get_net_from_proto_pin___CiType_17_30a4b514 -
> idm::object_name __CiType_20_3057fa88
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin-__CiType_17_30a4b4f0
 > idm::object_name __CiType_20_3057f9e8
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
 > idm::object_name __CiType_20_3057f9c0
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin __CiType_17_30a4b4a8
 > idm::object_name __CiType_20_3057fd08
> idm::get_net_from_proto_pin __CiType_17_30a4b484
 > idm::object_name __CiType_20_3057fce0
> idm::get_net_from_proto_pin __CiType_17_30a4b460
 > idm::object_name __CiType_20_3057f5d8
> idm::object_name __CiType_17_30a4b43c
> idm::get_net_from_proto_pin __CiType_17_30a4b43c
 > idm::object_name __CiType_20_3057f5b0
> idm::object_name __CiType_17_30a4b418
> idm::get_net_from_proto_pin __CiType_17_30a4b418
 > idm::object_name __CiType_20_3057f588
> idm::object_name __CiType_17_30a4b3f4
> idm::get_net_from_proto_pin __CiType_17_30a4b3f4
 > idm::object_name __CiType_17_30a4b3d0
> idm::get_net_from_proto_pin __CiType_17_30a4b3d0
 > idm::object_name __CiType_20_3057f718
> idm::object_name __CiType_17_30a4b3ac
> idm::get_net_from_proto_pin __CiType_17_30a4b3ac
```

```
> idm::object_name __CiType_20_3057f6f0
    > idm::object_name __CiType_17_30a4b364
    > idm::object_name __CiType_20_3057f768
    > idm::object_name __CiType_17_30a4b340
    > idm::get_net_from_proto_pin __CiType_17_30a4b340
     > idm::object_name __CiType 20 3057f740
  > dfstree {delbrkpt ALL }
   > delbrkpt ALL
[delbrkpt]: CMVC version 1.21 compiled on Mar 10 1999 at 05:04:49.
>>]: nextbox( SASname(RESTORE) );
[synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Execution time was 0.0 seconds.
[delbrkpt]: Removed 180 BRKPT gates
  > unpadnet
[unpadnet]: Removed 195 IOPADs.
   > idm::get_active_network
   > idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...
    > idm::object_name __CiType_17_30aac34c
   > idm::get_net_from_proto_pin __CiType_17_30aac34c
     > idm::object_name __CiType_20_3057fc90
  > idm::object_name __CiType_17_30aac328
> idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
 > idm::object_name __CiType_17_30aac304
 > idm::object_name __ClType_17_30aac304

> idm::get_net_from_proto_pin __CiType_17_30aac304
 > idm::object_name __CiType_20_3058f6e0
    > idm::object_name __CiType_17_30aac2e0
 > idm::get_net_from_proto_pin __CiType_17_30aac2e0
    > idm::object_name __CiType_20_3057f6c8-
    > idm::object_name __CiType_17_30aac2bc
    > idm::get_net_from_proto_pin __CiType_17_30aac2bc
     > idm::object_name __CiType_20_3057fe48
    > idm::object_name __CiType_17_30aac298
    > idm::get_net_from_proto_pin __CiType 17 30aac298
   > idm::object_name __CiType_20_3059af68
    > idm::object_name __CiType_17_30a4bda8
    > idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
    > idm::object_name __CiType_17_30a4bd84
    > idm::get_net_from_proto_pin __CiType_17_30a4bd84
     > idm::object_name __CiType_20_3057fd58
    > idm::object_name __CiType_17_30a4bd60
    > idm::get_net_from_proto_pin __CiType_17_30a4bd60
     > idm::object_name __CiType_20_30568e50
    > idm::object_name __CiType_17_30a4bd3c
    > idm::get net from proto pin CiType 17 30a4bd3c
     > idm::object_name __CiType_20_3057fcb8
    > idm::object_name __CiType_17_30a4bd18
    > idm::get_net_from_proto_pin __CiType_17_30a4bd18
     > idm::object_name __CiType_20_3057fdf8
    > idm::object_name __CiType_17_30a4bcf4
    > idm::get_net_from_proto_pin __CiType_17_30a4bcf4
```

```
> idm::object_name __CiType_20_3057f6a0
> idm::object_name __CiType_17_30a4bcd0
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
 > idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
 > idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
 > idm::object_name __CiType_20_3057ff60
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
 > idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
 > idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
 > idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0_
> idm::object_name __CiType_20_3057fa60
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin__CiType_17_30a4bb8c---
 > idm::object_name __CiType_20_3057f628
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
 > idm::object_name __CiType_20_3057fa38....
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
 > idm::object_name __CiType_20_3057fc68
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
 > idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
 > idm::object_name __CiType_20_3057fa10
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
 > idm::object_name __CiType_20_3057fd80
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
 > idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
 > idm::object_name __CiType_20_3057f650
> idm::get_net_from_proto_pin __CiType_17_30a4ba24
 > idm::object_name __CiType_20_3057f7b8
> idm::object_name __CiType_17_30a4ba00
> idm::get_net_from_proto_pin __CiType_17_30a4ba00
 > idm::object_name __CiType_20_3058fbb8
```

```
> idm::object_name __CiType_17_30a4b9dc
```

- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b9dc
- > idm::object\_name \_\_CiType\_20\_3059b1c0
- > idm::object\_name \_\_CiType\_17\_30a4b9b8
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b9b8
- > idm::object\_name \_\_CiType\_20\_3057f808
- > idm::object\_name \_\_CiType\_17\_30a4b994
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b994
- > idm::object\_name \_\_CiType\_20\_3059b648
- > idm::object\_name \_\_CiType\_17\_30a4b970
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b970
- > idm::object\_name \_\_CiType\_20\_3057fec0
- > idm::object\_name \_\_CiType\_17\_30a4b94c
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b94c
- > idm::object\_name \_\_CiType\_20\_3057fda8
- > idm::object\_name \_\_CiType\_17\_30a4b928
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b928
- > idm::object\_name \_\_CiType\_20\_3059b7d8
- > idm::object\_name \_\_CiType\_17\_30a4b904
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b904
- > idm::object\_name \_\_CiType\_20\_3057ff10
- > idm::object\_name \_\_CiType\_17\_30a4b8bc
- > idm::get\_net\_from\_proto\_pin\_\_\_CiType\_17\_30a4b8bc
- > idm::object\_name \_\_CiType\_20\_3059b8f0
- > idm::object\_name \_\_CiType\_17\_30a4b898
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b898
- -> idm::object\_name \_\_CiType\_20\_30590540
- > idm::object\_name \_\_CiType\_17\_30a4b874
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b874
- > idm::object\_name \_\_CiType\_20\_3057f790
- > idm::object\_name \_\_CiType\_17\_30a4b850
- > idm::get\_net\_from\_proto\_pin\_\_CiType\_17\_30a4b850
- > idm::object\_name \_\_CiType\_20\_3057fe70
- > idm::object\_name \_\_CiType\_17\_30a4b82c
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b82c
- > idm::object\_name \_\_CiType\_20\_3057f998
- > idm::object\_name \_\_CiType\_17\_30a4b808
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b808
- > idm::object\_name \_\_CiType\_20\_3057f970
- > idm::object\_name \_\_CiType\_17\_30a4b7e4
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b7e4
- > idm::object\_name \_\_CiType\_20\_3057f948
- > idm::object\_name \_\_CiType\_17\_30a4b7c0
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b7c0
- > idm::object\_name \_\_CiType\_20\_3057f920
- > idm::object\_name \_\_CiType\_17\_30a4b79c
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b79c
- > idm::object\_name \_\_CiType\_20\_3057f8d0
- > idm::object\_name \_\_CiType\_17\_30a4b778
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b778
- > idm::object\_name \_\_CiType\_20\_3057f880
- > idm::object\_name \_\_CiType\_17\_30a4b754
- > idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b754
- > idm::object\_name \_\_CiType\_20\_3057f858
- > idm::object\_name \_\_CiType\_17\_30a4b730

```
> idm::get_net_from_proto_pin __CiType_17_30a4b730
> idm::object_name __CiType_20_3057f830
> idm::get_net_from_proto_pin __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::get_net_from_proto_pin __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
> idm::object_name __CiType_17_30a4b6c4
> idm::get_net_from_proto_pin __CiType_17_30a4b6c4
> idm::object_name __CiType_20_3057fbf0
> idm::object_name __CiType_17_30a4b6a0
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
> idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
> idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
 > idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17_30a4b5ec
> idm::object_name __CiType_20_3057fb50
> idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
> idm::object_name __CiType_20_3057fb00
>_idm::object_name ___CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
 > idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
 > idm::object_name __CiType_20_3057fab0
> idm::object_name __CiType_17_30a4b514
> idm::get_net_from_proto_pin __CiType_17_30a4b514
 > idm::object_name __CiType_20_3057fa88
> idm::object_name __CiType_17_30a4b4f0
> idm::get_net_from_proto_pin __CiType_17_30a4b4f0
 > idm::object_name __CiType_20_3057f9e8
> idm::object_name __CiType_17_30a4b4cc
> idm::get_net_from_proto_pin __CiType_17_30a4b4cc
 > idm::object_name __CiType_20_3057f9c0
> idm::object_name __CiType_17_30a4b4a8
> idm::get_net_from_proto_pin _CiType_17_30a4b4a8
 > idm::object_name __CiType_20_3057fd08
> idm::object_name __CiType_17_30a4b484
> idm::object_name __CiType_20_3057fce0
> idm::object_name __CiType_17_30a4b460
> idm::get_net_from_proto_pin __CiType_17_30a4b460
 > idm::object_name __CiType_20_3057f5d8
> idm::object_name __CiType_17_30a4b43c
```

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4b43c

```
> idm::object_name __CiType_20_3057f5b0
  > idm::object_name __CiType_17_30a4b418
  > idm::get_net_from_proto_pin __CiType_17_30a4b418
   > idm::object_name __CiType_20_3057f588
  > idm::object_name __CiType_17_30a4b3f4
  > idm::get_net_from_proto_pin __CiType_17_30a4b3f4
   > idm::object_name __CiType_20_3057f560
  > idm::object_name __CiType_17_30a4b3d0
  > idm::get_net_from_proto_pin __CiType_17_30a4b3d0
   > idm::object_name __CiType_20_3057f718
  > idm::object_name __CiType_17_30a4b3ac
  > idm::get_net_from_proto_pin __CiType_17_30a4b3ac
   > idm::object_name __CiType_20_3057f6f0
  > idm::object_name __CiType_17_30a4b364
  > idm::get_net_from_proto_pin __CiType_17_30a4b364
   > idm::object_name __CiType_20_3057f768
  > idm::object_name __CiType_17_30a4b340
  > idm::get_net_from_proto_pin __CiType_17_30a4b340
  > idm::object_name __CiType_20_3057f740
> sweep -
```

[sweep]: sweep deleted 0 signals and 0 usage boxes.

The model has 754 signals, 531 usage boxes and 1369 connections.

>:checkfan

## Electrical Violations in Network 'IDCDSUC'

보는 것들이 한다는 사람들이 보고 있는데 보다 그 것이 되었다. 그 사람들이 가장 바꾸 보는데 하는데 그렇게 되었다. 그 유모를	Capacitance Slew Sink
Fanout	
Pin/Port -> Net	Limit / AdjLim / Actual Limit / AdjLim / Actual
Limit / AdjLim / Actual	
eu_iu_enter_slow_md -> eu_iu_enter_slo	ow_md 141.00 / 141.00 / 16.73 290.00
"/ 290.00 / 352.00 *   12 /   12 /   1   1   1   1   1   1   1   1   1	
op_inq_stores -> op_inq_stores	141.00 / 141.00 / 159.72 * 290.00 /
290.00 / 112.00 12 / 12 / 3 3	
eu_iu_mmode -> eu_iu_mmode	141.00 / 141.00 / 32.56 290.00 /
290.00 / 326.00 * 12 / 12 / 2 2	
du_iu_hold_aa_req -> du_iu_hold_aa_r	eq 141.00 / 141.00 / 141.99 * 290.00
/ 290.00 / 424.00 * 12 / 12 / 2 2	- · · · · · · · · · · · · · · · · · · ·
eu_iu_fpu_end_op -> eu_iu_fpu_end_o	op 141.00 / 141.00 / 30.80 290.00 /
290.00 / 339.00 * 12 / 12 / 1 1	
eu_iu_misc_hold -> eu_iu_misc_hold	141.00 / 141.00 / 19.15 290.00 /
290.00 / 332.00 * 12 / 12 / 1 1	
op_mcend_raw -> op_mcend_raw	141.00 / 141.00 / 144.35 * 290.00 /
290.00 / 91.00 12 / 12 / 3 3	
clkg -> clkg	141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
60.00 12/ 12/ 3 3	
du_iu_quiesced -> du_iu_quiesced	141.00 / 141.00 / 20.50 290.00 /
290.00 / 338.00 * 12 / 12 / 1 1	
iq_empty -> iq_empty	141.00 / 141.00 / 170.11 * 290.00 / 290.00
/116.00 12/ 12/ 4 4	
gptr_scan_in -> gptr_scan_in	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 12 / 12 / 1 1	
gptr_a_clk -> gptr_a_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /
0.00 12 / 12 / 1 1	444.00 / 444.00 / 404.00 / 404.00
gptr_b_clk -> gptr_b_clk	141.00 / 141.00 / 1011.00 * 0.00 / 0.00 /

```
0.00
       12/ 12/ 1 1
                                             141.00 / 141.00 / 145.52 * 100.00 / 100.00 /
                     -> clkq2
clkq2
        12/ 12/
                    3 3
60.00
                                                         141.00 / 141.00 / 15.67 290.00
eu_iu_fxu_exc_cond
                           -> eu_iu_fxu_exc_cond
                         12/ 1 1
/ 290.00 / 390.00 *
                   12/
                                                       141.00 / 141.00 / 16.89 290.00 /
du iu store_status(2)
                          -> du_iu_store_status(2)
290.00 / 500.00 *
                 12/
                       12 / 1 1
                                                        141.00 / 141.00 / 47.57 290.00 /
                          -> eu_iu_srlz_op_actn(0)
eu_iu_srlz_op_actn(0)
                       12/ 2 2
290.00 / 374.00 *
                  12/
                                                        141.00 / 141.00 / 47.57 290.00 /
                           -> eu iu srlz_op_actn(1)
eu_iu_srlz_op_actn(1)
                       12/ 2 2
290.00 / 341.00 *
                 12/
                                                     141.00 / 141.00 / 318.91 * 290.00 /
num dcd cvl(1)
                         -> num_dcd_cyl(1)
                12/ 12/ 1 1
290.00 / 80.00
                                                           141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(0)
                            -> eu_iu_srlz_op_encode(0)
290.00 / 290.00 / 401.00 *
                          12/ 12/ 1 1
                                                           141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(1)
                            -> eu iu srlz_op_encode(1)
                          12/ 12/ 1 1
290.00 / 290.00 / 400.00 *
                                                           141.00 / 141.00 / 16.89
eu iu srlz_op_encode(2)
                           -> eu_iu_srlz_op_encode(2)
290.00 / 290.00 / 420.00 *
                          12/ 12/ 1 1
eu_iu_srlz_op_encode(3)
                           -> eu_iu_srlz_op_encode(3)
                                                            141.00 / 141.00 / 16.89
290.00 / 290.00 / 302.00 *
                          12/ 12/ 1 1
                            -> eu_iu_srlz_op_encode(4)
                                                           -141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(4)
290.00 / 290.00 / 406.00 *
                          ---
                          -> eu_iu_srlz_op_encode(5)
                                                           141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(5)
290.00 / 290.00 / 373.00 *
                          12 / 12 / 1 1
eu_iu_srlz_op_encode(6)
                                                            141.00 / 141.00 / 16.89
                            -> eu_iu_srlz_op_encode(6)
290.00 / 290.00 / 354.00 * 12 / 12 / 1 1
                                                           141.00 / 141.00 / 16.89
eu_iu_srlz_op_encode(7)
                          -> eu iu srlz op encode(7)
                        --12/ 12/---1 -1 -- - - ----
290.00 / 290.00 / 398.00 *
                                                           141.00 / 141.00 / 16.89
                          -> eu_iu_srlz_op_encode(8)
eu iu srlz op encode(8)
290.00 / 290.00 / 367.00 *
                          12 / 12 / 1 1
                                                            141.00 / 141.00 / 16.89
                          -> eu_iu_srlz_op_encode(9)
eu iu_srlz_op_encode(9)
290.00 / 290.00 / 323.00 *
                          12/ 12/ 1 1
                                                           141.00 / 141.00 / 16.89
                             -> eu_iu_srlz_op_encode(11)
eu_iu_srlz_op_encode(11)
290.00 / 290.00 / 500.00 *
                          12/ 12/ 1 1
                                                                78.50 / 78.50 / 220.92 *
c1@slow mode.clockblock:cb_clk_32_1 -> slow_mode.c1_1
200.00 / 200.00 / 60.00 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                                                78.50 / 78.50 / 222.27 *
c2@slow_mode.clockblock:cb_clk_32_1 -> slow_mode.c2_1
                         12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
clka@slow_mode.clockblock:cb_clk_32_ -> slow_mode.clka_1
                                                                78.50 / 78.50 / 212.39 *
200.00 / 200.00 / 184.59 12 / 12 / 13 * 13 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                                                78.50 / 78.50 / 237.92 *
c1@slow_mode.clockblock_1:cb_clk_32_ -> slow_mode.c1_2
                       12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO_SERIAL
                                                                78.50 / 78.50 / 239.36 *
c2@slow mode.clockblock_1:cb_clk_32_ -> slow_mode.c2_2
                       12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
                                                                78.50 / 78.50 / 228.73 *
clka@slow_mode.clockblock_1:cb_clk_3 -> slow_mode.clka_2
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                                                78.50 / 78.50 / 237.92 *
c1@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c1_3
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
```

```
NO SERIAL
c2@slow_mode.clockblock_2:cb_clk_32_ -> slow_mode.c2_3
                                                            78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
clka@slow_mode.clockblock_2:cb_clk_3 -> slow mode.clka 3
                                                            78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c1@slow_mode.clockblock_3:cb_clk_32_ -> slow mode.c1 4
                                                            78.50 / 78.50 / 237.92 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
                                          Capacitance
                                                            Slew
                                                                         Sink
Fanout
Pin/Port
                     -> Net
                                           Limit / AdjLim / Actual Limit / AdjLim / Actual
Limit / AdjLim / Actual
c2@slow_mode.clockblock_3:cb_clk_32_ -> slow_mode.c2_4
                                                            78.50 / 78.50 / 239.36 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
clka@slow_mode.clockblock_3:cb_clk_3 -> slow_mode.clka_4
                                                            78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79. 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
c1@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c1_5
                                                            78.50 / 78.50 / 237.91 *
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO SERIAL
c2@slow_mode.clockblock_4:cb_clk_32_ -> slow_mode.c2_5 78.50 / 78.50 / 239.37 *
200.00 / 200.00 / 60.00
                     12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
                                                        78.50 / 78.50 / 228.73 *
clka@slow_mode.clockblock_4:cb_clk_3 -> slow_mode.clka 5
200.00 / 200.00 / 198.79 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL_
NO SERIAL
200.00 / 200.00 / 60.00 12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
NO_SERIAL
c2@slow_mode.clockblock_5:cb_clk_32_ -> slow_mode.c2
                                                         78.50 / 78.50 / 239.37 *
                       12 / 12 / 14 * 14 KEEP_BTR KEEP_BHC NO_PARALLEL
200.00 / 200.00 / 60.00
NO SERIAL
clka@slow_mode.clockblock_5:cb_clk_3 -> slow_mode.clka
                                                           78.50 / 78.50 / 228.73 *
200.00 / 200.00 / 198.79 12 / -12 / 14 * 14 KEEP_BTR KEEP_BHC-NO_PARALLEL
NO SERIAL
y@C167:cs_invvv11e
                          -> dcd_succ_last_t1
                                                     638.00 / 638.00 / 1011.00 *
301.00 / 301.00 / 300.47
                         12/ 12/ 1 1 KEEP_BTR
y@C1994:cs invvn01c
                           -> N1531
                                                  68.00 / 68.00 / 77.40 * 290.00 /
290.00 / 286.02
                12/ 12/ 2 2
y@C2013:cs_invvn12d
                           -> iu_slow_mode_t1
                                                      796.00 / 796.00 / 1011.00 *
301.00 / 301.00 / 279.84
                         12/ 12/ 1 1
                           -> idcdsuc_err
v@C2082:cs invvn12d
                                                   796.00 / 796.00 / 1011.00 * 301.00
/ 301.00 / 281.78
                       12/ 1 1
                 12 /
y@C2194:cs invvn07c
                           -> N1681
                                                  261.00 / 261.00 / 271.46 * 290.00 /
290.00 / 261.53
                 12 / 12 / 7 7
                            -> iu_reset_op_c_t1
v@C2393:cs nnd2v13d
                                                      813.00 / 813.00 / 1044.40 *
                         12/ 12/ 3 3
290.00 / 290.00 / 267.22
y@C2646:cs_invvn04c
                           -> N1645
                                                  133.00 / 133.00 / 150.69 * 290.00 /
               12/ 12/ 6 6
290.00 / 275.60
y@C2726:cs_nnd2n11c
                           -> dsucc_or_agi
                                                     500.00 / 500.00 / 540.60 * 290.00
/ 290.00 / 258.01
                12/ 12/ 2 2
```

```
996.00 / 996.00 / 1081.45 * 290.00
                                -> dcd_succ_last
v@C2744:cs_invvn13c
                            12/ 7 7
/ 290.00 / 269.95
                     12/
                                                              326.00 / 326.00 / 234.15
                                                                                          290.00 /
y@C2800:cs_invvn08c
                                 -> N1290
                           12 / 14 * 14
                    12/
290.00 / 193.42
                                                               167.00 / 167.00 / 183.47 * 290.00 /
                                  -> N1097
y@C2728rwr:cs_invvn05c
                                 4 4
290.00 / 266.58
                    12/
                          12 /
                                                                                           290.00 /
                                                               797.00 / 797.00 / 402.55
                                 -> gbfonet_0
y@gbfocell_0:cs_invvn12c
290.00 / 149.98
                    12 /
                         12 / 20 * 20
                                                                    247.00 / 247.00 / 301.71 *
I2_out_n@frc_blk_1cyc.reg_n.lat_0:cl -> frc_blk_1cyc_q
                              12/ 12/
290.00 / 290.00 / 242.45
[BD-500900]: (W) There were 61 electrical violations.
  > source cte_timing_reports.tcl
Loading: /afs/watson.ibm.com/projects/vtsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_timing_reports.tcl
   > summary_report -file /afs/apd/func/vlsi/alliance00/timin...
[measure]: Execution time was 0.0 seconds.
     > write_histogram_report -file /afs/apd/func/vlsi/alliance...
[ET-0018]: >Begin...Histogram Report
        for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.histogram.
[ET-0019]: <End.....Histogram Report.
     > write_checks_report -file /afs/apd/func/vlsi/alliance00/...
[ET-0018]: >Begin...Checks Report
        for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.check.
[ET-0916]: No User Define Setup Tests.
[ET-0916]: No User Define Hold Tests.
[ET-0917]: No Clock Pulse Width Tests.
[ET-0918]: No Clock Separation Tests.
[ET-0919]: No End Of Cycle Tests.
[ET-0922]: No Loop Tests.
[ET-0915]: No User Defined Required Arrival Times Late Tests.
[ET-0915]: No User Defined Required Arrival Times Early Tests.
[ET-0916]: No Abstract Tests.
 [ET-0019]: <End.....Checks Report.
      > write end point_report -file /afs/apd/func/vlsi/alliance...
 [ET-0018]: >Begin...New EndPoint Report
         for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.endpoint.
 [ET-0019]: <End.....New Endpoint Report.
      > write_net_report -late -file /afs/apd/func/vlsi/alliance...
 [ET-0018]: >Begin...Nets Report
         for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.net.
 [ET-0019]: <End.....Nets Report.
```

> write\_comprehensive\_report -file /afs/apd/func/vlsi/alli...

```
[ET-0018]: >Begin...Comprehensive Report
         for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.comp.
[ET-0019]: <End.....Comprehensive Report.
      > write_audit_report -file /afs/apd/func/vlsi/alliance00/t...
[ET-0018]: >Begin...Generate Audit Report
         for file /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/reports/macros//IDCDSUC.lm.audit.
[ET-0019]: <End.....Generate Audit Report.
    > CTE::writeverilog {FILE(/afs/apd/func/vlsi/alliance00/ti...
[writeverilog]: Release 1.0 Compiled on Jan 7 1999 at 18:31:22.
[writeverilog]: Writing out the proto for IDCDSUC
[writeverilog]: Writing out the proto for IDCDSUC in top proto IDCDSUC
    > source cte_bd2epic
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/cte/2.0/tcl/cte_bd2epic.tcl
      > unpadnet
[unpadnet]: Removed 0 IOPADs.
       > idm::get active network
      > idm::get_active_network
> idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...
> idm::object_name __CiType_17_30aac34c
> idm::get_net_from_proto_pin __CiType_17_30aac34c
  > idm::object_name __CiType_20_3057fc90
> idm::object_name __CiType_17_30aac328
> idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
> idm::object_name __CiType_17_30aac304
> idm::get_net_from_proto_pin __CiType_17_30aac304
> idm::object_name __CiType_20_3058f6e0
> idm::object_name __CiType_17_30aac2e0
> idm::object_name __CiType_17_30aac2e0
         > idm::object_name __CiType_20_3057fc90
   > idm::get_net_from_proto_pin __CiType_17_30aac2e0

> idm::object_name __CiType_20_3057f6c8

> idm::object_name __CiType_17_30aac2bc

> idm::get_net_from_proto_pin __CiType_17_30aac2bc

> idm::object_name __CiType_20_3057fe48
        > idm::object_name __CiType_17_30aac298
        > idm::get_net_from_proto_pin __CiType_17_30aac298
         > idm::object_name __CiType_20_3059af68
        > idm::object_name __CiType_17_30a4bda8
        > idm::get_net_from_proto_pin __CiType_17_30a4bda8
> idm::object_name __CiType_20_3059ae78
        > idm::object_name __CiType_17_30a4bd84
        > idm::get_net_from_proto_pin __CiType_17_30a4bd84
         > idm::object_name __CiType_20_3057fd58
        > idm::object_name __CiType_17_30a4bd60
        > idm::get_net_from_proto_pin __CiType_17_30a4bd60
         > idm::object_name __CiType_20_30568e50
        > idm::object_name __CiType_17_30a4bd3c
        > idm::get_net_from_proto_pin __CiType_17_30a4bd3c
         > idm::object_name __CiType_20_3057fcb8
        > idm::object_name __CiType_17_30a4bd18
        > idm::get_net_from_proto_pin __CiType_17_30a4bd18
         > idm::object_name __CiType_20_3057fdf8
        > idm::object_name __CiType_17_30a4bcf4
        > idm::get_net_from_proto_pin __CiType_17_30a4bcf4
         > idm::object_name ___CiType_20_3057f6a0
```

```
> idm::object_name __CiType_17_30a4bcd0
> idm::get_net_from_proto_pin __CiType_17_30a4bcd0
 > idm::object_name __CiType_20_3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
 > idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::get_net_from_proto_pin __CiType_17_30a4bc88
 > idm::object_name __CiType_20_3057ff60
> idm::object_name _CiType_17_30a4bc64
> idm::get_net_from_proto_pin__CiType_17_30a4bc64
 > idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
 > idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
 > idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin __CiType_17_30a4bbf8
 > idm::object_name __CiType_20_3058f960
> idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
 > idm::object_name __CiType_20_3057fa60.
> idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
 > idm::object_name __CiType_20_3057f628
> idm::object_name __CiType_17_30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
 > idm::object_name __CiType_20_3057fa38
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
 > idm::object_name __CiType_20_3057fc68
> idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
> idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
> idm::get_net_from_proto_pin __CiType_17_30a4bab4
 > idm::object_name __CiType_20_3057fa10
> idm::object_name __CiType_17_30a4ba90
> idm::get_net_from_proto_pin __CiType_17_30a4ba90
 > idm::object_name __CiType_20_3057fd80
> idm::object_name __CiType_17_30a4ba6c
> idm::get_net_from_proto_pin __CiType_17_30a4ba6c
 > idm::object_name __CiType_20_30568c98
> idm::object_name __CiType_17_30a4ba48
> idm::get_net_from_proto_pin __CiType_17_30a4ba48
 > idm::object_name __CiType_20_3057f650
> idm::object_name __CiType_17_30a4ba24
 > idm::get_net_from_proto_pin __CiType_17_30a4ba24
  > idm::object_name __CiType_20_3057f7b8
 > idm::object_name __CiType_17_30a4ba00
 > idm::get_net_from_proto_pin __CiType_17_30a4ba00
  > idm::object_name __CiType_20_3058fbb8
```

> idm::object\_name \_\_CiType\_17\_30a4b9dc

```
> idm::get_net_from_proto_pin __CiType_17_30a4b9dc
 > idm::object_name __CiType_20_3059b1c0
> idm::object_name __CiType_17_30a4b9b8
> idm::get_net_from_proto_pin __CiType_17_30a4b9b8
 > idm::object_name __CiType_20_3057f808
> idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin CiType 17 30a4b994
 > idm::object_name __CiType_20_3059b648
> idm::object_name __CiType_17_30a4b970
> idm::get_net_from_proto_pin __CiType_17_30a4b970
 > idm::object_name __CiType_20_3057fec0
> idm::object_name __CiType_17_30a4b94c
> idm::get_net_from_proto_pin __CiType_17_30a4b94c
 > idm::object_name __CiType_20_3057fda8
> idm::object_name __CiType_17_30a4b928
> idm::get_net_from_proto_pin __CiType_17_30a4b928
 > idm::object_name __CiType_20_3059b7d8
> idm::get_net_from_proto_pin __CiType_17_30a4b904
- > idm::object_name __CiType_20_3057ff10
> idm::object_name __CiType_17_30a4b8bc
> idm::get_net_from_proto_pin __CiType_17_30a4b8bc
 > idm::object_name __CiType_20_3059b8f0
> idm::object_name __CiType_17_30a4b898
> idm::get_net_from_proto_pin __CiType_17_30a4b898
 > idm::object_name __CiType_20_30590540
> idm::object_name __CiType_17_30a4b874
> idm::get_net_from_proto_pin __CiType_17_30a4b874
 > idm::object_name __CiType_20_3057f790
> idm::object_name __CiType_17_30a4b850
> idm::get_net_from_proto_pin __CiType_17_30a4b850
 > idm::object_name __CiType_20_3057fe70
> idm::object_name __CiType_17_30a4b82c
> idm::get_net_from_proto_pin __CiType_17_30a4b82c
 > idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17_30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
 > idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::get_net_from_proto_pin __CiType_17_30a4b7e4
 > idm::object_name __CiType_20_3057f948
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
 > idm::object_name __CiType 20 3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::get_net_from_proto_pin __CiType_17_30a4b79c
 > idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType 17 30a4b778
 > idm::object_name __CiType_20_3057f880
> idm::object_name __CiType_17_30a4b754
> idm::get_net_from_proto_pin __CiType_17_30a4b754
 > idm::object_name __CiType_20_3057f858
```

> idm::object\_name \_\_CiType\_17\_30a4b730

```
> idm::object_name __CiType_20_3057f830
 > idm::object_name __CiType_17_30a4b70c
 > idm::get_net_from_proto_pin __CiType_17_30a4b70c
  > idm::object_name __CiType_20_3057fc40
 > idm::object_name __CiType_17_30a4b6e8
 > idm::get_net_from_proto_pin __CiType_17_30a4b6e8
> idm::object_name __CiType_20_3057fc18
 > idm::object_name __CiType_17_30a4b6c4
 > idm::get_net_from_proto_pin __CiType_17_30a4b6c4
  > idm::object_name __CiType_20_3057fbf0
 > idm::object_name __CiType_17_30a4b6a0
 > idm::get_net_from_proto_pin __CiType_17_30a4b6a0
  > idm::object_name __CiType_20_3057fbc8
 > idm::object_name __CiType_17_30a4b67c
 > idm::get_net_from_proto_pin __CiType_17_30a4b67c
  > idm::object_name __CiType_20_3057fba0
 > idm::object_name __CiType_17_30a4b634
 > idm::get_net_from_proto_pin __CiType_17_30a4b634
  > idm::object_name __CiType_20_3057fb78
 > idm::object_name __CiType_17_30a4b5ec
 > idm::get_net_from_proto_pin __CiType_17_30a4b5ec
  > idm::object_name __CiType_20_3057fb50
 > idm::object_name __CiType_17_30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
  > idm::object_name __CiType_20_3057fb28 ____
 > idm::object_name __CiType_17_30a4b580
 > idm::get_net_from_proto_pin__CiType_17_30a4b580
 > idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::object_name __CiType_20_3057fad8
 > idm::object_name __CiType_17_30a4b538
 > idm::get_net_from_proto_pin __CiType_17_30a4b538
  > idm::object_name __CiType_20_3057fab0
 > idm::object_name __CiType_17_30a4b514
 > idm::get_net_from_proto_pin __CiType_17_30a4b514
  > idm::object_name __CiType_20_3057fa88
 > idm::object_name __CiType_17_30a4b4f0
 > idm::get_net_from_proto_pin __CiType_17_30a4b4f0
  > idm::object_name __CiType_20_3057f9e8
 > idm::object_name __CiType_17_30a4b4cc
 > idm::get_net_from_proto_pin __CiType_17_30a4b4cc
  > idm::object_name __CiType_20_3057f9c0
 > idm::object_name __CiType_17_30a4b4a8
 > idm::get_net_from_proto_pin __CiType_17_30a4b4a8
  > idm::object_name __CiType_20_3057fd08
 > idm::object_name __CiType_17_30a4b484
 > idm::get_net_from_proto_pin __CiType_17_30a4b484
  > idm::object_name __CiType_20_3057fce0
 > idm::object_name __CiType_17_30a4b460
 > idm::get_net_from_proto_pin __CiType_17_30a4b460
  > idm::object_name __CiType_20_3057f5d8
 > idm::object_name __CiType_17_30a4b43c
 > idm::get_net_from_proto_pin __CiType_17_30a4b43c
  > idm::object_name __CiType_20_3057f5b0
```

```
> idm::object_name __CiType_17_30a4b418
       > idm::get_net_from_proto_pin __CiType_17_30a4b418
         > idm::object name CiType 20 3057f588
       > idm::object_name __CiType_17_30a4b3f4
       > idm::get_net_from_proto_pin __CiType_17_30a4b3f4
        > idm::object_name __CiType_20_3057f560
       > idm::object_name __CiType_17_30a4b3d0
       > idm::get_net_from_proto_pin __CiType_17_30a4b3d0
         > idm::object_name __CiType_20_3057f718
       > idm::object_name __CiType_17_30a4b3ac
       > idm::get_net_from_proto_pin __CiType_17_30a4b3ac
         > idm::object_name __CiType_20_3057f6f0
       > idm::object_name __CiType_17_30a4b364
        > idm::get_net_from_proto_pin __CiType_17_30a4b364
         > idm::object_name __CiType_20_3057f768
        > idm::object_name __CiType_17_30a4b340
       > idm::get_net_from_proto_pin __CiType_17_30a4b340
         > idm::object_name __CiType_20_3057f740
     > delbrkpt ALL
>>]: nextbox( SASname(RESTORE) );
 [synsasname]: Restored 0 BRKPT net names
[synsasname]: Restored 189 REG and SEQUENTIAL output net names
[synsasname]: Hestored 109 DEG and DEGGEN, LESS, [synsasname]: Execution time was 0.0 seconds. [delbrkpt]: Removed 0 BRKPT gates
     > cleanse
> cleanse
Removed 0 boxes[sweep]: sweep deleted 2 signals and 0 usage boxes.
The model has 754 signals, 531 usage boxes and 1369 connections.
[
>>]: nextbox( invrem(),onein(),twoin() );
[BD-40600]: Removed 0 double inverters.
[invrem]: Execution time was 0.0 seconds.
 [BD-40500]: Removed 0 noninverting buffers.
 [BD-40501]: Changed 0 gates to inverters.
 [onein]: Execution time was 0.0 seconds.
 [BD-40550]: Removed 0 redundant pins.
 [twoin]: Execution time was 0.0 seconds.
 [cte]: Removed 0 boxes.
 [cte]: Execution time was 0.0 seconds.
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 754 signals, 531 usage boxes and 1369 connections.
 [cleanup]: 0 boxes disconnected
 [sweep]: sweep deleted 0 signals and 0 usage boxes.
                         The model has 754 signals, 531 usage boxes and 1369 connections.
 >>1: nextbox( twoin() ):
 [BD-40550]: Removed 0 redundant pins.
 [twoin]: Execution time was 0.0 seconds.
     > timing reset
 [timing_reset]: Timing has been reset.
      > write_end_point_report -points 2
 [ET-0018]: >Begin...New EndPoint Report
        for file /tmp/end_point_report..92476.
 [ET-0019]: <End.....New Endpoint Report.
```

Sun Apr 18 22:10:04 1999

Part: IDCDSUC

Mode: Late Mode / Nominal EDA EinsTimer EndPoint Report

Release Level: 03.01 and Compiled: Wed Mar 24 22:00:23 1999 Min. Slack: -1.13427E+38 Max. Slack: 1.13427E+38

Sort Field: Slack

Max. Endpoints: 2

Cause of Slack

Abbreviation Comparison/Description

Slack due to a point downstream on path Slack Continuation SlkCont ( ARRIVAL TIME < REQUIRED ARRIVAL TIME) Required Arrival Time RAT ( ARRIVAL TIME < ASSERTED REQUIRED ARRIVAL Asserted Required Arrival Time AssrtRAT TIME) ( DATA ARRIVAL TIME + CLOCK GATING SETUP < CLOCK Clock Gating Setup ClkGSet ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME - CLOCK GATING HOLD > CLOCK **Clock Gating Hold** ClkGHld ARRIVAL TIME + ADJUST ) **CIKTPW** ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK Clock Tree Pulse Width TRAILING EDGE ) ( DATA ARRIVAL TIME + SETUP < CLOCK ARRIVAL TIME + Setup Setup ADJUST) ( DATA ARRIVAL TIME - HOLD > CLOCK ARRIVAL TIME + Hold Hold ADJUST ) EndOfC (DATA-ARRIVAL TIME + CYCLE < CLOCK ARRIVAL TIME + EndOfCycle 1 . ADJUST ) ( CLOCK LEADING EDGE + PULSE WIDTH < CLOCK ClkPW · ClockPulseWidth TRAILING EDGE) CIKSep (CLOCK1 ARRIVAL TIME + CLOCK SEPARATION < CLOCK2 ClockSeparation ARRIVAL TIME + ADJUST ) ( DATA ARRIVAL TIME + FLUSH DELAY < OUTPUT TIME FROM Loop ALTest CLOCK + ADJUST ) Slack discontinuity due to failed test Arrival Time Limiting **ATLimit** 

Num/ LimitedAT/ Delay/ Failed Test/
Test PinName E Phase AT Slack Slew CL FO Cell P Func T.Adj
NetName

 1 xeu_dsbl_aftr_reg_n_lat_0/a		F C3+R	1761	-448	88	31 1 cl_in	vvn 0	7d SRL
47 n1013							_	
Setup xeu_dsbl_aftr_reg_n_lat_0/c1		F C3-	160		60	221 13 cl_in	vvn 0	7d
1200 slow_mode.c1_1			4.40	00	~4	4	00 - 1	IAAID
>{a} xc2856/y	FC3+	R 1761	-448	88	31	1 cs_nnd2n	UZC N	IANU
0 n1013						4 10	00 - 1	IANID
> xc2856/b	R C3+	R 1699	-448	104	1/	1 cs_nnd2n	02C N	IAND
62 n522								
>{b} xc2833/y	R C3+	R 1699	-448	104	17	' 1 cs_nnd2n	02c r	NAND
0 n522						10	00	
> xc2833/b	F C3+	R 1625	-448	129	234	14 cs_nnd2n	02c	NAND
74 n1290								
> xc2800/y	F C3+F	R 1625	-448	129	234	14 cs_invvn	08c N	101
0 n1290						_		
> xc2800/a	R C3+	R 1533	-448	170	37	1 cs_invvn	08c N	TC
92 n1648								
>{c} xc2779/y	R C3+	·R 1533	-448	170	37	' 1 cs_nnd2n	02c l	NAND
0 n1648								

	> xc2779/b	FC3+R	1419 -448	164 151 6 cs_nnd2	n 02c NAND
	114 n1645				
	> xc2646/y 0 n1645	F C3+R	1419 -448	164 151 6 cs_invvn	04c NOT
	> xc2646/a	R C3+R	1205 440	440 04 4 1-	04 1107
	114 n1746	n Co+n	1305 -446	110 21 1 cs_invvn	040 NO I
	>{d} xc2620/y	R C3+R	1305 -448	110 21 1 cs_nnd2	n 02c NAND
	0 n1746			_	
	> xc2620/a	F C3+R	1230 -448	133 67 4 cs_nnd2n	02c NAND
	75 n1740	E CO. D	1000 110	400 0- 4	
	> xc2602/y n1740	F C3+R	1230 -448	133 67 4 cs_invvn	02c NOT 0
	> xc2602/a 95 n905	R C3+R	1135 -448	146 37 2 cs_invvn	02c NOT
	>{e} xc2546/y 0 n905	R C3+R	1135 -448	146 37 2 cs_nnd2i	n 02c NAND
	> xc2546/a 90 n1647	F C3+R	1045 -448	96 17 1 cs_nnd2n	02c NAND
	> xc1928/y		1045 -448	96 17 1 cs_invvn	01c NOT 0
and the second	n1647 > xc1928/a 57 eu_iu_fxu_exc_cond	R C3+R	988 -448	390 16 1 cs_invvn	01c NOT
ا المراكب المر المراكب المراكب المراك	> eu_iu_fxu_exc_cond	R C3	8+R = 988	44839016 1 PI	0
	eu_iu_fxu_exc_cond				to the public of the control of the
	2 xeu_frc_milli_reg_n_lat_0/a 47_n994	F C	3+R 1761	-448 88 31 1 cl_in	vvn 07d SRL
	Setup xeu_frc_milli_reg_n_lat_0/c 1200 slow mode.c1 5	1F	C3- 160	60 238 14 cl_inv	∕vn 07d
en e	1200 slow_mode.c1_5 >{a} xc2857/y 0 n994	FC3+R	1761 -448	88 31 1 cs_nnd2n	02c NAND
	0 n994 > xc2857/b 62 n505	R C3+R	1699 -448	104 17 1 cs_nnd2n	02c NAND
	>Jb) vc2834/v	D CO. D	1000 440	404 47 4 10	

	57 eu_iu_fxu_exc_cond		_			10 100_1110111 0101401
	> eu_iu_fxu_exc_cond eu_iu_fxu_exc_cond	R C3	3+R -	988 -4	448	390-7-16-1-Pl 0
		*			11.4	
	2 xeu_frc_milli_reg_n_lat_0/a 47_n994	F C	3+R	1761 -	-448	88 31 1 cl_invvn 07d SRL
	Cotum syou fro milli non a lot Olad		00.5	400		60 238 14 cl_invvn 07d
e de la companya de l	>{a} xc2857/y 0 n994	F C3+R	1761	-448	88	31 1 cs_nnd2n 02c NAND
	> xc2857/b 62 n505	R C3+R	1699	-448	104	17 1 cs_nnd2n 02c NAND
•	1200 slow_mode.c1_5>{a} xc2857/y 0 n994> xc2857/b 62 n505>{b} xc2834/y 0 n505	R C3+R	1699	-448	104	17 1 cs_nnd2n 02c NAND
	> xc2834/b 74 n1290	F C3+R	1625	-448		234 14 cs_nnd2n
	> xc2800/y 0 n1290	F C3+R	1625	-448	129	234 14 cs_invvn 08c NOT
	> xc2800/a 92 n1648	R C3+R	1533	-448	170	37 1 cs_invvn 08c NOT
	>{c} xc2779/y 0 n1648	R C3+R	1533	-448	170	37 1 cs_nnd2n 02c NAND
	> xc2779/b 114 n1645	F C3+R	1419	-448	164	151 6 cs_nnd2n 02c NAND
	> xc2646/y 0 n1645	F C3+R	1419	-448	164	151 6 cs_invvn 04c NOT
	> xc2646/a 114 n1746	R C3+R	1305	-448	110	21 1 cs_invvn 04c NOT
	>{d} xc2620/y 0 n1746	R C3+R	1305	-448	110	21 1 cs_nnd2n 02c NAND
	> xc2620/a 75 n1740	F C3+R	1230	-448	133	67 4 cs_nnd2n
	> xc2602/y	F C3+R	1230	-448	133	67 4 cs_invvn 02c NOT (

```
n1740
                                                                                                               37 2 cs invvn 02c NOT
                                                           R C3+R
                                                                             1135
                                                                                       -448
                                                                                                    146
----> xc2602/a
95 n905
                                                                                                                37 2 cs_nnd2n 02c NAND
---->{e} xc2546/y
                                                            R C3+R
                                                                              1135
                                                                                         -448
                                                                                                     146
0 n905
                                                           FC3+R
                                                                             1045
                                                                                        -448
                                                                                                     96
                                                                                                              17 1 cs_nnd2n 02c NAND
----> xc2546/a
90 n1647
                                                                             1045
                                                                                        -448
                                                                                                     96
                                                                                                             17 1 cs_invvn 01c NOT
                                                                                                                                                              0
                                                          FC3+R
----> xc1928/v
n1647
                                                                                                              16 1 cs_invvn 01c NOT
                                                                              988
                                                                                        -448
                                                                                                    390
                                                           RC3+R
----> xc1928/a
57 eu_iu_fxu_exc_cond
                                                                                                                                                         0
                                                                                                                      16 1 PI
                                                                                      988
                                                                                                -448
                                                                                                           390
                                                                   R C3+R
----> eu_iu_fxu_exc_cond
eu_iu_fxu_exc_cond
[CTE::cte_bd2epic]: pathmill_options: -b 3 -u -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill%/afs/apd/func/vlsi/alliance00/local/cmos8s/cm
os8s.pathmill.early -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c
[CTE::cte bd2epic]: bd2epic_options:
ASSERT(/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/IDCDSUC.assert)
WLCOUNT_CAP(/afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/IDCDSUC.nodeca
p) WLCOUNT_CAP_NODES() WIRE_CAP_CASE() PM_OPTIONS(-b 3 -u -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill%/afs/apd/func/vlsi/alliance00/local/cmos8s/cm
os8s.pathmill.early -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c)
        > CTE::bd2epic { NETLIST(/afs/apd/func/vlsi/alliance00/tim...
[bd2epic]: Release 1.2 Compiled on Jan 29 1999 at 16:19:04.
[bd2epic]: Asserting pathmill wire cap based on wlcount table estimates
[bd2epic]: Pathmill wire cap based on cap values
[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clkl_mode4) is missing timing information!
[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clkl_mode5) is missing timing information! [node_cap]: (W) Usage (xslow_mode_clockblock) pin (clkl_mode6) is missing timing information!
[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clkl_mode5) is missing timing information!
[node_cap]: (W) Usage (xslow_mode_clockblock) pin (clkl_mode8) is missing timing information!
                                The second secon
> pagnet [padnet]: Added 195 IOPADs.
        > padnet
          > idm::get active network
          > idm::foreach_proto_pin po -protobox __CiType_16_30a98de8...
           > idm::object_name __CiType_17_30aac34c
            > idm::get_net_from_proto_pin __CiType_17_30aac34c
              > idm::object_name __CiType_20_3057fc90
            > idm::object_name __CiType_17_30aac328
            > idm::get_net_from_proto_pin __CiType_17_30aac328
> idm::object_name __CiType_20_30590568
            > idm::object_name __CiType_17_30aac304
            > idm::get_net_from_proto_pin __CiType_17_30aac304
              > idm::object_name __CiType_20_3058f6e0
            > idm::object_name __CiType_17_30aac2e0
            > idm::get_net_from_proto_pin __CiType_17_30aac2e0
              > idm::object_name __CiType_20_3057f6c8
            > idm::object_name __CiType_17_30aac2bc
            > idm::get_net_from_proto_pin __CiType_17_30aac2bc
              > idm::object_name __CiType_20_3057fe48
            > idm::object_name __CiType_17_30aac298
            > idm::get_net_from_proto_pin __CiType_17_30aac298
              > idm::object_name __CiType_20_3059af68
            > idm::object_name __CiType_17_30a4bda8
```

```
> idm::get_net_from_proto_pin __CiType_17_30a4bda8
 > idm::object_name __CiType_20_3059ae78
> idm::object_name __CiType 17 30a4bd84
> idm::get_net_from_proto_pin __CiType_17_30a4bd84
 > idm::object_name __CiType_20_3057fd58
> idm::object_name __CiType_17_30a4bd60
> idm::get_net_from_proto_pin __CiType_17_30a4bd60
 > idm::object_name __CiType_20_30568e50
> idm::object_name __CiType_17 30a4bd3c
> idm::get_net_from_proto_pin __CiType_17_30a4bd3c
 > idm::object_name __CiType_20_3057fcb8
> idm::object_name __CiType_17_30a4bd18
> idm::get_net_from_proto_pin __CiType_17_30a4bd18
 > idm::object_name __CiType 20 3057fdf8
> idm::object_name __CiType_17_30a4bcf4
> idm::get_net_from_proto_pin __CiType_17_30a4bcf4
 > idm::object_name __CiType_20_3057f6a0
> idm::object_name __CiType_17_30a4bcd0
> idm::object_name __CiType 20 3056a2c8
> idm::object_name __CiType_17_30a4bcac
> idm::get_net_from_proto_pin __CiType_17_30a4bcac
 > idm::object_name __CiType_20_30568d88
> idm::object_name __CiType_17_30a4bc88
> idm::object_name ___CiType_20_3057ff60
> idm::object_name __CiType_17_30a4bc64
> idm::get_net_from_proto_pin __CiType_17_30a4bc64
> idm::object_name __CiType_20_3058fe60
> idm::object_name __CiType_17_30a4bc40
> idm::get_net_from_proto_pin __CiType_17_30a4bc40
 > idm::object_name __CiType_20_3057fdd0
> idm::object_name __CiType_17_30a4bc1c
> idm::get_net_from_proto_pin __CiType_17_30a4bc1c
> idm::object_name __CiType_20_3057f678
> idm::object_name __CiType_17_30a4bbf8
> idm::get_net_from_proto_pin ___CiType_17_30a4bbf8
 > idm::object_name __CiType_17_30a4bbb0
> idm::get_net_from_proto_pin __CiType_17_30a4bbb0
 > idm::object_name __CiType_17_30a4bb8c
> idm::get_net_from_proto_pin __CiType_17_30a4bb8c
 > idm::object_name __CiType_20_3057f628
> idm::object_name __CiType 17 30a4bb44
> idm::get_net_from_proto_pin __CiType_17_30a4bb44
 > idm::object_name __CiType_20_3057fa38
> idm::object_name __CiType_17_30a4bb20
> idm::get_net_from_proto_pin __CiType_17_30a4bb20
 > idm::object_name __CiType_17_30a4bad8
> idm::get_net_from_proto_pin __CiType_17_30a4bad8
 > idm::object_name __CiType_20_3057f600
> idm::object_name __CiType_17_30a4bab4
```

> idm::get\_net\_from\_proto\_pin \_\_CiType\_17\_30a4bab4

```
> idm::object_name __CiType_20_3057fa10
                      > idm::object_name __CiType_17_30a4ba90
                      > idm::get_net_from_proto_pin __CiType_17_30a4ba90
                       > idm::object_name __CiType_20_3057fd80
                      > idm::object_name __CiType_17_30a4ba6c
                      > idm::get_net_from_proto_pin __CiType_17_30a4ba6c
                       > idm::object_name __CiType_20_30568c98
                      > idm::object_name __CiType_17_30a4ba48
                      > idm::get_net_from_proto_pin __CiType_17_30a4ba48
                       > idm::object_name __CiType_20_3057f650
                      > idm::object_name __CiType_17_30a4ba24
                      > idm::get_net_from_proto_pin __CiType_17_30a4ba24
                        > idm::object_name __CiType_20_3057f7b8
                      > idm::object_name __CiType_17_30a4ba00
                      > idm::get_net_from_proto_pin __CiType_17_30a4ba00
                       > idm::object_name __CiType_20_3058fbb8
                      > idm::object_name __CiType_17_30a4b9dc
                      > idm::get_net_from_proto_pin __CiType_17_30a4b9dc
                        > idm::object_name.__CiType_20_3059b1c0
                      > idm::object_name __CiType_17_30a4b9b8
                      > idm::get_net_from_proto_pin __CiType_17_30a4b9b8
                       > idm::object_name __CiType_20_3057f808
                      > idm::object_name __CiType_17_30a4b994
> idm::get_net_from_proto_pin __CiType_17_30a4b994 --- > idm::object_name __CiType_20_3059b648
                      > idm::get_net_from_proto_pin __CiType_17_30a4b994
> idm::object_name __CiType_17_30a4b970

> idm::get_net_from_proto_pin __CiType_17_30a4b970

> idm::object_name __CiType_20_3057fec0

> idm::object_name __CiType_17_30a4b94c

> idm::get_net_from_proto_pin __CiType_17_30a4b94c

> idm::object_name __CiType_20_3057fda8

> idm::object_name __CiType_17_30a4b928

> idm::object_name __CiType_17_30a4b928
              > idm::get_name __CiType_17_30a4b928

> idm::get_net_from_proto_pin __CiType_17_30a4b928

> idm::object_name __CiType_20_3059b7d8

[CTE::fixup_po_nets]: (I) PO net 'dotr scan_out&0' doesn't match_BO land
               rename
                         > idm::locate_net -name gptr_scan_out -proto_box __CiType_...
                          > idm::set_net_name -net __CiType_20_3059b7d8 -name gptr_s...
                       > idm::object_name __CiType_17_30a4b904
                       > idm::get_net_from_proto_pin __CiType_17_30a4b904
                        > idm::object_name __CiType_20_3057ff10
                       > idm::get_net_from_proto_pin __CiType_17_30a4b8bc
                        > idm::object_name __CiType_20_3059b8f0
                       > idm::object_name __CiType_17_30a4b898
                       > idm::get_net_from_proto_pin __CiType_17_30a4b898
                        > idm::object_name __CiType_20_30590540
                       > idm::object name CiType_17_30a4b874
                       > idm::get_net_from_proto_pin __CiType_17_30a4b874
                        > idm::object_name __CiType_20_3057f790
                       > idm::object_name __CiType_17_30a4b850
                       > idm::get_net_from_proto_pin __CiType_17_30a4b850
                        > idm::object_name__CiType_20_3057fe70
                       > idm::get_net_from_proto_pin __CiType_17_30a4b82c
```

```
> idm::object_name __CiType_20_3057f998
> idm::object_name __CiType_17 30a4b808
> idm::get_net_from_proto_pin __CiType_17_30a4b808
 > idm::object_name __CiType_20_3057f970
> idm::object_name __CiType_17_30a4b7e4
> idm::object_name __CiType_17_30a4b7c0
> idm::get_net_from_proto_pin __CiType_17_30a4b7c0
 > idm::object_name __CiType_20_3057f920
> idm::object_name __CiType_17_30a4b79c
> idm::get net from proto pin CiType 17 30a4b79c
 > idm::object_name __CiType_20_3057f8d0
> idm::object_name __CiType_17_30a4b778
> idm::get_net_from_proto_pin __CiType_17_30a4b778
 > idm::object_name __CiType_20_3057f880
> idm::object_name __CiType 17 30a4b754
> idm::get net from proto pin CiType 17 30a4b754
 > idm::object_name __CiType_20_3057f858
> idm::object_name __CiType_17_30a4b730
> idm::get_net_from_proto_pin __CiType_17_30a4b730
 > idm::object_name __CiType_20_3057f830
> idm::object_name __CiType_17_30a4b70c
> idm::get_net_from_proto_pin __CiType_17_30a4b70c
> idm::object_name __CiType_20_3057fc40
> idm::object_name __CiType_17_30a4b6e8
> idm::get_net_from_proto_pin___CiType_17_30a4b6e8
 > idm::object_name __CiType_20_3057fc18
> idm::object_name __CiType_17_30a4b6c4
> idm::get_net_from_proto_pin:__CiType 17 30a4b6c4
> idm::object_name __CiType=20_3057fbf0
> idm::object_name __CiType 17 30a4b6a0
> idm::get_net_from_proto_pin __CiType_17_30a4b6a0
 > idm::object_name __CiType_20_3057fbc8
> idm::object_name __CiType_17_30a4b67c
> idm::get_net_from_proto_pin __CiType_17_30a4b67c
... > idm::object_name __CiType_20_3057fba0
> idm::object_name __CiType_17_30a4b634
> idm::get_net_from_proto_pin __CiType_17_30a4b634
 > idm::object_name __CiType_20_3057fb78
> idm::object_name __CiType_17_30a4b5ec
> idm::get_net_from_proto_pin __CiType_17 30a4b5ec
 > idm::object_name __CiType_20_3057fb50
> idm::object_name __CiType 17 30a4b5c8
> idm::get_net_from_proto_pin __CiType_17_30a4b5c8
 > idm::object_name __CiType_20_3057fb28
> idm::object_name __CiType_17_30a4b580
> idm::get_net_from_proto_pin __CiType_17_30a4b580
 > idm::object_name __CiType_20_3057fb00
> idm::object_name __CiType_17_30a4b55c
> idm::get_net_from_proto_pin __CiType_17_30a4b55c
 > idm::object_name __CiType_20_3057fad8
> idm::object_name __CiType_17_30a4b538
> idm::get_net_from_proto_pin __CiType_17_30a4b538
 > idm::object_name __CiType_20_3057fab0
```

```
> idm::object_name __CiType_17_30a4b514
      > idm::get_net_from_proto_pin __CiType_17_30a4b514
       > idm::object_name __CiType_20_3057fa88
      > idm::object_name __CiType_17_30a4b4f0
      > idm::get_net_from_proto_pin __CiType_17_30a4b4f0
       > idm::object_name __CiType_20_3057f9e8
      > idm::object_name __CiType_17_30a4b4cc
      > idm::get_net_from_proto_pin __CiType_17_30a4b4cc
       > idm::object_name __CiType_20_3057f9c0
      > idm::object_name __CiType_17_30a4b4a8
      > idm::get_net_from_proto_pin __CiType_17_30a4b4a8
       > idm::object_name __CiType_20_3057fd08
      > idm::object_name __CiType_17_30a4b484
      > idm::get_net_from_proto_pin __CiType_17_30a4b484
       > idm::object_name __CiType_20_3057fce0
      > idm::object_name __CiType_17_30a4b460
      > idm::get_net_from_proto_pin __CiType_17_30a4b460
       > idm::object_name __CiType_20_3057f5d8
      > idm::object_name __CiType_17_30a4b43c
      > idm::get_net_from_proto_pin __CiType_17_30a4b43c
       > idm::object_name __CiType_20_3057f5b0
      > idm::object_name __CiType_17_30a4b418
      > idm::get_net_from_proto_pin __CiType_17_30a4b418
       > idm::object_name __CiType_20_3057f588
      > idm::object_name ___CiType_17-230a4b3f4-
     > idm::get_net_from_proto_pin __CiType_17_30a4b3f4
     > idm::object_name __CiType_20_3057f560
     >-idm::object_name __CiType_17_30a4b3d0
      > idm::get_net_from_proto_pin __CiType_17_30a4b3d0
       > idm::object_name __CiType_20_3057f718
      > idm::get_net_from_proto_pin __CiType_17_30a4b3ac
     > idm::object_name __CiType_20_3057f6f0
      > idm::object_name __CiType_17_30a4b364
      > idm::get_net_from_proto_pin __CiType_17_30a4b364
       > idm::object_name __CiType_20_3057f768
      > idm::object_name __CiType_17_30a4b340
      > idm::get_net_from_proto_pin __CiType_17_30a4b340
       > idm::object_name __CiType_20_3057f740
   > write vim -library /afs/apd/func/vlsi/alliance00/timing/...
bdz> vim_preexport __CiType_16_30a98de8
Loading: /afs/watson.ibm.com/projects/vlsi/cte/tools/bd2/vol1/booledozer/4.1/tcl/constant_support.tcl
         > str_parm one_net_name
         > str_parm zero_net_name
         > is parm custom constants_kill_fanout_tree
          > is parm custom constants_kill_const_boxes
       > nextbox dot2ms()
>>]: nextbox( dot2ms() );
bdz> vim_postexport __CiType_16_30a98de8
        > str_parm one_net_name
        > str_parm zero_net_name
        > is_parm standard_constants_run_tiegen
       > nextnet ms2dot(BUS)
[
```

```
>>]: nextnet( ms2dot(BUS) );
Process took 709.21 cpu seconds or 00:20:19 wall time.
Used 39924388 bytes or 38 megs.
Highest message level was ERROR: 97 WARNING, 65 ERROR.
Return code 0
cte ci term
[DCL-17025]:
                            Start of Limit checking messages
                            End of Limit checking messages
*Info* Running Pathmill Model Build
CTE: Initializing for technology cmos8s
WARNING: Overriding technology files by command line parameter.
Preprocessing configuration file epic.inp --> epic.inp.final
 Include path for cpp...
  /afs/apd/func/vlsi/alliance00/libraries/pathmill/config
  /afs/watson/projects/vlsi/cte/tech/cmos8s/base/prod/pathmill/config
  /afs/apd/func/vlsi/alliance00/bscc8/prod/cc8s/pathmill/config
  /afs/watson/projects/vlsi/cte/tools/epic/5.1/local/pathmill/config
 Locating cpp include files for epic.inp...
  /afs/apd/func/vlsi/alliance00/libraries/pathmill/config/template.cfg
  -./IDCDSUC.assert-
  /afs/apd/func/vlsi/alliance00/libraries/pathmill/config/sets.cfg
  ./IDCDSUC.nodecap
 Executing /usr/ccs/lib/cpp...
 Executing PERL: substituting CTE vars and generating node lists...
Preprocessing completed successfully
*EXEC* /afs/apd/func/vlsi/alliance00/libraries/pathmill/audit/pm_audit_alli00 -U
/afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo
s8s.pathmill.early -x -n netlist -c epic.inp.final -L
/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice -b 3 -u -o build model
[pm_audit_alli00] Alliance 2000 Pathmill Audit Program (version 0.1)
[pm_audit_alli00] Executed: Sun Apr 18 22:10:20 EDT 1999
[pm_audit_alli00] WARNING -- Specified 2 tech files:
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early!
[pm_audit_alli00] CTE environment specifies...
[pm_audit_alli00] technology: cmos8s
[pm_audit_alli00] ibmtech verion: 5.1
[pm_audit_alli00] pathmill install: 5.1
[pm_audit_alli00] Checking netlist file: netlist
```

[pm\_audit\_alli00] WARNING -- Netlist is missing technology audit data! [pm\_audit\_alli00] Completed successfully

EPIC\_CC\_OPTIONS is set to: -D\_ENABLE\_HOOKS -D\_ENABLE\_HOOKS -D\_PROCESS\_MODEL

pathmill -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo s8s.pathmill.early -x -n netlist -c epic.inp.final -L /afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models -L /afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice -b 3 -u -o build\_model Building libCustom.o .... #! .epicrun/libCustom.o if\_setup epic\_mti\_if\_quit\_ack epicState shm\_put\_msg put msa ld: 0711-319 WARNING: Exported symbol not defined: estimateDeviceParameters ld: 0711-319 WARNING: Exported symbol not defined: timemill\_user\_init ld: 0711-319 WARNING: Exported symbol not defined: powrmill\_user\_init ld: 0711-319 WARNING: Exported symbol not defined: iAreaCap ld: 0711-319 WARNING: Exported symbol not defined: iDiffCap ld: 0711-319 WARNING: Exported symbol not defined: iFringeCap ld: 0711-319 WARNING: Exported symbol not defined: ilnit Id: 0711-319 WARNING: Exported symbol not defined: m12cc ld: 0711-319 WARNING: Exported symbol not defined: m12dw Id: 0711-319 WARNING: Exported symbol not defined: epicUserControl ld: 0711-319 WARNING: Exported symbol not defined: epicUserMain ld: 0711-319 WARNING: Exported symbol not defined: epic\_mti\_if\_quit\_ack ld: 0711-319 WARNING: Exported symbol not defined: if\_setup ld: 0711-319 WARNING: Exported symbol not defined: epicState

Notice: License pathmill will expire on 4/30/99.

ld: 0711-319 WARNING: Exported symbol not defined: shm\_put\_msg

ld: 0711-319 WARNING: Exported symbol not defined: put\_msq

## options:

pathmill -t -c epic.inp.final -p /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early -o build\_model -b 3 Simulator execution begins...

Using /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc\_mac/libCustom.o ...

Notice: License pathmill/pfx will expire on 4/30/99.

Compiling "netlist"

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Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cb\_mode\_block.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_mode\_block.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_invvn02.spi" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oPfet" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oNfet" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_invvn.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_lat\_core\_s.spi"
Notice: License spice\_parser will\_expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cb\_clk\_32\_1.spi"
Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_32\_1.spi" Notice: License spice\_parser will expire on 4/30/99.

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Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_se.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_clka.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv11e.spi" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oPfetLowVt" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oNfetLowVt" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn12c.spi" Notice; License spice\_parser will expire on 4/30/99.

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Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n02c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn01c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n04c.spi"

Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn15c.spi"
Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn11c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn13c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv19b.spi" Notice: License spice\_parser will expire on 4/30/99.

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Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2v05c.spi" Notice: License spice\_parser will expire on 4/30/99.

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Notice: License spice\_parser will expire on 4/30/99.

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Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv09c.spi"
Notice: License spice\_parser will expire on 4/30/99.

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Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd4v06c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn01e.spi"

PathMill Version 5.1plus |
SN: P013098-AIX |
Copyright (c) 1997 Synopsys Inc., All Rights Reserved.

Built by olevi in "PM\_DEV" on Fri Jan 30 12:01:27 PST 1998

Enabling ibmgray model bulding code.

Warning: invalid command or arguments on line 69 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill. corners 10 1.45

Warning: invalid command or arguments on line 1920 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill. corners 10 1.45

Warning: invalid command or arguments on line 68 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early. corners -10 1.70

Warning: invalid command or arguments on line 1919 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early. corners -10 1.70

## Done building data structure

CTE Pathmill post-processor: Determining clock nodes to ignore

CTE Pathmill post-processor: Determining pattern files from configuration file WARNING:PathMill:0x20521001:Node gptr\_scan\_out does not exist in netlist

WARNING:PathMill:0x20521001:Node gptr\_scan\_out does not exist in netlist

WARNING:PathMill:0x20525001:source\_node test\_c1 is set to LOW

WARNING:PathMill:0x20525001:source\_node scan\_in is set to LOW

WARNING:PathMill:0x20521001:Node scan\_in<0> does not exist in netlist

WARNING:PathMill:0x20521001:Node scan\_in<1> does not exist in netlist

WARNING:PathMill:0x20521001:Node scan\_in<2> does not exist in netlist

WARNING:PathMill:0x20525001:source\_node a\_clk is set to LOW

WARNING:PathMill:0x20525001:source\_node b\_clk is set to LOW

WARNING:PathMill:0x20525001:source\_node clkl\_mode7 is set to HIGH

WARNING:PathMill:0x20525001:source\_node gptr\_a\_clk is set to LOW

WARNING:PathMill:0x20525001:source\_node gptr\_b\_clk is set to LOW

WARNING:PathMill:0x20525001:source\_node gptr\_scan\_in is set to LOW

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_P465.IBMtech\_P(pf\_epic)

(I=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_P465.IBMtech\_P(pf\_epic)

(I=0.55u) is not in tech file.

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_N468.IBMtech\_N(nf\_epic)

(l=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_N468:IBMtech\_N(nf\_epic)

(I=0.55u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_P346.IBMtech\_P(pf\_e pic) (I=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_P346.IBMtech\_P(pf\_e pic) (I=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_N344.IBMtech\_N(nf\_e pic) (I=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_N344.IBMtech\_N(nf\_e pic) (I=0.65u) is not in tech file

Working in timing verify mode - clock edge reference, turning on the transparent\_mode

Unlimited transparency depth data\_to\_latch report is on latch\_to\_latch report is on gated\_clock report is on pattern acac\_drv2000: 0 matched pattern invmux: 0 matched pattern buffer2: 0 matched

pattern zljs\_clk\_core\_padc1: 0 matched

==> ibm\_gray: Opened the NT latch pattern list named:

/afs/apd/func/vlsi/alliance00/libraries/pathmill/patterns/nt\_latch\_pattern\_list

pattern zljs\_clk\_32\_1: 6 matched pattern zljs\_clk\_core: 6 matched pattern zljs\_clk\_corepar: 0 matched pattern zljs\_clk\_32\_2: 0 matched pattern zljs\_clk\_core: 0 matched pattern zljs\_clk\_corepar: 0 matched pattern zljs\_clk\_32\_3: 0 matched pattern zljs\_clk\_core3: 0 matched pattern zljs\_clk\_core3par: 0 matched pattern zljs\_lat\_core\_a: 0 matched pattern zljs\_lat\_core\_b: 83 matched pattern zljs\_lat\_core\_c: 0 matched pattern tg: 42 matched pattern 4ns: 0 matched pattern 4ps: 9 matched pattern 2ns: 96 matched pattern 2ps: 714 matched pattern 2ns1a: 28 matched pattern 2ps1a: 104 matched pattern 2ns1: 32 matched pattern 2ps1: 32 matched pattern 2ns2: 118 matched pattern 2ps2: 40 matched pattern XN4: 0 matched pattern XR4: 0 matched pattern XN3: 0 matched pattern XR3: 0 matched pattern XN2: 0 matched pattern XN2B: 1 matched pattern XN2BGoofyExtract: 0 matched pattern XR2: 0 matched pattern XR2B: 1 matched build model name idcdsuc\_mac 

Done reading setup file for build\_model characterize.file pattern zljs\_mode\_block: 0 matched pattern zljs\_mode\_block: 1 matched

Marking Inverters, Latches and RAM cells Finished Marking Inverters, Latches and RAM cells

Marking Transfer gates
Finished Marking Transfer gates

Setting transistor Directions
The percentage of elements with direction set is (including bi-directional) 100.00%.
Clock Propagation Begins
Clock Propagation End
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr\_latch.X\_mb.X\_mode<4>.l2
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock
xgptr\_latch.X\_mb.X\_mode<4>.l1\_n
WARNING:PathMill:0x20522006:Found a latch node without a controlling clock

xgptr\_latch.X\_mb.X\_mode<5>.l2

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr latch.X mb.X mode<5>.l1 n

ASPRIACOLATIONAL MODES SOLUTION

 $WARNING: PathMill: 0x20522006: Found a latch node without a controlling clock xgptr\_latch. X\_mb. X\_mode < 6 > . 12$ 

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xgptr\_latch.X\_mb.X\_mode<6>.l1\_n

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xgptr\_latch.X\_mb.X\_mode<7>.l2

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xgptr\_latch.X\_mb.X\_mode<7>.l1\_n

\*\*\* start calculating MAX clock skew \*\*\*

start propagating clock information for node clkg stop propagating clock information from node clkg

start propagating clock information for node clkg2 stop propagating clock information from node clkg2

\*\*\* finished calculating MAX clock skew \*\*\*

\*\*\* start calculating MIN clock skew \*\*\*

start propagating clock information for node clkg stop propagating clock information from node clkg

start propagating clock information for node clkg2 stop propagating clock information from node clkg2

\*\*\* finished calculating MIN clock skew \*\*\*

Path Search Begins

\*\*\* start searching LONGEST paths \*\*\*

start searching for source node clkg

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n stop searching from source node clkg

start searching for source node clkg2 stop searching from source node clkg2

start searching for source node op\_dsbl\_after stop searching from source node op\_dsbl\_after

start searching for source node eu\_iu\_spare1

stop searching from source node eu\_iu\_spare1

start searching for source node second\_op\_lat stop searching from source node second\_op\_lat

start searching for source node mcr41\_trap stop searching from source node mcr41\_trap

start searching for source node ifet\_xcptn stop searching from source node ifet\_xcptn

start searching for source node iu\_eu\_xcpt\_pend stop searching from source node iu\_eu\_xcpt\_pend

start searching for source node iq\_blk\_d1 stop searching from source node iq\_blk\_d1

start searching for source node dcd\_op\_44 stop searching from source node dcd\_op\_44

start searching for source node ru\_write\_in\_iq stop searching from source node ru\_write\_in\_iq

start searching for source node ru\_iu\_rcvy\_rst stop searching from source node ru\_iu\_rcvy\_rst

garanta da Santa da

start searching for source node eu\_iu\_enter\_slow\_md stop searching from source node eu\_iu\_enter\_slow\_md

start searching for source node id\_instr\_stores stop searching from source node id\_instr\_stores

start searching for source node op\_inq\_stores
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2766.X\_P1.IBMtech\_P to node n1115
DC path exists through the following transistors from node: n1115 to vdd
xc2766.X\_P2.IBMtech\_P
stop searching from source node op\_inq\_stores

start searching for source node iq\_blk\_aa stop searching from source node iq\_blk\_aa

start searching for source node aa\_ofc\_available stop searching from source node aa\_ofc\_available

start searching for source node eu\_iu\_mmode stop searching from source node eu\_iu\_mmode

start searching for source node eu\_iu\_mcset\_e1 stop searching from source node eu\_iu\_mcset\_e1

start searching for source node aa\_ofc\_hold stop searching from source node aa\_ofc\_hold

start searching for source node ru\_98\_43

stop searching from source node ru\_98\_43

start searching for source node srlz\_op\_match stop searching from source node srlz\_op\_match

start searching for source node first\_op\_lat stop searching from source node first\_op\_lat

start searching for source node zero\_branches stop searching from source node zero\_branches

start searching for source node dcd\_mcr41\_blk stop searching from source node dcd\_mcr41\_blk

start searching for source node xu\_iu\_xlat\_busy stop searching from source node xu\_iu\_xlat\_busy

start searching for source node du\_iu\_hold\_aa\_req stop searching from source node du\_iu\_hold\_aa\_req

start searching for source node eu\_iu\_fpu\_end\_op stop searching from source node eu\_iu\_fpu\_end\_op

start searching for source node eu\_iu\_misc\_hold stop searching from source node eu\_iu\_misc\_hold

start searching for source node op\_cmp\_raw stop searching from source node op\_cmp\_raw

start searching for source node op\_dsbl\_before stop searching from source node op\_dsbl\_before

start searching for source node op\_drain stop searching from source node op\_drain

start searching for source node eu\_iu\_fxu\_end\_op stop searching from source node eu\_iu\_fxu\_end\_op

start searching for source node op\_mcend\_raw stop searching from source node op\_mcend\_raw

start searching for source node need\_opnd\_req stop searching from source node need\_opnd\_req

start searching for source node legal\_bht\_br stop searching from source node legal\_bht\_br

start searching for source node bht\_branch\_req stop searching from source node bht\_branch\_req

start searching for source node id\_ex\_in\_mm stop searching from source node id\_ex\_in\_mm

start searching for source node du\_iu\_quiesced stop searching from source node du\_iu\_quiesced

start searching for source node iu\_op\_cmp\_hit\_a stop searching from source node iu\_op\_cmp\_hit\_a

start searching for source node iu\_op\_cmp\_hit\_b stop searching from source node iu\_op\_cmp\_hit\_b

start searching for source node iu\_op\_cmp\_hit\_c stop searching from source node iu\_op\_cmp\_hit\_c

start searching for source node iu\_op\_cmp\_hit\_d stop searching from source node iu\_op\_cmp\_hit\_d

start searching for source node dcd\_frc\_milli stop searching from source node dcd\_frc\_milli

start searching for source node iq\_empty stop searching from source node iq\_empty

start searching for source node op\_serialize stop searching from source node op\_serialize

start searching for source node aa\_agi\_lat stop searching from source node aa\_agi\_lat

start searching for source node branch\_request stop searching from source node branch\_request

start searching for source node ru\_9a\_52 stop searching from source node ru\_9a\_52

start searching for source node bu\_iu\_quiesced stop searching from source node bu\_iu\_quiesced

start searching for source node dcd\_blk\_dsucc stop searching from source node dcd\_blk\_dsucc

start searching for source node op\_eim\_dcd stop searching from source node op\_eim\_dcd

start searching for source node iqmcode\_mod\_390gr stop searching from source node iqmcode\_mod\_390gr

start searching for source node eu\_iu\_e1\_exc\_cond stop searching from source node eu\_iu\_e1\_exc\_cond

start searching for source node aa\_ofc\_block\_req

stop searching from source node aa\_ofc\_block\_req

start searching for source node eu\_iu\_fpu\_excpn stop searching from source node eu\_iu\_fpu\_excpn

start searching for source node block\_aa\_branch stop searching from source node block\_aa\_branch

start searching for source node ru\_iu\_rq\_blk stop searching from source node ru\_iu\_rq\_blk

start searching for source node op\_chkpt\_synch stop searching from source node op\_chkpt\_synch

start searching for source node ireg\_valid
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2752.X\_P1.IBMtech\_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X\_P2.IBMtech\_P
stop searching from source node ireg\_valid

start searching for source node ru\_9a\_36 stop searching from source node ru\_9a\_36

start searching for source node three\_branches stop searching from source node three\_branches

start searching for source node bht\_block\_dcd stop searching from source node bht\_block\_dcd

start searching for source node ru\_9a\_20 stop searching from source node ru\_9a\_20

start searching for source node iu\_eu\_data\_blocked stop searching from source node iu\_eu\_data\_blocked

start searching for source node op\_is\_44 stop searching from source node op\_is\_44

start searching for source node inst\_fetches stop searching from source node inst\_fetches

start searching for source node eu\_iu\_fxu\_exc\_cond stop searching from source node eu\_iu\_fxu\_exc\_cond

start searching for source node ru\_9a\_04 stop searching from source node ru\_9a\_04

start searching for source node br\_wrong\_targ
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P1<0>.IBMtech\_P to node
xex\_in\_prog\_reg\_n\_lat\_0.X\_core.I1\_n
DC path exists through the following transistors from node: xex\_in\_prog\_reg\_n\_lat\_0.dn to vdd
xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P2<0>.IBMtech\_P
stop searching from source node br\_wrong\_targ

start searching for source node scan\_enable stop searching from source node scan\_enable

start searching for source node du\_iu\_store\_status<0> stop searching from source node du\_iu\_store\_status<0>

start searching for source node du\_iu\_store\_status<1> stop searching from source node du\_iu\_store\_status<1>

start searching for source node du\_iu\_store\_status<2> stop searching from source node du\_iu\_store\_status<2>

start searching for source node eu\_iu\_srlz\_op\_actn<0> stop searching from source node eu\_iu\_srlz\_op\_actn<0>

start searching for source node eu\_iu\_srlz\_op\_actn<1> stop searching from source node eu\_iu\_srlz\_op\_actn<1>

start searching for source node ru\_9a\_0001<0> stop searching from source node ru\_9a\_0001<0>

start searching for source node ru\_9a\_0001<1> stop searching from source node ru\_9a\_0001<1>

start searching for source node ireg\_0\_1<0> stop searching from source node ireg\_0\_1<0>

start searching for source node ireg\_0\_1<1>
stop searching from source node ireg\_0\_1<1>

start searching for source node num\_dcd\_cyl<0> stop searching from source node num\_dcd\_cyl<0>

start searching for source node num\_dcd\_cyl<1> stop searching from source node num\_dcd\_cyl<1>

start searching for source node ru\_9a\_3233<32> stop searching from source node ru\_9a\_3233<32>

start searching for source node ru\_9a\_3233<33> stop searching from source node ru\_9a\_3233<33>

start searching for source node eu\_iu\_interrupt\_info<0> stop searching from source node eu\_iu\_interrupt\_info<0>

start searching for source node eu\_iu\_interrupt\_info<1> stop searching from source node eu\_iu\_interrupt\_info<1>

start searching for source node eu\_iu\_interrupt\_info<2> stop searching from source node eu\_iu\_interrupt\_info<2>

start searching for source node eu\_iu\_interrupt\_info<3> stop searching from source node eu\_iu\_interrupt\_info<3>

start searching for source node ru\_9a\_1617<16>

stop searching from source node ru\_9a 1617<16>

start searching for source node ru\_9a\_1617<17> stop searching from source node ru\_9a\_1617<17>

start searching for source node eu\_iu\_srlz\_op\_encode<0> stop searching from source node eu\_iu\_srlz\_op\_encode<0>

start searching for source node eu\_iu\_srlz\_op\_encode<1> stop searching from source node eu\_iu\_srlz\_op\_encode<1>

start searching for source node eu\_iu\_srlz\_op\_encode<2>stop searching from source node eu\_iu\_srlz\_op\_encode<2>

start searching for source node eu\_iu\_srlz\_op\_encode<3> stop searching from source node eu\_iu\_srlz\_op\_encode<3>

start searching for source node eu\_iu\_srlz\_op\_encode<4> stop searching from source node eu\_iu\_srlz\_op\_encode<4>

start searching for source node eu\_iu\_srlz\_op\_encode<5> stop searching from source node eu\_iu\_srlz\_op\_encode<5>

start searching for source node eu\_iu\_srlz\_op\_encode<6> stop searching from source node eu\_iu\_srlz\_op\_encode<6>

start searching for source node eu\_iu\_srlz\_op\_encode<7>
stop searching from source node eu\_iu\_srlz\_op\_encode<7>

start searching for source node eu\_iu\_srlz\_op\_encode<8> stop searching from source node eu\_iu\_srlz\_op\_encode<8>

start searching for source node eu\_iu\_srlz\_op\_encode<9> stop searching from source node eu\_iu\_srlz\_op\_encode<9>

start searching for source node eu\_iu\_srlz\_op\_encode<10> stop searching from source node eu\_iu\_srlz\_op\_encode<10>

start searching for source node eu\_iu\_srlz\_op\_encode<11> stop searching from source node eu\_iu\_srlz\_op\_encode<11>

start searching for source node ru\_9a\_4849<48> stop searching from source node ru\_9a\_4849<48>

start searching for source node ru\_9a\_4849<49> stop searching from source node ru\_9a\_4849<49>

start searching for source node ireg\_1631<22> stop searching from source node ireg\_1631<22>

start searching for source node ireg\_1631<23> stop searching from source node ireg\_1631<23>

start searching for source node ireg\_1631<24> stop searching from source node ireg\_1631<24>

start searching for source node ireg\_1631<25> stop searching from source node ireg\_1631<25>

start searching for source node ireg\_1631<26> stop searching from source node ireg\_1631<26>

start searching for source node ireg\_1631<27> stop searching from source node ireg\_1631<27>

start searching for source node ireg\_1631<28> stop searching from source node ireg\_1631<28>

start searching for source node ireg\_1631<29> stop searching from source node ireg\_1631<29>

start searching for source node ireg\_1631<30> stop searching from source node ireg\_1631<30>

\*\*\* finished searching LONGEST paths \*\*\*

\*\*\* start searching SHORTEST paths \*\*\*

start searching for source node clkg WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate:X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_qate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n stop searching from source node clkg

start searching for source node clkg2 stop searching from source node clkg2

start searching for source node op\_dsbl\_after stop searching from source node op\_dsbl\_after

start searching for source node eu\_iu\_spare1 stop searching from source node eu\_iu\_spare1

start searching for source node second\_op\_lat stop searching from source node second\_op\_lat

start searching for source node mcr41\_trap stop searching from source node mcr41\_trap

start searching for source node ifet\_xcptn stop searching from source node ifet\_xcptn

start searching for source node iu\_eu\_xcpt\_pend stop searching from source node iu\_eu\_xcpt\_pend

start searching for source node iq\_blk\_d1 stop searching from source node iq\_blk\_d1

start searching for source node dcd\_op\_44 stop searching from source node dcd\_op\_44

start searching for source node ru\_write\_in\_iq stop searching from source node ru\_write\_in\_iq

start searching for source node ru\_iu\_rcvy\_rst stop searching from source node ru\_iu\_rcvy\_rst

start searching for source node eu\_iu\_enter\_slow\_md stop searching from source node eu\_iu\_enter\_slow\_md

start searching for source node id\_instr\_stores stop searching from source node id\_instr\_stores

start searching for source node op\_inq\_stores stop searching from source node op\_inq\_stores

start searching for source node iq\_blk\_aa stop searching from source node iq\_blk\_aa

start searching for source node aa\_ofc\_available stop searching from source node aa\_ofc\_available

start searching for source node eu\_iu\_mmode stop searching from source node eu\_iu\_mmode

start searching for source node eu\_iu\_mcset\_e1 stop searching from source node eu\_iu\_mcset\_e1

start searching for source node aa\_ofc\_hold stop searching from source node aa\_ofc\_hold

start searching for source node ru\_98\_43 stop searching from source node ru\_98\_43

start searching for source node srlz\_op\_match stop searching from source node srlz\_op\_match

start searching for source node first\_op\_lat stop searching from source node first\_op\_lat

start searching for source node zero\_branches stop searching from source node zero\_branches

start searching for source node dcd\_mcr41\_blk

stop searching from source node dcd\_mcr41\_blk

start searching for source node xu\_iu\_xlat\_busy stop searching from source node xu\_iu\_xlat\_busy

start searching for source node du\_iu\_hold\_aa\_req stop searching from source node du\_iu\_hold\_aa\_req

start searching for source node eu\_iu\_fpu\_end\_op stop searching from source node eu\_iu\_fpu\_end\_op

start searching for source node eu\_iu\_misc\_hold stop searching from source node eu\_iu\_misc\_hold

start searching for source node op\_cmp\_raw stop searching from source node op\_cmp\_raw

start searching for source node op\_dsbl\_before stop searching from source node op\_dsbl\_before

start searching for source node op\_drain stop searching from source node op\_drain

start searching for source node eu\_iu\_fxu\_end\_op stop searching from source node eu\_iu\_fxu\_end\_op

start searching for source node op\_mcend\_raw stop searching from source node op\_mcend\_raw

start searching for source node need\_opnd\_req stop searching from source node need\_opnd\_req

start searching for source node legal\_bht\_br stop searching from source node legal\_bht\_br

start searching for source node bht\_branch\_req stop searching from source node bht\_branch\_req

start searching for source node id\_ex\_in\_mm stop searching from source node id\_ex\_in\_mm

start searching for source node du\_iu\_quiesced stop searching from source node du\_iu\_quiesced

start searching for source node iu\_op\_cmp\_hit\_a stop searching from source node iu\_op\_cmp\_hit\_a

start searching for source node iu\_op\_cmp\_hit\_b stop searching from source node iu\_op\_cmp\_hit\_b

start searching for source node iu\_op\_cmp\_hit\_c stop searching from source node iu\_op\_cmp\_hit\_c

start searching for source node iu\_op\_cmp\_hit\_d stop searching from source node iu\_op\_cmp\_hit\_d

start searching for source node dcd\_frc\_milli stop searching from source node dcd\_frc\_milli

start searching for source node iq\_empty stop searching from source node iq\_empty

start searching for source node op\_serialize stop searching from source node op\_serialize

start searching for source node aa\_agi\_lat stop searching from source node aa\_agi\_lat

start searching for source node branch\_request stop searching from source node branch\_request

start searching for source node ru\_9a\_52 stop searching from source node ru\_9a\_52

start searching for source node bu\_iu\_quiesced stop searching from source node bu\_iu\_quiesced

start searching for source node dcd\_blk\_dsucc stop searching from source node dcd\_blk\_dsucc

start searching for source node op\_eim\_dcd stop searching from source node op\_eim\_dcd

start searching for source node iqmcode\_mod\_390gr stop searching from source node iqmcode\_mod\_390gr

start searching for source node eu\_iu\_e1\_exc\_cond stop searching from source node eu\_iu\_e1\_exc\_cond

start searching for source node aa\_ofc\_block\_req stop searching from source node aa\_ofc\_block\_req

start searching for source node eu\_iu\_fpu\_excpn stop searching from source node eu\_iu\_fpu\_excpn

start searching for source node block\_aa\_branch stop searching from source node block\_aa\_branch

start searching for source node ru\_iu\_rq\_blk stop searching from source node ru\_iu\_rq\_blk

start searching for source node op\_chkpt\_synch

stop searching from source node op\_chkpt\_synch

start searching for source node ireg\_valid
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2752.X\_P1.IBMtech\_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X\_P2.IBMtech\_P
stop searching from source node ireg\_valid

start searching for source node ru\_9a\_36 stop searching from source node ru\_9a\_36

start searching for source node three\_branches stop searching from source node three\_branches

start searching for source node bht\_block\_dcd stop searching from source node bht\_block\_dcd

start searching for source node ru\_9a\_20 stop searching from source node ru\_9a\_20

start searching for source node iu\_eu\_data\_blocked stop searching from source node iu\_eu\_data\_blocked

start searching for source node op\_is\_44 stop searching from source node op\_is\_44

start searching for source node inst\_fetches stop searching from source node inst\_fetches

start searching for source node eu\_iu\_fxu\_exc\_cond stop searching from source node eu\_iu\_fxu\_exc\_cond

start searching for source node ru\_9a\_04 stop searching from source node ru\_9a\_04

start searching for source node br\_wrong\_targ
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P1<0>.IBMtech\_P to node
xex\_in\_prog\_reg\_n\_lat\_0.X\_core.l1\_n
DC path exists through the following transistors from node: xex\_in\_prog\_reg\_n\_lat\_0.dn to vdd
xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P2<0>.IBMtech\_P
stop searching from source node br\_wrong\_targ

start searching for source node scan\_enable stop searching from source node scan\_enable

start searching for source node du\_iu\_store\_status<0> stop searching from source node du\_iu\_store\_status<0>

start searching for source node du\_iu\_store\_status<1> stop searching from source node du\_iu\_store\_status<1>

start searching for source node du\_iu\_store\_status<2> stop searching from source node du\_iu\_store\_status<2>

start searching for source node eu\_iu\_srlz\_op\_actn<0> stop searching from source node eu\_iu\_srlz\_op\_actn<0>

start searching for source node eu\_iu\_srlz\_op\_actn<1> stop searching from source node eu\_iu\_srlz\_op\_actn<1>

start searching for source node ru\_9a\_0001<0> stop searching from source node ru\_9a\_0001<0>

start searching for source node ru\_9a\_0001<1> stop searching from source node ru\_9a\_0001<1>

start searching for source node ireg\_0\_1<0> stop searching from source node ireg\_0\_1<0>

start searching for source node ireg\_0\_1<1>
stop searching from source node ireg\_0\_1<1>

start searching for source node num\_dcd\_cyl<0>
stop searching from source node num\_dcd\_cyl<0>

start searching for source node num\_dcd\_cyl<1> stop searching from source node num\_dcd\_cyl<1>

start searching for source node ru\_9a\_3233<32> stop searching from source node ru\_9a\_3233<32>

start searching for source node ru\_9a\_3233<33> stop searching from source node ru\_9a\_3233<33>

start searching for source node eu\_iu\_interrupt\_info<0>
stop searching from source node eu\_iu\_interrupt\_info<0>

start searching for source node eu\_iu\_interrupt\_info<1> stop searching from source node eu\_iu\_interrupt\_info<1>

start searching for source node eu\_iu\_interrupt\_info<2> stop searching from source node eu\_iu\_interrupt\_info<2>

start searching for source node eu\_iu\_interrupt\_info<3> stop searching from source node eu\_iu\_interrupt\_info<3>

start searching for source node ru\_9a\_1617<16> stop searching from source node ru\_9a\_1617<16>

start searching for source node ru\_9a\_1617<17> stop searching from source node ru\_9a\_1617<17>

start searching for source node eu\_iu\_srlz\_op\_encode<0> stop searching from source node eu\_iu\_srlz\_op\_encode<0>

start searching for source node eu\_iu\_srlz\_op\_encode<1> stop searching from source node eu\_iu\_srlz\_op\_encode<1>

start searching for source node eu iu srlz op encode<2>

stop searching from source node eu\_iu\_srlz\_op\_encode<2>

start searching for source node eu\_iu\_srlz\_op\_encode<3> stop searching from source node eu\_iu\_srlz\_op\_encode<3>

start searching for source node eu\_iu\_srlz\_op\_encode<4> stop searching from source node eu\_iu\_srlz\_op\_encode<4>

start searching for source node eu\_iu\_srlz\_op\_encode<5> stop searching from source node eu\_iu\_srlz\_op\_encode<5>

start searching for source node eu\_iu\_srlz\_op\_encode<6> stop searching from source node eu\_iu\_srlz\_op\_encode<6>

start searching for source node eu\_iu\_srlz\_op\_encode<7> stop searching from source node eu\_iu\_srlz\_op\_encode<7>

start searching for source node eu\_iu\_srlz\_op\_encode<8> stop searching from source node eu\_iu\_srlz\_op\_encode<8>

start searching for source node eu\_iu\_srlz\_op\_encode<9> stop searching from source node eu\_iu\_srlz\_op\_encode<9>

start searching for source node eu\_iu\_srlz\_op\_encode<10> stop searching from source node eu\_iu\_srlz\_op\_encode<10>

start searching for source node eu\_iu\_srlz\_op\_encode<11> stop searching from source node eu\_iu\_srlz\_op\_encode<11>

start searching for source node ru\_9a\_4849<48> stop searching from source node ru\_9a\_4849<48>

start searching for source node ru\_9a\_4849<49> stop searching from source node ru\_9a\_4849<49>

and the second of the second o

start searching for source node ireg\_1631<22> stop searching from source node ireg\_1631<22>

start searching for source node ireg\_1631<23> stop searching from source node ireg\_1631<23>

start searching for source node ireg\_1631<24> stop searching from source node ireg\_1631<24>

start searching for source node ireg\_1631<25> stop searching from source node ireg\_1631<25>

start searching for source node ireg\_1631<26> stop searching from source node ireg\_1631<26>

start searching for source node ireg\_1631<27> stop searching from source node ireg\_1631<27>

start searching for source node ireg\_1631<28> stop searching from source node ireg\_1631<28>

start searching for source node ireg\_1631<29> stop searching from source node ireg\_1631<29>

start searching for source node ireg\_1631<30> stop searching from source node ireg\_1631<30> .

\*\*\* finished searching SHORTEST paths \*\*\*

\*\*\* Critical Paths Search Completed. \*\*\*

\*\*\* Printing Reports. \*\*\*

A total of 2000 timing errors were reported in build\_model.err A total of 200 critical paths were reported in build\_model.out

\*\*\*Node Slopes

## NODES WITH LARGE SLOPE

\_\_\_\_\_\_

## NODE <-> slowest slope <-> node causing this transition

	0.487 F 0.422 F 0.407 F 0.423 R 0.53 F 0.44 R		<iiuii></iiuii>	
eu_iu_misc_hold	0.415 R		<null></null>	
eu_iu_srlz_op_encode<11> eu_iu_srlz_op_actn<0>		0.625 F	-	<null></null>
eu_iu_srlz_op_actn<0>	0.467 F		<null></null>	
eu_iu_srlz_op_actn<1>	0.426 F		<null></null>	_
eu_iu_srlz_op_encode<5>		0.466 F		<null></null>
eu_iu_srlz_op_encode<4>		0.507 R		<null></null>
eu_iu_srlz_op_encode<6>		0.442 R		<null></null>
eu_iu_srlz_op_encode<7>		0.497 R		<null></null>
eu_iu_srlz_op_encode<8>		0.458 F		<null></null>
eu_iu_srlz_op_encode<9>		0.403 R		<null></null>
eu_iu_srlz_op_encode<2>		0.525 F		<null></null>
eu_iu_srlz_op_encode<1>		0.5 R		<null></null>
eu_iu_srlz_op_encode<0>		0.501 F		<null></null>
du_iu_store_status<2>	0.625 F		<null></null>	

## \*\*\*End Node Slopes

==> ibm\_gray: Starting generation of PathMill IBMgray file. Program version: Version 04/23/98

==> ibm\_gray: Writing output messages into file: idcdsuc\_mac.ibmgray.log ...

==> ibm\_gray: Program finished, now exiting.

==> ibm\_gray: Starting generation of PathMill IBMgray file.

==> ibm\_gray: Program log file generated by ibm\_gray program Version 04/23/98

==> ibm\_gray: Program run on: Sun Apr 18 22:16:29 1999

==> ibm\_gray: Pathmill version: PATHMILL PM DEV

==> ibm\_gray: No latches were flagged as NON-TRANSPARENT by the PathMill patterns!

```
==> ibm_gray: Data Gathering Phase ....
==> ibm gray: Storing list of dynamic nodes, latches, and clock gates...
==> ibm_gray: Total number of dangling nodes found: 0
==> ibm_gray: Gathering data on clock tree nodes...
==> ibm_gray: Gathering data on model segments and nodes...
==> ibm_gray: Writing out the data into file: idcdsuc_mac.ibmgray ...
==> ibm_gray: Number of PIS found:
==> ibm_gray: Number of POS found:
                                           0
==> ibm_gray: Number of LATCHS found:
==> ibm_gray: Number of NON-TRANS LATCHS found: 0
==> ibm gray: Number of DYNAMIC CIRCUITS found: 0
==> ibm_gray: Number of CLOCK GATES found:
==> ibm_gray: Number of GLOBAL CLK SEGS found: 0
==> ibm_gray: Number of OTHER PROP SEGS found: 0
==> ibm gray: Program finished, now exiting.
```

CTE Pathmill post-processor: Determining quality record from configuration file CTE Pathmill post-processor: Determining clock information from pathmill data CTE Pathmill post-processor: Determining worst internal setup and hold slacks

Start writing model file idcdsuc\_mac.c Finished writing model file

\*\*\* Finished Printing Reports. \*\*\*

\*Info\* Pathmill model build finished with a return code of: 0

\*Info\* Running Pathmill Path Search\_

CTE: Initializing for technology cmos8s.

WARNING: Overriding technology files by command line parameter.

Preprocessing configuration file epic.inp --> epic.inp.final

Include path for cpp...

/afs/apd/func/vlsi/alliance00/libraries/pathmill/config /afs/watson/projects/vlsi/cte/tech/cmos8s/base/prod/pathmill/config /afs/apd/func/vlsi/alliance00/bscc8/prod/cc8s/pathmill/config /afs/watson/projects/vlsi/cte/tools/epic/5.1/local/pathmill/config

Locating cpp include files for epic.inp...
/afs/apd/func/vlsi/alliance00/libraries/pathmill/config/template.cfg
./IDCDSUC.assert
/afs/apd/func/vlsi/alliance00/libraries/pathmill/config/sets.cfg
./IDCDSUC.nodecap

Executing /usr/ccs/lib/cpp...

Executing PERL: substituting CTE vars and generating node lists...

Preprocessing completed successfully \*EXEC\* /afs/apd/func/vlsi/alliance00/libraries/pathmill/audit/pm\_audit\_alli00 -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p

```
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo
 s8s.pathmill.early -x -n netlist -c epic.inp.final -L
 /afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
 /afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice -b 3 -u
 [pm_audit_alli00] Alliance 2000 Pathmill Audit Program (version 0.1)
 [pm_audit_alli00] Executed: Sun Apr 18 22:16:44 EDT 1999
 [pm_audit_alli00] WARNING -- Specified 2 tech files:
 /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill
 /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early!
 [pm_audit_alli00] CTE environment specifies...
 [pm_audit_alli00] technology: cmos8s
 [pm_audit_alli00] ibmtech verion: 5.1
 [pm_audit_alli00] pathmill install: 5.1
 [pm_audit_alli00] Checking netlist file: netlist
 [pm_audit_alli00] WARNING -- Netlist is missing technology audit data!
 [pm_audit_alli00] Completed successfully
 EPIC_CC_OPTIONS is set to: -D_ENABLE_HOOKS -D_PROCESS_MODEL
pathmill -U /afs/apd/func/vlsi/alliance00/libraries/pathmill/lib/customize.c -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo
                                       thmill/spice -b 3 -u
s8s.pathmill.early -x -n netlist -c epic.inp.final -L
/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech_models -L
/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice -b 3 -u
Building libCustom.o ....
#! .epicrun/libCustom.o
                         ----
#! .epicrun/libCustom.o

if_setup

epic_mti_if_quit_ack

epicState
                    shm_put_msg
put msq
ld: 0711-319 WARNING: Exported symbol not defined: estimateDeviceParameters
ld: 0711-319 WARNING: Exported symbol not defined: timemill_user_init
ld: 0711-319 WARNING: Exported symbol not defined: powrmill_user_init
ld: 0711-319 WARNING: Exported symbol not defined: iAreaCap
ld: 0711-319 WARNING: Exported symbol not defined: iDiffCap
ld: 0711-319 WARNING: Exported symbol not defined: iFringeCap
ld: 0711-319 WARNING: Exported symbol not defined: ilnit
ld: 0711-319 WARNING: Exported symbol not defined: m12cc
ld: 0711-319 WARNING: Exported symbol not defined: m12dw
ld: 0711-319 WARNING: Exported symbol not defined: epicUserControl
ld: 0711-319 WARNING: Exported symbol not defined: epicUserMain
ld: 0711-319 WARNING: Exported symbol not defined: epic mti if quit ack
ld: 0711-319 WARNING: Exported symbol not defined: if setup
ld: 0711-319 WARNING: Exported symbol not defined: epicState
ld: 0711-319 WARNING: Exported symbol not defined: shm put msa
ld: 0711-319 WARNING: Exported symbol not defined: put_msq
Using /afs/apd/func/vlsi/alliance00/timing/bsiu/batchz/pathmill/idcdsuc_mac/libCustom.o ...
Notice: License pathmill will expire on 4/30/99.
options:
pathmill -t -c epic.inp.final -p
/afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill:/afs/apd/func/vlsi/alliance00/local/cmos8s/cmo
```

s8s.pathmill.early -o pathmill.out -b 3 Simulator execution begins...

Notice: License pathmill/pfx will expire on 4/30/99.

Compiling "netlist"

Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cb\_mode\_block.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_mode\_block.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_invvn02.spi"——Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oPfet" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oNfet" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_invvn.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_lat\_core\_s.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cb\_clk\_32\_1.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_32\_1.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_core.spi"

Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_se.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_clk\_clka.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv11e.spi" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oPfetLowVt" Compiling "/afs/apd/func/vlsi/alliance00/libraries/pathmill/ibmtech\_models/pm\_oNfetLowVt" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn12c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn09c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n02c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn01c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n04c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn15c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn11c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn13c.spi" Notice: License spice parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv19b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn06c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2v05c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn08c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn12d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn02c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv14c.spi"...
Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn04c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn05c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n12c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3n02c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor2n02c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_ao22n03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3v02c.spi"

Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2v13c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor2n04c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd4n03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn14c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_ao12n03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_xbn2n01b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3n03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor3n03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_oa21n10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n11c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_oa22n10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_xbo2n01d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2x14c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_ao12n10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2v13d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn06d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_ao22n04c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2x14e.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd4n05d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_ao22n10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2x14b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3i11b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd4v10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2g14e.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd4v10b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_oa21n10e.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_ao12n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n08c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv13b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor2g12e.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv13c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2v14c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor2n06d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor3v10e.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn16c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvv09c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3n05c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2n05c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nor2v11c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2v11c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2g11b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3z10c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_invvn07d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/zljs\_lat\_core\_b.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_invvn07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_nnd2n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_nnd2n02.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_invvn05c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_ao22n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_ao22n02.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_invvn06d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_invvn05d.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_nnd3n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_nnd3n02.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_nor2n06c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_nor2n02.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_ao21n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_ao21n02.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_invvn06c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cl\_oa21n07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cc\_oa21n02.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd2f03c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd3z07c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_nnd4v06c.spi" Notice: License spice\_parser will expire on 4/30/99.

Compiling "/afs/apd/func/vlsi/alliance00/bscc8/prod/pathmill/spice/cs\_invvn01e.spi"

PathMill Version 5.1plus | SN: P013098-AIX | Copyright (c) 1997 Synopsys Inc., All Rights Reserved. |

Built by olevi in " PM\_DEV " on Fri Jan 30 12:01:27 PST 1998

Enabling ibmgray model bulding code.

Warning: invalid command or arguments on line 69 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill. corners 10 1.45

Warning: invalid command or arguments on line 1920 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill. corners 10 1.45

Warning: invalid command or arguments on line 68 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early.corners -10 1.70

Warning: invalid command or arguments on line 1919 in file /afs/apd/func/vlsi/alliance00/local/cmos8s/cmos8s.pathmill.early. corners -10 1.70

Done building data structure CTE Pathmill post-processor: Determining clock nodes to ignore CTE Pathmill post-processor: Determining pattern files from configuration file WARNING:PathMill:0x20521001:Node gptr\_scan\_out does not exist in netlist WARNING:PathMill:0x20521001:Node gptr\_scan\_out does not exist in netlist WARNING:PathMill:0x20525001:source\_node test\_c1 is set to LOW WARNING:PathMill:0x20525001:source\_node scan\_in is set to LOW WARNING:PathMill:0x20521001:Node scan\_in<0> does not exist in netlist WARNING:PathMill:0x20521001:Node scan\_in<1> does not exist in netlist WARNING:PathMill:0x20521001:Node scan\_in<2> does not exist in netlist WARNING:PathMill:0x20525001:source\_node a\_clk is set to LOW WARNING:PathMill:0x20525001:source\_node b\_clk is set to LOW WARNING:PathMill:0x20525001:source\_node clkl\_mode7 is set to HIGH WARNING:PathMill:0x20525001:source\_node gptr\_a\_clk is set to LOW WARNING:PathMill:0x20525001:source\_node gptr\_b\_clk is set to LOW WARNING:PathMill:0x20525001:source\_node gptr\_scan\_in is set to LOW WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_P465.IBMtech\_P(pf\_epic) (I=0.55u) is not in tech file WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_P465.IBMtech\_P(pf\_epic) (I=0.55u) is not in tech file WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_N468.IBMtech\_N(nf\_epic) (I=0.55u) is not in tech file WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_core.X\_N468.IBMtech\_N(nf\_epic) (I=0.55u) is not in tech file WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_P346.IBMtech\_P(pf\_e pic) (I=0.65u) is not in tech file

WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_P346.IBMtech\_P(pf\_e pic) (l=0.65u) is not in tech file WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_N344.IBMtech\_N(nf\_e pic) (l=0.65u) is not in tech file WARNING:PathMill:0x20551015:xslow\_mode\_clockblock.X\_cb.X\_scan\_enable.X\_N344.IBMtech\_N(nf\_e pic) (l=0.65u) is not in tech file

Working in timing verify mode - clock edge reference, turning on the transparent\_mode

Unlimited transparency depth data\_to\_latch report is on latch\_to\_latch report is on gated\_clock report is on pattern acac\_drv2000: 0 matched pattern invmux: 0 matched pattern buffer2: 0 matched pattern zljs\_clk\_core\_padc1: 0 matched ==> ibm\_gray: Opened the NT latch pattern list named: /afs/apd/func/vlsi/alliance00/libraries/pathmill/patterns/nt\_latch\_pattern\_list pattern zljs\_clk\_32\_1: 6 matched pattern zljs\_clk\_core: 6 matched pattern zljs\_clk\_corepar: 0 matched pattern zljs\_clk\_32\_2: 0 matched pattern zljs\_clk\_core: 0 matched pattern zljs\_clk\_corepar: 0 matched pattern zljs\_clk\_32\_3: 0 matched pattern zlis clk core3: 0 matched pattern zlis\_clk\_core3par: 0 matched pattern zljs\_lat\_core\_a: 0 matched pattern zlis\_lat\_core\_b: 83 matched pattern zljs\_lat\_core\_c: 0 matched pattern tg: 42 matched pattern 4ns: 0 matched pattern 4ps: 9 matched pattern 2ns: 96 matched pattern 2ps: 714 matched pattern 2ns1a: 28 matched pattern 2ps1a: 104 matched pattern 2ns1: 32 matched pattern 2ps1: 32 matched pattern 2ns2: 118 matched pattern 2ps2: 40 matched pattern XN4: 0 matched pattern XR4: 0 matched pattern XN3: 0 matched pattern XR3: 0 matched pattern XN2: 0 matched pattern XN2B: 1 matched pattern XN2BGoofyExtract: 0 matched pattern XR2: 0 matched pattern XR2B: 1 matched

Done reading setup file for build\_model characterize.file

build model name idcdsuc mac

pattern zljs\_mode\_block: 0 matched pattern zljs\_mode\_block: 1 matched

Marking Inverters, Latches and RAM cells Finished Marking Inverters, Latches and RAM cells

Marking Transfer gates
Finished Marking Transfer gates

**Setting transistor Directions** 

The percentage of elements with direction set is (including bi-directional) 100.00%.

**Clock Propagation Begins** 

Clock Propagation End

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr latch.X\_mb.X\_mode<4>.l2

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xgptr\_latch.X\_mb.X\_mode<4>.l1\_n

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr latch.X\_mb.X\_mode<5>.l2

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr\_latch.X\_mb.X\_mode<5>.l1\_n

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xgptr latch.X mb.X\_mode<6>.l2

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr\_latch.X\_mb.X\_mode<6>.l1\_n

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr\_latch.X\_mb.X\_mode<7>.l2

WARNING:PathMill:0x20522006:Found a latch node without a controlling clock xqptr\_latch.X\_mb.X\_mode<7>.l1\_n

\*\*\* start calculating MAX clock skew \*\*\*

start propagating clock information for node clkg stop propagating clock information from node clkg

start propagating clock information for node clkg2 stop propagating clock information from node clkg2

\*\*\* finished calculating MAX clock skew \*\*\*

\*\*\* start calculating MIN clock skew \*\*\*

start propagating clock information for node clkg stop propagating clock information from node clkg

start propagating clock information for node clkg2 stop propagating clock information from node clkg2

\*\*\* finished calculating MIN clock skew \*\*\*

Path Search Begins

\*\*\* start searching LONGEST paths \*\*\*

start searching for source node clkg WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n stop searching from source node clkg

start searching for source node clkg2 stop searching from source node clkg2

start searching for source node op\_dsbl\_after stop searching from source node op\_dsbl\_after

start searching for source node eu\_iu\_spare1 stop searching from source node eu\_iu\_spare1

start searching for source node second\_op\_lat stop searching from source node second\_op\_lat

start searching for source node mcr41\_trap
stop searching from source node mcr41\_trap

start searching for source node ifet\_xcptn stop searching from source node ifet\_xcptn

start searching for source node iu\_eu\_xcpt\_pend stop searching from source node iu\_eu\_xcpt\_pend

start searching for source node iq\_blk\_d1 stop searching from source node iq\_blk\_d1

start searching for source node dcd\_op\_44 stop searching from source node dcd\_op\_44

start searching for source node ru\_write\_in\_iq stop searching from source node ru\_write\_in\_iq

start searching for source node ru\_iu\_rcvy\_rst stop searching from source node ru\_iu\_rcvy\_rst

start searching for source node eu\_iu\_enter\_slow\_md stop searching from source node eu\_iu\_enter\_slow\_md

start searching for source node id\_instr\_stores stop searching from source node id\_instr\_stores

start searching for source node op\_inq\_stores
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2766.X\_P1.IBMtech\_P to node n1115
DC path exists through the following transistors from node: n1115 to vdd

xc2766.X\_P2.IBMtech\_P stop searching from source node op\_inq\_stores

start searching for source node iq\_blk\_aa stop searching from source node iq\_blk\_aa

start searching for source node aa\_ofc\_available stop searching from source node aa\_ofc\_available

start searching for source node eu\_iu\_mmode stop searching from source node eu\_iu\_mmode

start searching for source node eu\_iu\_mcset\_e1 stop searching from source node eu\_iu\_mcset\_e1

start searching for source node aa\_ofc\_holdstop searching from source node aa\_ofc\_hold

start searching for source node ru\_98\_43 stop searching from source node ru\_98\_43

start searching for source node srlz\_op\_match stop searching from source node srlz\_op\_match

start searching for source node first\_op\_lat stop searching from source node first\_op\_lat

start searching for source node zero\_branches stop searching from source node zero\_branches

start searching for source node dcd\_mcr41\_blk stop searching from source node dcd\_mcr41\_blk

start searching for source node xu\_iu\_xlat\_busy stop searching from source node xu\_iu\_xlat\_busy

start searching for source node du\_iu\_hold\_aa\_req stop searching from source node du\_iu\_hold\_aa\_req

start searching for source node eu\_iu\_fpu\_end\_op stop searching from source node eu\_iu\_fpu\_end\_op

start searching for source node eu\_iu\_misc\_hold stop searching from source node eu\_iu\_misc\_hold

start searching for source node op\_cmp\_raw stop searching from source node op\_cmp\_raw

start searching for source node op\_dsbl\_before stop searching from source node op\_dsbl\_before

start searching for source node op\_drain stop searching from source node op\_drain

start searching for source node eu\_iu\_fxu\_end\_op

stop searching from source node eu\_iu\_fxu\_end\_op

start searching for source node op\_mcend\_raw stop searching from source node op\_mcend\_raw

start searching for source node eu\_iu\_br\_wrong WARNING:PathMill:0x20532001:

Can't simulate delay from tx xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P1<0>.IBMtech\_P to node xex\_in\_prog\_reg\_n\_lat\_0.X\_core.l1\_n

DC path exists through the following transistors from node: xex\_in\_prog\_reg\_n\_lat\_0.dn to vdd xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P2<0>.IBMtech\_P

stop searching from source node eu\_iu\_br\_wrong

start searching for source node need\_opnd\_req stop searching from source node need\_opnd\_req

start searching for source node legal\_bht\_br stop searching from source node legal\_bht\_br

start searching for source node bht\_branch\_req stop searching from source node bht\_branch\_req

start searching for source node id\_ex\_in\_mm stop searching from source node id\_ex\_in\_mm

start searching for source node du\_iu\_quiesced stop searching from source node du\_iu\_quiesced

start searching for source node iu\_op\_cmp\_hit\_a stop searching from source node iu\_op\_cmp\_hit\_a

start searching for source node iu\_op\_cmp\_hit\_b stop searching from source node iu\_op\_cmp\_hit\_b

start searching for source node iu\_op\_cmp\_hit\_c stop searching from source node iu\_op\_cmp\_hit\_c

start searching for source node iu\_op\_cmp\_hit\_d stop searching from source node iu\_op\_cmp\_hit\_d

start searching for source node dcd\_frc\_milli stop searching from source node dcd\_frc\_milli

start searching for source node iq\_empty stop searching from source node iq\_empty

start searching for source node op\_serialize stop searching from source node op\_serialize

start searching for source node aa\_agi\_lat stop searching from source node aa\_agi\_lat

start searching for source node branch\_request stop searching from source node branch\_request

start searching for source node ru\_9a\_52 stop searching from source node ru\_9a\_52

start searching for source node bu\_iu\_quiesced stop searching from source node bu\_iu\_quiesced.

start searching for source node dcd\_blk\_dsucc stop searching from source node dcd\_blk\_dsucc

start searching for source node op\_eim\_dcd stop searching from source node op\_eim\_dcd

start searching for source node iqmcode\_mod\_390gr stop searching from source node iqmcode\_mod\_390gr

start searching for source node eu\_iu\_e1\_exc\_cond stop searching from source node eu\_iu\_e1\_exc\_cond

start searching for source node aa\_ofc\_block\_req stop searching from source node aa\_ofc\_block\_req

start searching for source node eu\_iu\_fpu\_excpn stop searching from source node eu\_iu\_fpu\_excpn

start searching for source node block\_aa\_branch stop searching from source node block\_aa\_branch

start searching for source node ru\_iu\_rq\_blk stop searching from source node ru\_iu\_rq\_blk

start searching for source node op\_chkpt\_synch stop searching from source node op\_chkpt\_synch

start searching for source node ireg\_valid
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2752.X\_P1.IBMtech\_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X\_P2.IBMtech\_P
stop searching from source node ireg\_valid

start searching for source node ru\_9a\_36 stop searching from source node ru\_9a\_36

start searching for source node three\_branches stop searching from source node three\_branches

start searching for source node bht\_block\_dcd stop searching from source node bht\_block\_dcd

start searching for source node ru\_9a\_20 stop searching from source node ru\_9a\_20

start searching for source node iu\_eu\_data\_blocked stop searching from source node iu\_eu\_data\_blocked

start searching for source node op\_is\_44 stop searching from source node op is\_44

start searching for source node inst\_fetches stop searching from source node inst\_fetches

start searching for source node eu\_iu\_fxu\_exc\_cond stop searching from source node eu\_iu\_fxu\_exc\_cond

start searching for source node ru\_9a\_04 stop searching from source node ru\_9a\_04

start searching for source node br\_wrong\_targ
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P1<0>.IBMtech\_P to node
xex\_in\_prog\_reg\_n\_lat\_0.X\_core.I1\_n
DC path exists through the following transistors from node: xex\_in\_prog\_reg\_n\_lat\_0.dn to vdd
xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P2<0>.IBMtech\_P
stop searching from source node br\_wrong\_targ

start searching for source node scan\_enable stop searching from source node scan\_enable

المتعددة الشعفان وإعراضها أأطره أأأ العرأ الوار

start searching for source node du\_iu\_store\_status<0> stop searching from source node du\_iu\_store\_status<0>

start searching for source node du\_iu\_store\_status<1> stop searching from source node du\_iu\_store\_status<1>

The second secon

start searching for source node du\_iu\_store\_status<2> stop searching from source node du\_iu\_store\_status<2>

start searching for source node eu\_iu\_srlz\_op\_actn<0> stop searching from source node eu\_iu\_srlz\_op\_actn<0>

start searching for source node eu\_iu\_srlz\_op\_actn<1> stop searching from source node eu\_iu\_srlz\_op\_actn<1>

start searching for source node ru\_9a\_0001<0> stop searching from source node ru\_9a\_0001<0>

start searching for source node ru\_9a\_0001<1> stop searching from source node ru\_9a\_0001<1>

start searching for source node ireg\_0\_1<0> stop searching from source node ireg\_0\_1<0>

start searching for source node ireg\_0\_1<1> stop searching from source node ireg\_0\_1<1>

start searching for source node num\_dcd\_cyl<0> stop searching from source node num\_dcd\_cyl<0>

start searching for source node num\_dcd\_cyl<1> stop searching from source node num\_dcd\_cyl<1>

start searching for source node ru\_9a\_3233<32> stop searching from source node ru\_9a\_3233<32>

start searching for source node ru\_9a\_3233<33> stop searching from source node ru\_9a\_3233<33>

start searching for source node eu\_iu\_interrupt\_info<0> stop searching from source node eu\_iu\_interrupt\_info<0>

start searching for source node eu\_iu\_interrupt\_info<1> stop searching from source node eu\_iu\_interrupt\_info<1>

start searching for source node eu\_iu\_interrupt\_info<2> stop searching from source node eu\_iu\_interrupt\_info<2>

start searching for source node eu\_iu\_interrupt\_info<3> stop searching from source node eu\_iu\_interrupt\_info<3>

start searching for source node ru\_9a\_1617<16> stop searching from source node ru\_9a\_1617<16>

start searching for source node ru\_9a\_1617<17> stop searching from source node ru\_9a\_1617<17>

start searching for source node eu\_iu\_srlz\_op\_encode<0> stop searching from source node eu\_iu\_srlz\_op\_encode<0>

start searching for source node eu\_iu\_srlz\_op\_encode<1> stop searching from source node eu\_iu\_srlz\_op\_encode<1>

start searching for source node eu\_iu\_srlz\_op\_encode<2> stop searching from source node eu\_iu\_srlz\_op\_encode<2>

start searching for source node eu\_iu\_srlz\_op\_encode<3> stop searching from source node eu\_iu\_srlz\_op\_encode<3>

start searching for source node eu\_iu\_srlz\_op\_encode<4> stop searching from source node eu\_iu\_srlz\_op\_encode<4>

start searching for source node eu\_iu\_srlz\_op\_encode<5> stop searching from source node eu\_iu\_srlz\_op\_encode<5>

start searching for source node eu\_iu\_srlz\_op\_encode<6> stop searching from source node eu\_iu\_srlz\_op\_encode<6>

start searching for source node eu\_iu\_srlz\_op\_encode<7> stop searching from source node eu\_iu\_srlz\_op\_encode<7>

start searching for source node eu\_iu\_srlz\_op\_encode<8> stop searching from source node eu\_iu\_srlz\_op\_encode<8>

start searching for source node eu\_iu\_srlz\_op\_encode<9> stop searching from source node eu\_iu\_srlz\_op\_encode<9>

start searching for source node eu\_iu\_srlz\_op\_encode<10>

stop searching from source node eu\_iu\_srlz\_op\_encode<10>

start searching for source node eu\_iu\_srlz\_op\_encode<11>
stop searching from source node eu\_iu\_srlz\_op\_encode<11>

start searching for source node ru\_9a\_4849<48> stop searching from source node ru\_9a\_4849<48>

start searching for source node ru\_9a\_4849<49> stop searching from source node ru\_9a\_4849<49>

start searching for source node ireg\_1631<22> stop searching from source node ireg\_1631<22>

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start searching for source node ireg\_1631<29> stop searching from source node ireg\_1631<29>

start searching for source node ireg\_1631<30> stop searching from source node ireg\_1631<30>

\*\*\* finished searching LONGEST paths \*\*\*

start searching for source node clkg
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n
WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx
xnum\_dcd\_reg\_n\_lat\_1.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_1.X\_core.l1\_n

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<sup>\*\*\*</sup> start searching SHORTEST paths \*\*\*

WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<0>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n WARNING:PathMill:0x20596001:side branch limit reduced to 0 to compute delay from tx xnum\_dcd\_reg\_n\_lat\_0.X\_gate.X\_N4<1>.IBMtech\_N to node xnum\_dcd\_reg\_n\_lat\_0.X\_core.l1\_n stop searching from source node clkg

start searching for source node clkg2 stop searching from source node clkg2

start searching for source node op\_dsbl\_after stop searching from source node op\_dsbl\_after

start searching for source node eu\_iu\_spare1 stop searching from source node eu\_iu\_spare1

start searching for source node second\_op\_lat stop searching from source node second\_op\_lat

start searching for source node-mcr41\_trap stop searching from source node mcr41\_trap

start searching for source node ifet\_xcptn stop searching from source node ifet\_xcptn

start searching for source node iu\_eu\_xcpt\_pend stop searching from source node iu\_eu\_xcpt\_pend

start searching for source node iq\_blk\_d1 stop searching from source node iq\_blk\_d1

start searching for source node dcd\_op\_44 stop searching from source node dcd\_op\_44

start searching for source node ru\_write\_in\_iq stop searching from source node ru\_write\_in\_iq

start searching for source node ru\_iu\_rcvy\_rst stop searching from source node ru\_iu\_rcvy\_rst

start searching for source node eu\_iu\_enter\_slow\_md stop searching from source node eu\_iu\_enter\_slow\_md

start searching for source node id\_instr\_stores stop searching from source node id\_instr\_stores

start searching for source node op\_inq\_stores stop searching from source node op\_inq\_stores

start searching for source node iq\_blk\_aa stop searching from source node iq\_blk\_aa

start searching for source node aa\_ofc\_available stop searching from source node aa\_ofc\_available

start searching for source node eu\_iu\_mmode

stop searching from source node eu\_iu\_mmode

start searching for source node eu\_iu\_mcset\_e1 stop searching from source node eu\_iu\_mcset\_e1

start searching for source node aa\_ofc\_hold stop searching from source node aa\_ofc\_hold

start searching for source node ru\_98\_43 stop searching from source node ru\_98\_43

start searching for source node srlz\_op\_match stop searching from source node srlz\_op\_match

start searching for source node first\_op\_lat stop searching from source node first\_op\_lat

start searching for source node zero\_branches stop searching from source node zero\_branches

start searching for source node dcd\_mcr41\_blk stop searching from source node dcd\_mcr41\_blk

start searching for source node xu\_iu\_xlat\_busy stop searching from source node xu\_iu\_xlat\_busy

start searching for source node du\_iu\_hold\_aa\_req stop searching from source node du\_iu\_hold\_aa\_req

start searching for source node eu\_iu\_fpu\_end\_op stop searching from source node eu\_iu\_fpu\_end\_op

start searching for source node eu\_iu\_misc\_hold stop searching from source node eu\_iu\_misc\_hold

start searching for source node op\_cmp\_raw stop searching from source node op\_cmp\_raw

start searching for source node op\_dsbl\_before stop searching from source node op\_dsbl\_before

start searching for source node op\_drain stop searching from source node op\_drain

start searching for source node eu\_iu\_fxu\_end\_op stop searching from source node eu\_iu\_fxu\_end\_op

start searching for source node op\_mcend\_raw stop searching from source node op\_mcend\_raw

start searching for source node eu\_iu\_br\_wrong
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P1<0>.IBMtech\_P to node
xex\_in\_prog\_reg\_n\_lat\_0.X\_core.l1\_n
DC path exists through the following transistors from node: xex\_in\_prog\_reg\_n\_lat\_0.dn to vdd

xex\_in\_prog\_reg\_n\_lat\_0.X\_gate.X\_P2<0>.IBMtech\_P\_stop searching from source node eu\_iu\_br\_wrong

start searching for source node need\_opnd\_req stop searching from source node need\_opnd\_req.

start searching for source node legal\_bht\_br stop searching from source node legal\_bht\_br

start searching for source node bht\_branch\_req stop searching from source node bht\_branch\_req

start searching for source node id\_ex\_in\_mm stop searching from source node id\_ex\_in\_mm

start searching for source node du\_iu\_quiesced stop searching from source node du\_iu\_quiesced

start searching for source node iu\_op\_cmp\_hit\_a stop searching from source node iu\_op\_cmp\_hit\_a

start searching for source node iu\_op\_cmp\_hit\_b stop searching from source node iu\_op\_cmp\_hit\_b

start searching for source node iu\_op\_cmp\_hit\_c stop searching from source node iu\_op\_cmp\_hit\_c

start searching for source node iu\_op\_cmp\_hit\_d stop searching from source node iu\_op\_cmp\_hit\_d

start searching for source node dcd\_frc\_milli stop searching from source node dcd\_frc\_milli

start searching for source node iq\_empty stop searching from source node iq\_empty

start searching for source node op\_serialize stop searching from source node op\_serialize

start searching for source node aa\_agi\_lat stop searching from source node aa\_agi\_lat

start searching for source node branch\_request stop searching from source node branch\_request

start searching for source node ru\_9a\_52 stop searching from source node ru\_9a\_52

start searching for source node bu\_iu\_quiesced stop searching from source node bu\_iu\_quiesced

start searching for source node dcd\_blk\_dsucc stop searching from source node dcd\_blk\_dsucc

start searching for source node op\_eim\_dcd

stop searching from source node op\_eim\_dcd

start searching for source node iqmcode\_mod\_390gr stop searching from source node iqmcode\_mod\_390gr

start searching for source node eu\_iu\_e1\_exc\_cond stop searching from source node eu\_iu\_e1\_exc\_cond

start searching for source node aa\_ofc\_block\_req stop searching from source node aa\_ofc\_block\_req

start searching for source node eu\_iu\_fpu\_excpn stop searching from source node eu\_iu\_fpu\_excpn

start searching for source node block\_aa\_branch stop searching from source node block\_aa\_branch

start searching for source node ru\_iu\_rq\_blk stop searching from source node ru\_iu\_rq\_blk

start searching for source node op\_chkpt\_synch stop searching from source node op\_chkpt\_synch

start searching for source node ireg\_valid
WARNING:PathMill:0x20532001:
Can't simulate delay from tx xc2752.X\_P1.IBMtech\_P to node n1415
DC path exists through the following transistors from node: n1415 to vdd
xc2752.X\_P2.IBMtech\_P
stop searching from source node ireg\_valid

start searching for source node ru\_9a\_36 stop searching from source node ru\_9a\_36

start searching for source node three\_branches stop searching from source node three\_branches

start searching for source node bht\_block\_dcd stop searching from source node bht\_block\_dcd

start searching for source node ru\_9a\_20 stop searching from source node ru\_9a\_20

start searching for source node iu\_eu\_data\_blocked stop searching from source node iu\_eu\_data\_blocked

start searching for source node op\_is\_44 stop searching from source node op\_is\_44

start searching for source node inst\_fetches stop searching from source node inst\_fetches

start searching for source node eu\_iu\_fxu\_exc\_cond stop searching from source node eu\_iu\_fxu\_exc\_cond

start searching for source node ru 9a 04

stop searching from source node ru\_9a\_04

start searching for source node scan\_enable stop searching from source node scan\_enable

start searching for source node du\_iu\_store\_status<0> stop searching from source node du\_iu\_store\_status<0>

start searching for source node du\_iu\_store\_status<1> stop searching from source node du\_iu\_store\_status<1>

start searching for source node du\_iu\_store\_status<2> stop searching from source node du\_iu\_store\_status<2>

start searching for source node eu\_iu\_srlz\_op\_actn<0> stop searching from source node eu\_iu\_srlz\_op\_actn<0>

start searching for source node eu\_iu\_srlz\_op\_actn<1> stop searching from source node eu\_iu\_srlz\_op\_actn<1>

start searching for source node ru\_9a\_0001<0> stop searching from source node ru\_9a\_0001<0>

start searching for source node ru\_9a\_0001<1> stop searching from source node ru\_9a\_0001<1>

start searching for source node ireg\_0\_1<0> stop searching from source node ireg\_0\_1<0>

start searching for source node ireg\_0\_1<1> stop searching from source node ireg\_0\_1<1>

start searching for source node num\_dcd\_cyl<0> stop searching from source node num\_dcd\_cyl<0>

start searching for source node num\_dcd\_cyl<1> stop searching from source node num\_dcd\_cyl<1>

start searching for source node ru\_9a\_3233<32> stop searching from source node ru\_9a\_3233<32>

start searching for source node ru\_9a\_3233<33> stop searching from source node ru\_9a\_3233<33>

start searching for source node eu\_iu\_interrupt\_info<0> stop searching from source node eu\_iu\_interrupt\_info<0>

start searching for source node eu\_iu\_interrupt\_info<1> stop searching from source node eu\_iu\_interrupt\_info<1>

start searching for source node eu\_iu\_interrupt\_info<2> stop searching from source node eu\_iu\_interrupt\_info<2>

start searching for source node eu\_iu\_interrupt\_info<3> stop searching from source node eu\_iu\_interrupt\_info<3>

start searching for source node ru\_9a\_1617<16> stop searching from source node ru\_9a\_1617<16>

start searching for source node ru\_9a\_1617<17> stop searching from source node ru\_9a\_1617<17>

start searching for source node eu\_iu\_srlz\_op\_encode<0> stop searching from source node eu\_iu\_srlz\_op\_encode<0>

start searching for source node eu\_iu\_srlz\_op\_encode<1> stop searching from source node eu\_iu\_srlz\_op\_encode<1>

start searching for source node eu\_iu\_srlz\_op\_encode<2> stop searching from source node eu\_iu\_srlz\_op\_encode<2>

start searching for source node eu\_iu\_srlz\_op\_encode<3> stop searching from source node eu\_iu\_srlz\_op\_encode<3>

start searching for source node eu\_iu\_srlz\_op\_encode<4> stop searching from source node eu\_iu\_srlz\_op\_encode<4>

start searching for source node eu\_iu\_srlz\_op\_encode<5> stop searching from source node eu\_iu\_srlz\_op\_encode<5>

start searching for source node eu\_iu\_srlz\_op\_encode<6> stop searching from source node eu\_iu\_srlz\_op\_encode<6>

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start searching for source node eu\_iu\_srlz\_op\_encode<9> stop searching from source node eu\_iu\_srlz\_op\_encode<9>

start searching for source node eu\_iu\_srlz\_op\_encode<10> stop searching from source node eu\_iu\_srlz\_op\_encode<10>

start searching for source node eu\_iu\_srlz\_op\_encode<11> stop searching from source node eu\_iu\_srlz\_op\_encode<11>

start searching for source node ru\_9a\_4849<48> stop searching from source node ru\_9a\_4849<48>

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stop searching from source node ru\_9a\_4849<49>

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start searching for source node ireg\_1631<29> stop searching from source node ireg\_1631<29>

start searching for source node ireg\_1631<30> stop searching from source node ireg\_1631<30>

- \*\*\* finished searching SHORTEST paths \*\*\*
- \*\*\* Critical Paths Search Completed. \*\*\*
- \*\*\* Printing Reports. \*\*\*

A total of 2000 timing errors were reported in pathmill.err A total of 200 critical paths were reported in pathmill.out

## NODES WITH LARGE SLOPE

## NODE <-> slowest slope <-> node causing this transition

eu_iu_fxu_exc_cond	0.487 F	<null></null>
du_iu_quiesced	0.422 F	<null></null>
eu_iu_mmode	0.407 F	<null></null>
eu_iu_fpu_end_op	0.423 R	<null></null>
du_iu_hold_aa_req	0.53 F	<null></null>
eu_iu_enter_slow_md	0.44 R	<null></null>
eu_iu_misc_hold	0.415 R	<null></null>
eu_iu_srlz_op_encode<11>	0.625	F
eu iu srlz on actn<0>	0 467 F	<null></null>

<null>

<sup>\*\*\*</sup>Node Slopes

eu_iu_srlz_op_actn<1>	0.426 F		<null></null>	
eu_iu_srlz_op_encode<5>	0.4201	0.466 F	VIIII)	<null></null>
eu_iu_srlz_op_encode<4>		0.507 R		<null></null>
eu_iu_srlz_op_encode<6>		0.442 R		<null></null>
eu_iu_srlz_op_encode<7>		• • • • •		<null></null>
eu_iu_srlz_op_encode<8>		0.458 F		<null></null>
eu_iu_srlz_op_encode<9>		0.403 R		<null></null>
eu_iu_srlz_op_encode<2>		0.525 F		<null></null>
eu_iu_srlz_op_encode<1>		0.5 R		<null></null>
eu_iu_srlz_op_encode<0>		0.501 F		<null></null>
du_iu_store_status<2>	0.625 F		<null></null>	
***End Node Slopes				
ib Chartian conora	tion of DothMill IDA	Acros file D	oarom voroi	an: Varaiar

```
==> ibm_qray: Starting generation of PathMill IBMgray file. Program version: Version 04/23/98
```

==> ibm\_gray: Writing output messages into file: idcdsuc\_mac.ibmgray.log ...

==> ibm\_gray: Program finished, now exiting.

==> ibm\_gray: Starting generation of PathMill IBMgray file.

==> ibm\_gray: Program log file generated by ibm\_gray program Version 04/23/98

==> ibm\_gray: Program run on: Sun Apr 18 22:23:03 1999

==> ibm\_gray: Pathmill version: PATHMILL PM\_DEV

==> ibm\_gray: No latches were flagged as NON-TRANSPARENT by the PathMill patterns!

==> ibm\_gray: Data Gathering Phase ....

==> ibm\_gray: Storing list of dynamic nodes, latches, and clock gates...

==> ibm\_gray: Total number of dangling nodes found: 0

==> ibm\_gray: Gathering data on clock tree nodes...

==> ibm\_gray: Gathering data on model segments and nodes...

==> ibm\_gray: Writing out the data into file: idcdsuc\_mac.ibmgray ...

==> ibm\_gray: Number of PIS found:

==> ibm\_gray: Number of POS found:

==> ibm gray: Number of LATCHS found:

==> ibm gray: Number of NON-TRANS LATCHS found: 0 ==> ibm\_gray: Number of DYNAMIC CIRCUITS found: 0

==> ibm\_gray: Number of CLOCK GATES found:

==> ibm\_gray: Number of GLOBAL CLK SEGS found: 0

==> ibm\_gray: Number of OTHER PROP SEGS found: 0

==> ibm\_gray: Program finished, now exiting.

CTE Pathmill post-processor: Determining quality record from configuration file CTE Pathmill post-processor: Determining clock information from pathmill data CTE Pathmill post-processor: Determining worst internal setup and hold slacks

Start writing model file idcdsuc\_mac.c Finished writing model file

\*Info\* Pathmill path search finished with a return code of: 0 laceyl: Message sent

This file is not changed; compression does not save space.

<sup>\*\*\*</sup> Finished Printing Reports. \*\*\*

feedback directory is defaulted to /afs/apd/func/vlsi/alliance00/timing/bsiu/actual/ WARNING no pis record for aa\_blk\_dcd\_prtIR, using default WARNING no pis record for aa\_blk\_dcd\_prtlF, using default WARNING no pis record for bht\_block\_dcdR, using default WARNING no pis record for bht\_block\_dcdF, using default WARNING no pos record for iu\_slow\_mode\_t1R, using default WARNING no eta record for iu\_slow\_mode\_t1R, using default WARNING no pos record for iu\_slow\_mode\_t1F, using default WARNING no eta record for iu slow\_mode\_t1F, using default WARNING no pos record for iu\_reset\_op\_c\_t1R, using default WARNING no eta record for iu\_reset\_op\_c\_t1R, using default WARNING no pos record for iu\_reset\_op\_c\_t1F, using default WARNING no eta record for iu\_reset\_op\_c\_t1F, using default WARNING no eta record for iu milli\_mode\_t2R, using default WARNING no eta record for iu\_milli\_mode\_t2F, using default WARNING no pos record for iu\_reset\_op\_c\_t1R, using default WARNING no pos record for iu\_reset\_op\_c\_t1F, using default WARNING no pos record for iu\_slow\_mode\_t1R, using default WARNING no pos record for iu\_slow\_mode\_t1F, using default WARNING no eta record for idcdsuc\_errR, using default WARNING no eta record for idcdsuc errF, using default WARNING no pos record for iu\_reset\_op\_c\_t1R, using default WARNING no pos record for iu\_reset\_op\_c\_t1F, using default WARNING no pos record for iu\_reset\_op\_c\_t1R, using default

WARNING no pos record for iu\_reset\_op\_c\_t1F, using default

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Be it known that in connection with my accompanying affidavit and log file appended to an affidavit of Yau-Hing Chan, I, Lisa Bryant Lacey, retrieved the following lines of information, to help clarify. I added a comment in the log "\*\*\*\*\*POU92000-0107US1\*\*\*\*\* code invocation" that should the reader of these pages.

\*\*\*\*\*POU92000-0107US1\*\*\*\*\* code invocation [tc\_parm]: [set\_benefit\_per\_unit\_cost]: calculated margin is 6.090000 > critical repower (SCORE (ALL), REPOWER\_GROUP (TAPERED), TAPER... critical ( repower (SCORE (ALL), REPOWER\_GROUP (TAPERED), TAPERED\_PIN\_SWAP) ); -1865.06 Avg: -167.73 maximum area for proto box IDCDSUC is 4606 repower: setting SCORE option to ALL. repower: setting TAPERED\_PIN\_SWAP option.

Also, to document the date, note that the log maintains the date when run

\*\*\*\*\*POU92000-0107US1\*\*\*\* code invocation date Sun Apr 18 21:58:17 1999

Part : IDCDSUC

Sworn to an subscribed before me, this  $\frac{23}{}$ 

day of February, 2005

At Poughkeepsie, New York.

Sandra Kilmer, Notary Public, Dutchess County, New

LYN

SANDRA LYN KILMER Notary Fullic, State of New York No. 5562885

**Qualified in Dutchess County** Commission Expires 10. 30.

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